Dielectric and carrier transport properties of vanadium dioxide thin films across the phase transition utilizing gated capacitor devices

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Vanadium dioxide (VO_2) is a strongly correlated oxide that undergoes a sharp metal-insulator transition (MIT) in the vicinity of room temperature. Fundamental knowledge of the semiconducting properties of thin film VO_2 is needed to advance our understanding of the microscopic transition mechanisms that are presently being actively explored and also for novel electron devices that could utilize the phase transition. In this report, the temperature dependence of the dielectric constant and carrier conduction in VO_2 thin films are investigated, from quantitative capacitance-voltage analyses of a multilayer capacitor with $HfO_2/VO_2/HfO_2/n$-Si-substrate stack structure. The finite conductance of the VO_2 in the capacitor structure is taken into account in the impedance transformations to obtain material properties as a function of temperature. The dielectric constant of VO_2 increases from a value of ~36 at room temperature to a value exceeding 6×10^4 at 100 °C. The carrier type of VO_2 thin film is electronic, determined by the polarity of the capacitance-voltage spectra. The electron carrier concentration of the VO_2 thin films shows about four orders of magnitude increase from room temperature to the temperature near phase transition. The approach of deriving insights into carrier conduction from capacitance measurement analyses can be applied to other materials beyond VO_2, wherein sensitive temperature-dependence or low carrier mobility makes Hall measurements challenging. Furthermore, the stack structure consisting of $HfO_2/VO_2/HfO_2/n$-Si shows a strong temperature dependence of capacitance due to the MIT in the sandwiched VO_2 layer. This suggests the potential for strongly correlated oxides that undergo a hysteretic MIT in thermally tunable capacitors that could be of interest for solid-state devices.

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I. INTRODUCTION

Vanadium dioxide (VO_2) is a material of great interest in condensed-matter physics and oxide electronics due to its metal-insulator transition (MIT) around 340 K.[1–9] VO_2 shows a sharp (several orders of magnitude) change in resistance along with a structural change from low-temperature monoclinic MoO_2 structure to high-temperature tetragonal rutile structure across the phase transition. There is a great deal of experimental and theoretical interest in understanding the elementary mechanisms (Mott vs Peierls) leading to the transition.[9,10] To advance our physical understanding of this material, knowledge pertaining to carrier transport is indispensible, to elucidate the possibility of correlation effects toward transition mechanism, as well as lead to a better understanding of electron transport in VO_2 material for future devices. Recently, it has been found that the MIT in VO_2 could be electrically triggered,[11–14] which may have potential applications to Mott field-effect transistor,[15,16] memristor,[17] oscillator,[18] optical switch,[19,20] active metamaterials,[8,21] and microwave switching.[22] The carrier concentration and dielectric constant in VO_2 as a function of temperature especially in the nominally insulating state are two fundamental parameters of importance. However, the most straightforward experimental method to investigate carrier property—Hall effect, is a challenge for VO_2, due to the low mobility and sensitive temperature dependence of the carrier concentration in VO_2. Although it has been over 50 years since the discovery of the MIT in VO_2,[1] only a handful of papers have addressed carrier concentration measurements in VO_2, particularly in thin-film structures.[23–25] In this paper, we present a detailed study on temperature-dependent carrier concentration, as well as dielectric constant measurements in thin-film VO_2, from quantitative analyses of temperature-dependent capacitance-voltage (C-V) data of a multilayer $HfO_2/VO_2/HfO_2/n$-Si thin-film stack capacitor. The results are of relevance to further advance understanding of the physical properties of this correlated oxide, and in broader context present approaches to study low-mobility oxide semiconductors taking into account their finite conductance. Further, studies on thin-film structures could potentially be of relevance to future devices that may exploit such phase transitions in correlated oxides.

II. EXPERIMENTS

The stack ($HfO_2/VO_2/HfO_2/n$-Si) capacitor device structure is shown in Fig. 1. First, a hafnium oxide (HfO_2) dielectric layer was grown on n-Si (1–10 Ω cm) substrate using a Cambridge NanoTech Savannah S200 atomic layer deposition (ALD) system. Water (H_2O) and tetrakis (dimethylamino) hafnium [$Hf(NMe_2)_4$] were used for oxygen and hafnium precursors, respectively. The growth temperature was 250 °C. Then, a VO_2 thin film was grown on top of the HfO_2-on-Si by radio frequency sputtering from a V_2O_5 target with 99.25 SCCM Ar plus 0.75 SCCM O_2 gas flow. The growth temperature, growth pressure, and target gun plasma power are 550 °C, 10 mTorr, and 80 W, respectively. Extensive experiments were carried out to optimize the VO_2 growth conditions on such underlayers and representative results are reported here. Finally, a second HfO_2 layer was grown on top of the VO_2 layer using ALD with the same recipe as the first HfO_2 layer. Au (200 nm)/Ti (20 nm) metals

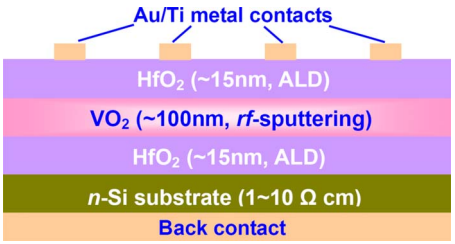

FIG. 1. (Color online) Schematic of $HfO_2/VO_2/HfO_2/Si$ stack structure capacitor device.

were deposited on top of the HfO_2 layer as top contacts for the capacitor device using a Sharon e-beam evaporator. The square-shape top metal contacts with a size of 300 $\times 300$ μm^2, defined with a shadow mask, were used for the electric characterizations of the device. Rapid thermal annealing was performed on the device at 200 °C for 30 s in N_2 ambient after metal deposition.

The current-voltage (*I-V*) and *C-V* characteristics were measured by a Keithley 236 Source Measure Unit and an Agilent 4284A Precision LCR Meter integrated in an MDC (Materials Development Corporation) system with a temperature controllable probe station. The temperature was read and calibrated with four thermocouples. The device was closely contacted on top the probe station stage using a vacuum pump and the metallic top surface of the probe station acts as the bottom contact of the capacitor device. X-ray photoelectron spectroscopy (XPS) was performed using Al $K\alpha$ of 1.4866 keV as x-ray source. Depth-dependent XPS study was conducted by Ar ion sputtering. Transmission electron microscopy (TEM) was carried out using a JEOL 2100 TEM system. Cross-sectional TEM specimens were prepared by mechanical thinning, polishing, and dimpling, followed by Ar ion milling in a Gatan Model 691 precision ion polishing system. First, the Ar ion milling was operated in the double gun mode at 5 kV with different gun tilting angles. Finally, gentle milling was performed using 2 kV Ar gas with 1° gun tiling angle. The film thicknesses were designed based on the precalibrated growth rates of the sputtering (for VO_2 layer) and ALD (for HfO_2 layers) systems, which have been double checked by cross-sectional TEM measurements. The thicknesses of bottom HfO_2, VO_2, and top HfO_2 layers are ~15 nm, ~100 nm, and ~15 nm, respectively. The size of the sample is 2.8×2.8 cm^2, i.e., the area of the bottom metallic contact. No evident elemental interdiffusion among layers was observed within the limits of energy-dispersive x-ray spectroscopy studies in the TEM.

III. RESULTS

First, we discuss the structural and compositional characterizations briefly for completeness sake. Figure 2(a) shows the cross-sectional TEM image of a capacitor device. Figure 2(b) shows a high-resolution TEM (HRTEM) image of the interface between the VO_2 and the bottom-HfO_2 layers, showing a clean interface. Figure 3(a) shows the XPS spectra taken from the top HfO_2 layer. Figure 3(b) shows the XPS

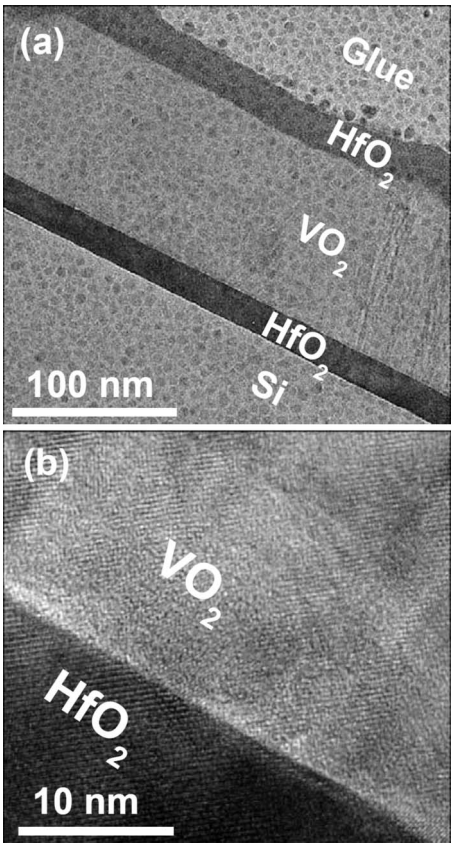

FIG. 2. (a) Cross-sectional TEM image of the capacitor device. (b) Cross-sectional HRTEM image of VO_2-HfO_2 interface region.

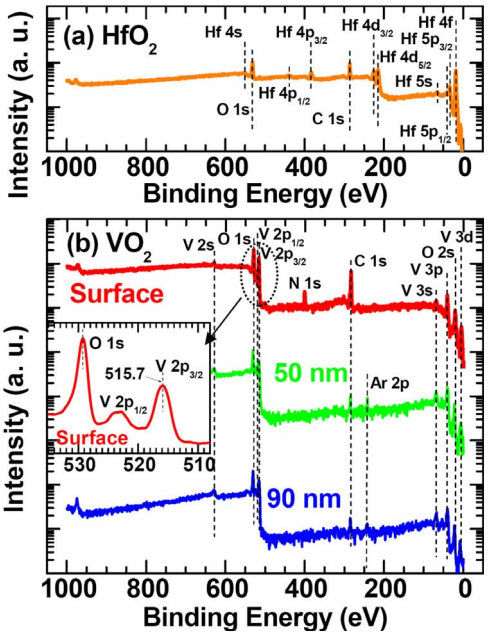

FIG. 3. (Color online) (a) XPS spectrum of HfO_2 thin-film surface. (b) XPS of at surface (red curve), 50 nm (green curve), and 90 nm (blue curve) depth from the surface of the VO_2 thin film. The inset shows the high-resolution XPS taken from VO_2 thin-film surface.

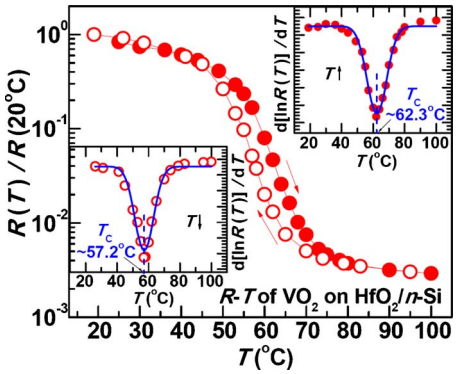

FIG. 4. (Color online) Temperature dependence of the normalized resistance of the VO_2 film sandwiched in the stacked device (measured before depositing the top HfO_2 layer). The MIT temperature T_C is determined to be ~62 and ~57 °C during temperature ramping up and ramping down, respectively, shown in the top and bottom insets.

spectra of the VO_2 layer from a dedicated reference sample prior to top HfO_2 layer deposition. The red, green, and blue curves show the XPS spectra of the VO_2 thin film at surface, 50 nm, and 90 nm deep from the surface of the VO_2 thin film (i.e., 50 and 90 nm VO_2 films were removed from the top surface using Ar ion sputtering.) The inset in Fig. 3(b) shows high-resolution XPS spectra of the VO_2 thin-film surface in the O 1*s* and V 2*p* region. The peak position of V $2p_{3/2}$ at 515.7 eV represents the valence of V is +4 (V $2p_{3/2}$ at 515.8 ± 0.2 eV for +4 valence),[26–32] indicating good stoichiometry of the VO_2 thin film. The extrinsic XPS peaks N 1*s*, C 1*s*, and Ar 2*p* arise from the sample surface contamination, the tapes used for sample mounting, and the Ar gas used as sputtering source during the in-depth profile XPS studies, respectively. It is observed that the N 1*s* peak disappears after the surface of the VO_2 film was sputtered away and Ar 2*p* peaks do not show up until the Ar gas sputtering source was introduced.

Figure 4 shows the temperature dependence of the normalized in-plane resistance $[R(T)/R(20\ ^\circ\mathrm{C})]$ of the VO_2 thin film sandwiched in the stack capacitor device. The measurement was done *prior* to top HfO_2 deposition. The resistance of the VO_2 thin film at each temperature point is determined based on the reciprocal slope of an *I-V* scan between two probes at different temperatures. Nearly three orders of magnitude of resistance change is observed from 20 to 100 °C, indicating good quality of the VO_2 film. Using standard Gaussian fitting on the derivative logarithmic plot,[33–35] the MIT temperature (T_C) of the VO_2 layer is determined to be ~62 °C and ~57 °C during temperature ramping up and ramping down, respectively, as shown in the top and bottom insets in Fig. 4.

Figure 5(a) shows the *I-V* characteristics of the device during heating with the temperature ramping up from 20 to 100 °C. At temperatures far below T_C, the conduction is dominated by the Poole-Frenkel (P-F) mechanism[13,36,37] indicated by an approximate linear plot of $\ln(I/V)$ versus $\sqrt{V}$. Figure 5(b) shows two representative plots corresponding

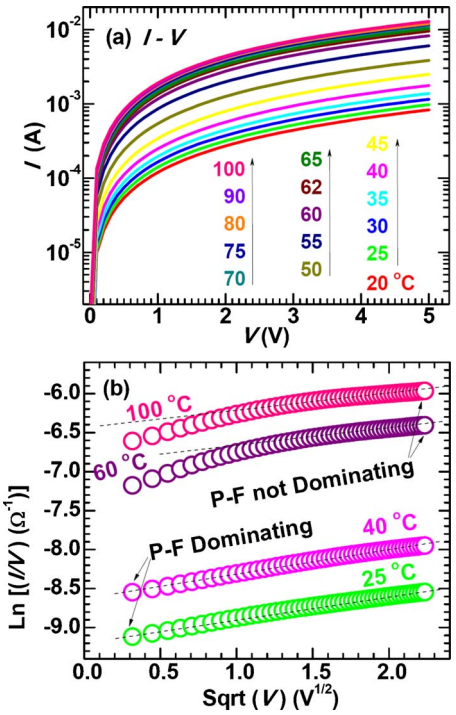

FIG. 5. (Color online) (a) *I-V* characteristics measured between top and bottom contacts during heating from 20 to 100 °C. (b) The plot of $\ln(I/V)$ versus $\sqrt{V}$ derived from the 25, 40, 60, and 100 °C *I-V* curves. The approximate linear relationship at 25 and 40 °C indicates Poole-Frenkel mechanism as dominant while the conduction mechanism at 60 and 100 °C are not dominated by the Poole-Frenkel mechanism due to the MIT in the VO_2 layer. The dashed lines are for visual guidance.

to 25 and 40 °C. However, when the temperature is approaching or above T_C, nonlinear dependence of $\ln(I/V)$ on $\sqrt{V}$ is observed, indicating the conduction is not purely from P-F mechanism. This is due to the proximity of the metallic state onset in VO_2 at elevated temperatures. Ohmic conduction onsets in the VO_2 layer,[13] hence, the overall conduction from top to bottom in the device is not purely attributed to a single mechanism. Two representative plots of 60 and 100 °C are shown in Fig. 5(b) to illustrate this.

Figures 6(a) and 6(b) show 1 MHz *C-V* characteristics of the capacitor device measured at varying temperatures from 20 to 100 °C, during temperature ramping up and down, respectively. Figures 6(c) and 6(d) show the same plots as (a) and (b) but only for high-temperature curves in a linear scale, to magnify the high-temperature range. The *C-V* curves look similar as expected for a metal-oxide-semiconductor (MOS) capacitor device with accumulation and inversion observed in positive and negative voltages. Figure 7 summarizes the temperature dependence of the capacitance measured from the $HfO_2/VO_2/HfO_2/Si$ stack device at 5 V (red circles), 0 V (green diamonds), and −5 V (blue hexagons). With increasing temperature, both the capacitance in accumulation and inversion regions increase. As shown with red circles in Fig. 7, the changes in the accumulation (+5 V bias) capaci-

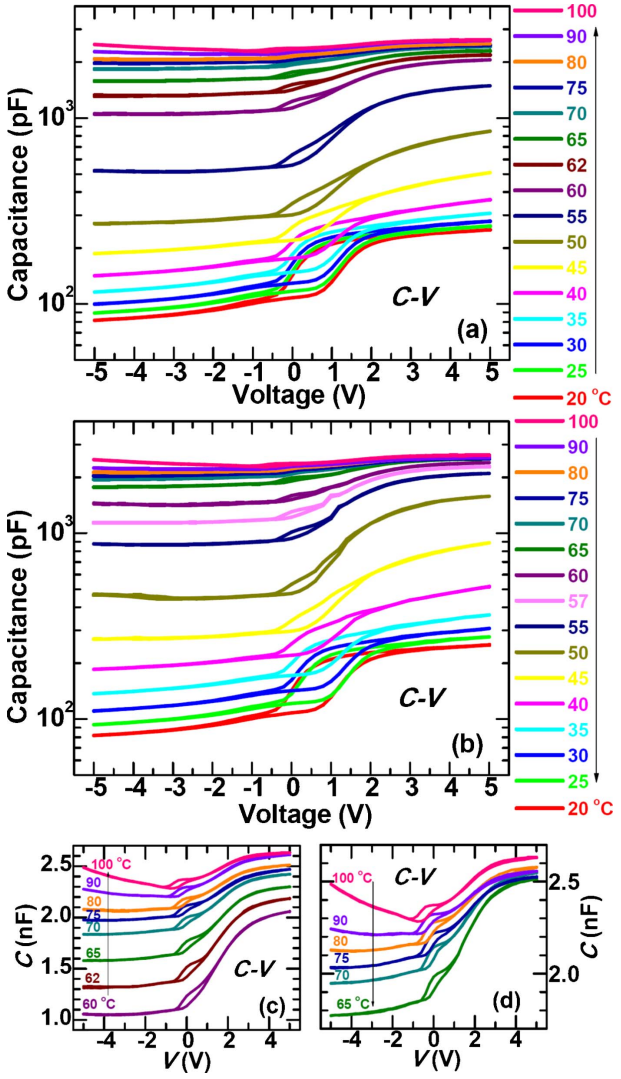

FIG. 6. (Color online) 1 MHz *C-V* characteristics of the $HfO_2/VO_2/HfO_2/Si$ stack device during temperature (a) ramping up and (b) ramping down. [(c) and (d)] The same plots as (a) and (b) but only for high-temperature curves in linear scale, to magnify the high-temperature range.

tance with temperature are hysteretic. The accumulation capacitance shows about one order of magnitude enhancement when temperature is increased from 20 to 100 °C (~251 pF at 20 °C vs ~2628 pF at 100 °C). The temperature dependence of the accumulation capacitance (at +5 V) of a reference metal/HfO_2/*n*-Si MOS capacitor device is shown as red circles in the inset of Fig. 7, which is nearly constant within the range of 20–100 °C. The HfO_2 dielectric layer with a thickness of ~40 nm in the reference sample was grown by ALD using an identical process as that in the $HfO_2/VO_2/HfO_2/Si$ capacitor. The reference capacitor device does not show any evident capacitance change with temperature, indicating that the strong temperature-dependent capacitance of the metal/$HfO_2/VO_2/HfO_2$/*n*-Si/metal capacitor device arises from the sandwiched VO_2 layer. This is to be expected due to the significant change in

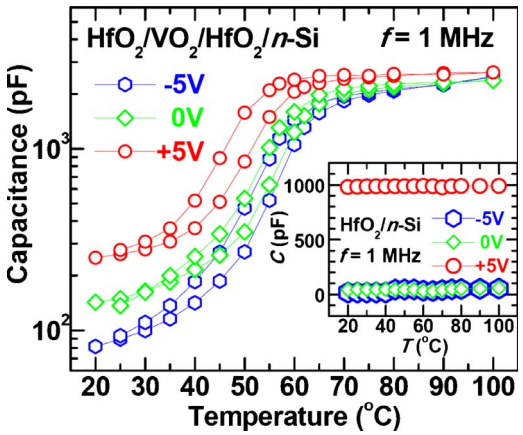

FIG. 7. (Color online) The temperature dependence of the capacitance measured from the $HfO_2/VO_2/HfO_2/Si$ stack device at 5 V (red circles), 0 V (green diamonds), and −5 V (blue hexagons). The inset shows the temperature dependence of the capacitance from the reference HfO_2 (40 nm)/Si MOS capacitor at 5 V (red circles), 0 V (green diamonds), and −5 V (blue hexagons). Capacitance hysteresis loops with about one order of magnitude capacitance change are observed in the $HfO_2/VO_2/HfO_2/Si$ stack device while the reference HfO_2/Si MOS capacitor shows nearly temperature-independent behavior.

the electrical properties of VO_2 with temperature. We should consider why the inversion (−5 V bias) capacitance also increases more than one order of magnitude, as shown in blue hexagons in Fig. 7, since in a typical inversion region at high frequencies, the MOS capacitor should be dominated by the depletion-layer capacitance from the silicon (fixed by the dopant concentration in the silicon). The likely reason is that the area of the capacitor of C_s in the reference HfO_2/*n*-Si MOS capacitor is several orders of magnitude smaller than that of the $HfO_2/VO_2/HfO_2$/*n*-Si capacitor C_{s1} because the VO_2 layer spreads the current, then in the $HfO_2/VO_2/HfO_2$/*n*-Si capacitor device the area of top oxide capacitor C_{ox} is defined as the top metal contacts area (300×300 μm^2) but the bottom oxide capacitor C_{ox1} and Si depletion layer capacitor C_{s1} are defined by bottom metal contact. So the inversion capacitance of the reference HfO_2/*n*-Si MOS capacitor is magnified significantly in the $HfO_2/VO_2/HfO_2$/*n*-Si capacitor. Further analysis of the data is presented below.

IV. ANALYSES AND DISCUSSION

A. Impedance transformation calculations

To quantitatively account for the finite conductance in the VO_2 layers, we first discuss the circuit diagram briefly. The equivalent circuit diagrams of the reference HfO_2/Si MOS capacitor and the $HfO_2/VO_2/HfO_2/Si$ stack capacitor are shown in Figs. 8(a) and 8(b). C_{ox0} in Fig. 8(a), C_{ox} and C_{ox1} in Fig. 8(b) are constant oxide capacitors from the HfO_2 layers with

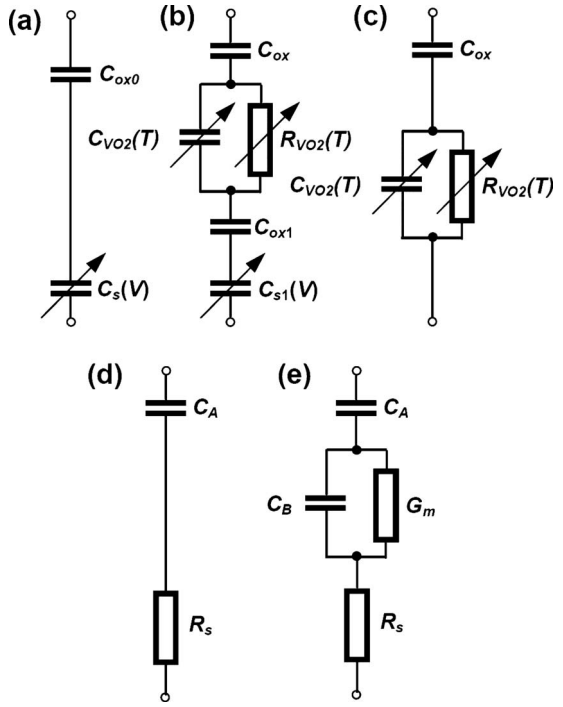

FIG. 8. (a) Equivalent circuit of the reference HfO_2/Si MOS capacitor device with two capacitors C_{ox0} and C_s in series. (b) Equivalent circuit of the $HfO_2/VO_2/HfO_2/Si$ stack device. C_{ox} and C_{ox1} are the capacitors of top and bottom HfO_2 layers and C_{s1} is the Si depletion-layer capacitor. The VO_2 layer acts as a capacitor $C_{VO_2}(T)$ in parallel with a resistor $R_{VO_2}(T)$, both of which are functions of temperature T. (c) Simplified equivalent circuit of the $HfO_2/VO_2/HfO_2/Si$ stack device. Capacitors C_{ox1} and C_{s1} are neglected comparing to (b), due to the orders of magnitude larger capacitor area. (d) Equivalent circuit of the MDC C-V meter during accumulation initialization test. (e) Equivalent circuit of the MDC C-V meter during regular measurements.

$$C_{ox} = \frac{A\varepsilon_{HfO_2}\varepsilon_0}{t_{ox}}, \tag{1}$$

where A is the area of the capacitor device, ε_{HfO_2} is the relative dielectric constant of HfO_2, ε_0 is the permittivity in vacuum, and t_{ox} is the thickness of the corresponding HfO_2 layer. C_s in Fig. 8(a) and C_{s1} in Fig. 8(b) are the Si depletion-layer capacitors, which are functions of applied voltages. The VO_2 layer is represented as a temperature-dependent capacitor $C_{VO_2}(T)$ in parallel with a temperature-dependent resistor $R_{VO_2}(T)$ in Fig. 8(b), which cannot be neglected due to the conductance of VO_2 especially at high temperatures. Due to spreading in the VO_2 layer as discussed before, the two bottom capacitors C_{ox1} and C_{s1} in Fig. 8(b) have much larger area than the top capacitors. In a series of capacitors, always the smaller capacitor dominates; hence the capacitors C_{ox1} and C_{s1} are neglected. Finally, the equivalent circuit diagrams of the $HfO_2/VO_2/HfO_2/Si$ stack capacitor device approximately simplified to Fig. 8(c) from Fig. 8(b). The impedance for the circuit diagram shown in Fig. 8(c) $\tilde{Z}_c$ is

$$\tilde{Z}_c = \frac{1}{j\omega C_{ox}} + \frac{1}{j\omega C_V + 1/R_V}, \tag{2}$$

where C_V and R_V represent for $C_{VO_2}(T)$ and $R_{VO_2}(T)$, respectively. Figures 8(d) and 8(e) show the equivalent circuits of the MDC C-V instrumentation at accumulation initialization test and during regular measurements, respectively. The two parameters C_A and R_S obtained in the accumulation initialization tests are introduced into the subsequent regular C-V measurements. The impedance $\tilde{Z}_d$ and $\tilde{Z}_e$ of the circuit diagrams shown in Fig. 8(d) and shown in Fig. 8(e) are,

$$\tilde{Z}_d = \frac{1}{j\omega C_A} + R_s \tag{3}$$

and

$$\tilde{Z}_e = \frac{1}{j\omega C_A} + \frac{1}{j\omega C_B + G_m} + R_s. \tag{4}$$

In order to retrieve the physical properties of the VO_2 thin film, we need to separate the VO_2 capacitance and resistance components, which are now coupled with each other in Fig. 8(c) during the C-V measurements. First, at +5 V bias (accumulation), we use the impedance transformation linked between Eqs. (2) and (3). Using $\tilde{Z}_c = \tilde{Z}_d$, we obtain,

$$R_V = R_s + \frac{1}{\omega^2 C_\Delta^2 R_s} \tag{5}$$

as the real part with $C_\Delta \equiv (\frac{1}{C_A} - \frac{1}{C_{ox}})^{-1}$ and the imaginary part as

$$C_V = \frac{C_\Delta}{1 + \omega^2 C_\Delta^2 R_s^2}. \tag{6}$$

Using Eq. (5) we can obtain the out-of-plane resistance of the VO_2 layer sandwiched in the stack capacitor. The temperature dependence of the resistance (normalized) in vertical direction of the VO_2 layer is shown in Fig. 9(a) as the blue curves. The directly measured in-plane normalized resistance of the VO_2 thin film (as shown in Fig. 4) is shown as red curves in Fig. 9(a) for comparison. The difference between the two temperature dependence trends are most likely due to the top HfO_2 layer induced stress onto the VO_2 thin film (i.e., with top HfO_2 layer in the C-V measurements but without top HfO_2 layer for the in-plane direct resistance measurements),[38] and also possibly from any conductivity anisotropy[39] of the VO_2 thin film in the device (i.e., perpendicular out-of-plane geometry vs horizontal in-plane geometry).

Using Eq. (6), the +5 V bias (accumulation) capacitance of VO_2 layer is derived. The red curves in Fig. 9(b) show the temperature dependence of the VO_2 +5 V bias capacitance. It shows strong temperature dependence, which is due to the significant change in the electrical properties of VO_2 with increasing temperature. With $\tilde{Z}_c = \tilde{Z}_e$, we obtain,

$$C_V = \frac{\dfrac{\omega^2 C_\Delta C_B + G_m^2 + \omega^2 C_B^2}{\omega C_\Delta [G_m + R_s G_m^2 + R_s \omega^2 C_B^2]}}{\omega \left[1 + \dfrac{(\omega^2 C_\Delta C_B + G_m^2 + \omega^2 C_B^2)^2}{\omega^2 C_\Delta^2 (G_m + R_s G_m^2 + R_s \omega^2 C_B^2)^2} \right] \left(\dfrac{G_m}{\omega^2 C_B^2 + G_m^2} + R_s \right)}. \quad (7)$$

Using Eq. (7), the −5 V bias (inversion) capacitance of VO_2 layer is derived. The blue curves in Fig. 9(b) show the temperature dependence of the VO_2 −5 V bias capacitance.

B. Dielectric constant

The relative dielectric constant of VO_2 thin film is derived from $\varepsilon_{VO_2} = \frac{C_{VO_2} t_{VO_2}}{A \varepsilon_0}$, where A is the area of the capacitor device, C_{VO_2} is the capacitance of VO_2 layer, ε_0 is the permittivity in vacuum, and t_{VO_2} is the thickness of the corresponding HfO_2 layer. The temperature dependence of the dielectric constant of VO_2 is shown in Fig. 10. The relative dielectric constant of VO_2 increases from ~36 at room temperature to $\sim 6.6 \times 10^4$ at 100 °C. This significant dielectric constant increase arises from the thermally induced phase transition. Literature values for VO_2 thin film[40] and bulk VO_2 crystals[41,42] are also shown together in Fig. 10 for comparison with Hood and Denatale in Ref. 40, Zylbersztejn *et al.* in Ref. 41, and Barker *et al.* in Ref. 42. The inset shows a magnified view of the near room-temperature region. Our results and trends are consistent with reported values indicating validity of our methodology described above as well as quality of the thin-film samples with reference to prior bulk single-crystal dielectric measurements. We also note that the sharp change in dielectric constant due to the phase transition and the resulting thermally tunable capacitor presents an interesting result in itself with potential for novel devices.

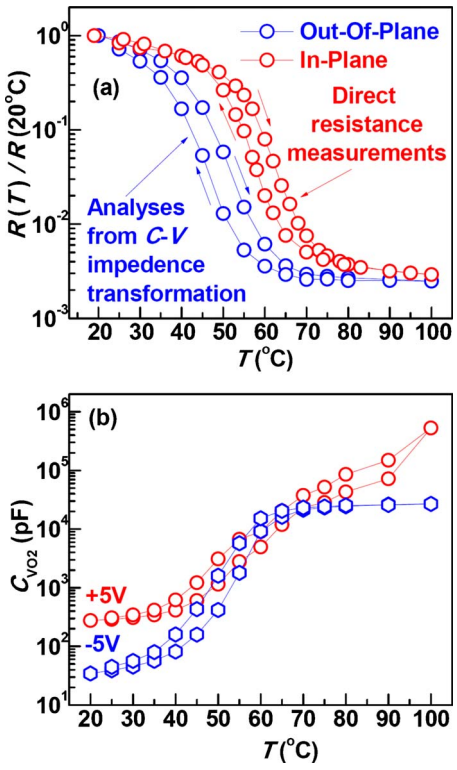

FIG. 9. (Color online) (a) The blue curves show the temperature dependence of the normalized VO_2 resistance [R_{VO_2} as shown in the equivalent circuit in Fig. 8(c)] derived from impedance transformation calculations using Eq. (5). The red curves show the temperature dependence of the normalized resistance of the VO_2 film measured directly using *I-V* meter (exactly same as Fig. 4, shown here again for comparison). Both curves are normalized by the resistance value at 20 °C. (b) The temperature dependence of the accumulation (+5 V bias, red circles) and inversion (−5 V bias, blue hexagons) capacitances [C_{VO_2} as shown in the equivalent circuit in Fig. 8(c)] of the VO_2 layer derived from the impedance transformation using Eqs. (6) and (7).

C. Carrier conduction properties

The carrier type in this VO_2 thin film is determined to be electronic, due to the occurrence of inversion at negative voltage region while accumulation is seen in positive gate voltage regime. This is in agreement with Hall measurements as well as photoemission spectroscopy.[42,43] The carrier concentration of the VO_2 thin film is analyzed from the inversion capacitance equation as

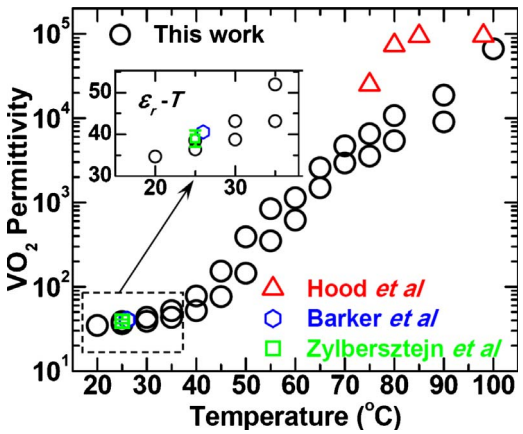

FIG. 10. (Color online) The temperature dependence of the relative dielectric constant of the VO_2 thin film derived from the temperature dependence of the accumulation (+5 V bias) capacitance of the VO_2 layer [red circles in Fig. 9(b) in the paper]. Literature values were also shown together for comparison with Hood and Denatale in Ref. 40, Zylbersztejn *et al.* in Ref. 41, and Barker *et al.* in Ref. 42. The inset shows the magnified near room-temperature region.

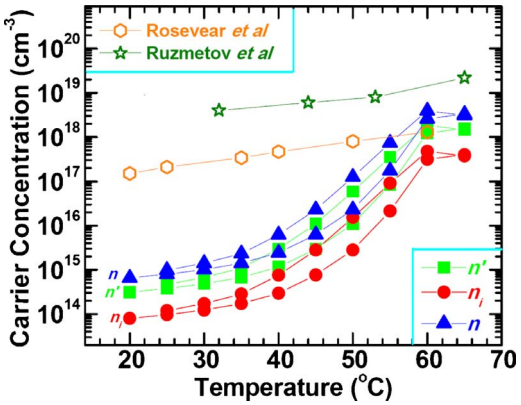

FIG. 11. (Color online) The temperature dependence of the carrier concentration of the VO_2 thin film. The green squares, red circles, and blue triangles show the values of effective carrier concentration n', intrinsic carrier concentration n_i, and real electron carrier concentration n, respectively. Literature reported values are also shown together for comparison with Ruzmetov *et al.* in Ref. 25 and Rosevear and Paul in Ref. 44.

$$C_V(\text{inversion}) = \frac{Ae}{2}\sqrt{\frac{\varepsilon_{VO_2}\varepsilon_0 n}{k_B T \ln(n/n_i)}}, \tag{8}$$

where A is the capacitor device area, e is the electron charge, ε_{VO_2} is the relative dielectric constant of VO_2, ε_0 is the permittivity in vacuum, k_B is Boltzmann constant, T is the temperature, n is the carrier concentration of VO_2, and n_i is "intrinsic" carrier concentration of VO_2. Equation (8) is a transcendental function, for convenience, we introduce "effective" carrier concentration n' here, as

$$n' \equiv \frac{n}{\ln(n/n_i)} = \frac{4k_B T}{A^2 e^2}\frac{1}{\varepsilon_{VO_2}\varepsilon_0} C_V^2(\text{inversion}). \tag{9}$$

Using Eq. (9), we obtain n' as shown with the green squares in Fig. 11. The temperature dependence of n' approximately represents the trend of n. More precisely, we need to solve the transcendental equation $\frac{n}{\ln(n/n_i)} = n'$. Although we could not find reported values of n_i in VO_2 from literature (unlike well-studied semiconductor materials such as Si and GaAs), n_i of VO_2 at room temperature can be approximately estimated[45] as $\sim 8.0 \times 10^{13}$ cm^{-3} from the physical parameters (e.g., band gap, effective mass, and density of states) reported for bulk crystal form of VO_2 in earlier studies.[2–7] n_i is likely strongly dependent on temperature due to the phase transition, unlike conventional semiconductors (n_i shows weakly temperature dependence). In order to solve the above transcendental equation, we make an approximation here, assuming that the n_i and n follows the same temperature dependence. This approximation is perhaps reasonable because the temperature dependence of both n_i and n are roughly an exponential function of VO_2 band gap over temperature. The blue triangles and red circles in Fig. 11 show the values of electron carrier concentration n and intrinsic carrier concentration n_i, respectively. It is observed that n is larger than n_i, which has been observed in oxide semiconductors[46] due to the strong dependence of n over stoichiometry. The electron concentration n of the VO_2 thin films increases about four orders of magnitude from room temperature to the temperature region approaching MIT T_C. Literature values for the carrier concentration are also shown together for comparison, with Ruzmetov *et al.* in Ref. 25 and Rosevear and Paul in Ref. 44.[47] The results show consistent trends with carrier concentration data from limited Hall measurements found in literature. The difference among the reported values and ours are likely due to different VO_2 material preparation methods (phase transition properties of VO_2 are known to be rather sensitive to the synthesis procedure and the insulating state resistivity can be tuned over a broad range)[33–35,48–52] and carrier concentration measurement approaches involved in these different techniques.

V. SUMMARY

In summary, $HfO_2/VO_2/HfO_2/n$-Si stack capacitor devices have been fabricated, characterized, and studied. The capacitance shows strong temperature dependence due to MIT in the sandwiched VO_2 layer and is hysteretic. From impedance transformation, the capacitance of the VO_2 layer in accumulation and inversion are extracted from 20 to 100 °C. The relative dielectric constants of the VO_2 thin films at different temperatures are derived from the VO_2 accumulation capacitance with a value of ~36 at room temperature and a value exceeding 6×10^4 at 100 °C, in agreement with previous reports. The electron carrier concentration of the VO_2 thin films is derived from the VO_2 inversion capacitance, which shows about four orders of magnitude increase from room temperature to the temperature approaching the MIT. We anticipate the results and approaches presented here to be of relevance to advancing physical insights into properties of VO_2 thin films and possibly their explorations in electronics.

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[45] The intrinsic carrier concentration n_i in VO_2 is approximately estimated as

$$n_i = 2\left(\frac{2\pi k_B T}{h^2}\right)^{3/2}(m_n m_p)^{3/4}\exp\left(-\frac{E_g}{2k_B T}\right)$$

$$= \left\{2.5\times 10^{19}(\sqrt{\alpha}m_n^*)^{3/4}\left(\frac{T(\mathrm{K})}{300}\right)^{3/2} \times\exp\left(-\frac{E_g(\mathrm{eV})}{0.0518}\frac{300}{T(\mathrm{K})}\right)\right\}\ (\mathrm{cm}^{-3})$$

with $m_n^* \sim 1.6$ (Refs. 2 and 5), $E_g \sim 0.7$ eV (Refs. 2–4). Although this assumption is approximate, it gives a rough idea of how the real carrier concentration n is solved from the transcendental equation [Eq. (9)]. From the results, we can observe that the effective carrier concentration n' approximately represents n, by comparing the green squares to blue triangles in Fig. 11.

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