Electrical Properties and Anisotropy in Amorphous Si and $Si_{0.5}Ge_{0.5}$ Alloy

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The electrical conductivity of amorphous Si films ranging in thickness between 610 Å and 2.2 μm was measured both in the plane and in the transverse directions. A similar although briefer study was performed on amorphous $Si_{0.5}Ge_{0.5}$ films. The films were deposited at 300 and 77 °K by the getter-sputtering technique. The major portion of the study was conducted on films deposited and kept at 77 °K: There are marked differences in electrical properties between films deposited at 300 °K and films deposited and kept at 77 °K, which were related to the structure of the films. While a marked anisotropy in both the resistivity and its temperature dependence was previously reported for Ge, one only notices an anisotropy in the temperature dependence with Si films below 2500 Å; this anisotropy increases with decreasing film thickness down to the thinnest film studied (610 Å). In general, one can state that the electrical properties of $Si_{0.5}Ge_{0.5}$ are intermediate between those of Si and Ge and that the anisotropy, if present at all, is very small and develops below 1200 Å.

I. INTRODUCTION

Recently, an anisotropy was reported[1] in the electrical conduction of amorphous Ge. Furthermore, there was also a marked difference in electrical properties between films deposted at 300 °K and films deposited and kept at 77 °K. This difference as well as the annealing behavior of films deposited at 77 °K was interpreted[1,2] in terms of the structure of the films. From the structural point of view, the cracks suggested by Galeener[3,4] in amorphous Ge on the basis of optical measurements have been observed[2] by high-resolution electron micrographs by Donovan and Heinemann.[5] Cargill[6] using small-angle x-ray scattering reported rodlike low-density regions in a 7-μm-thick film. On the other hand, the structural situation is not as clear in amorphous Si. Moss and Graczyk,[7] using electron diffraction, found that the density deficit in amorphous Si was associated with submicroscopic voids. Additional evidence for the voids was provided by ESR studies by Brodsky *et al.*[8] but contrary to the Ge case, the voids in Si were never directly observed. As the size and shape of the voids may affect the electrical conduction and its anisotropy,[1,2] it would be interesting to find out whether or not Si has the same defect structure as Ge and to compare the resulting anisotropy (if any) with that of Ge. Furthermore, little work has been reported on the electrical conduction of amorphous Si. Walley[9] and Morgan and Walley[10] reported that the resistivity of amorphous Si was well fitted between 300 and 60 °K by the relation,[11,12]

$$\rho = \rho_0 e^{(T_0/T)^{1/4}}, \tag{1}$$

where T_0, which is given by $16\alpha^3/kN(E_F)$, was equal to 6.1×10^7 °K; α is the coefficient of exponential decay of localized states, $N(E_F)$ is the density of localized states at the Fermi level, and k is Boltzmann's constant. The prefactor ρ_0 was shown by Mott[11] to be equal to $[T\alpha/N(E_F)]^{1/2}$. Equation (1) is only applicable to the temperature range in which conduction is dominated by phonon-assisted tunneling between localized states near E_F. However, quite recently Pollak *et al.*[13] have shown that Eq. (1) is applicable to much higher temperatures than was previously realized thus explaining why the experimental fit[9,10] seems to hold up to room temperature. Brodsky and Gambino[14] reported the same fit between 300 and 100 °K with $T_0 = 3.1\times10^7$ °K, but pointed out that while T_0 could be explained with reasonable physical parameters, ρ_0 could not. They further showed[14] that the changes with annealing in ρ_0 and T_0 were inconsistent. T_0 generally increased (in good agreement with the anneal of amorphous Ge films deposited at 77 °K[1,2]), indicating a lower density of states $N(E_F)$; but ρ_0 occasionally decreased indicating a higher $N(E_F)$. Consequently, it would be interesting to study the conduction in Si films deposited at 300 and 77 °K as well as their annealing behavior and anisotropy. The study of amorphous Ge films and amorphous Si films can be best linked together by the study of Si-Ge alloys.

II. EXPERIMENTAL PROCEDURE

The films were deposited on sapphire and glass substrates by getter-sputtering[15] from Si and $Si_{0.5}GE_{0.5}$ targets. The Si target was ground from a 1.25-in. -diam, cylindrical high-purity single crystal with a resistivity of 50 Ω cm. The $Si_{0.5}Ge_{0.5}$ target was prepared by inductively melting[16] a mixture of high-purity Si and Ge. The composition of the target was checked by x-ray fluorescence analysis. The rates of deposition varied between 0.2 and 2 Å/sec. The film thickness was

determined by weighing thick films and using a density of 2.05 g cm^{-3}, which seems to be the most representative value for amorphous Si films as reported by Mogab.[17] This corresponds to a density 12% lower than the crystalline value in agreement with other studies.[7] These thickness measurements agreed with direct angstrometer measurements performed on thinner films. The experimental technique used in the electrical measurements is identical to the one used for the amorphous Ge films which has already been described.[1,2] For both planar and transverse measurements, films deposited at 77 °K were transferred onto a holder without warming and the resistivity was measured at first by cooling down to 20 °K and then by warming above 77 °K to study the annealing behavior of the films. The electron micrographs were obtained[18] by depositing 100-Å films on cleaved NaCl substrates at room temperature. The films were floated free and mounted on a perforated carbon substrate and examined by high-resolution electron microscopy (magnification 250 000) with an underfocusing of about 3000 Å.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. Si Films

Before discussing the electrical properties of the amorphous Si films, there is an interesting point that one can make about the conditions under which the films were prepared. Walley,[9] who studied the variation of resistivity with residual gas pressure and rate of deposition for both Ge and Si, showed that the resistivity starts to increase (and very rapidly for Si) when the rate of deposition falls below 30 Å/sec for a residual-gas pressure of about 10^{-5} Torr. This threshold corresponds to the point where the deposition rate of gas atoms is comparable with that of metal atoms. The fact that Si films getter-sputtered at 300 °K show a constant resistivity of a few hundred Ω cm independent of the rate of deposition between 0.2 and 2 Å/sec, is proof once again that getter-sputtering leads to a very low concentration of reactive gases[15] such as O_2 and N_2 ($< 6\times 10^{-8}$ for the present experiments).

The electron micrograph of Fig. 1(a) taken on a 100-Å Si film shows that the defect structure of amorphous Si films is very similar to the one reported for amorphous Ge films.[2,5] Once again we see ≃ 40 Å dark areas surrounded by a network of cracks. The scale of the defect structure is similar to that of Ge-sputtered films[1] but is smaller than that of evaporated Ge films.[5] Consequently, if this defect structure had any influence on the electrical properties (the contrary was argued in the case of Ge films,[2] except possibly for ultrathin films), we would expect the electrical conductivity and its anisotropy to be similar for amorphous Ge and Si.

Let us therefore turn our attention to the electrical properties of amorphous Si. The temperature dependence of the planar resistance of the film for films deposited at room temperature is shown in Fig. 2. The data are well fitted by relation (1) with $T_0 \simeq 8\times 10^7$ °K and a room-temperature resistivity ρ_{RT} on the order of a few hundred Ω cm (see Table I where the properties of all Si films are summarized); this is to be compared with films evaporated at 300 °K, which yield $T_0 = 6.1 \times 10^7$ °K and $\rho_{RT} = 46$ Ω cm[9,10] or $T_0 = 3.5\times 10^7$ °K and $\rho_{RT} = 15$ Ω cm.[19] As the electron micrograph [Fig. 1(a)] shows that the sputtered films have a

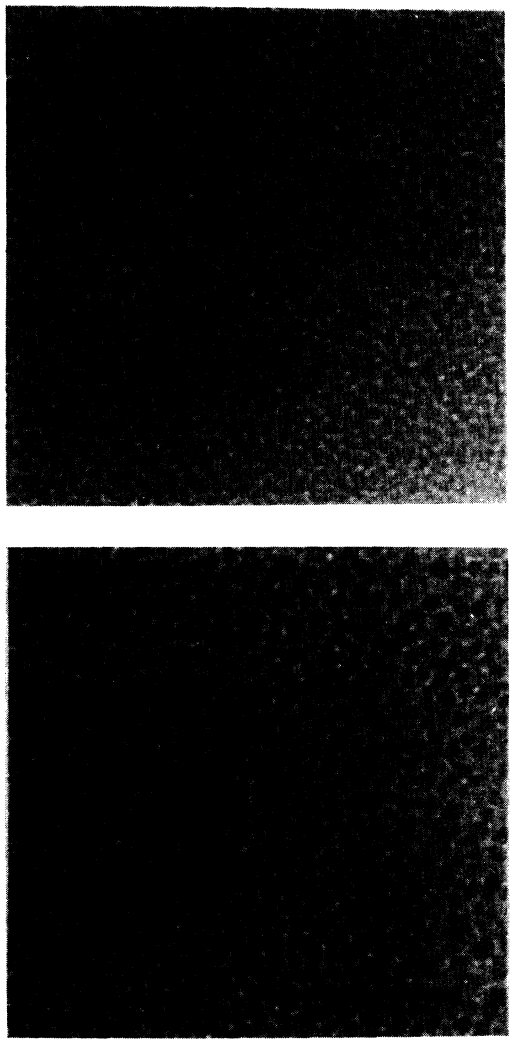

FIG. 1. Bright-field electron micrographs of (a) a 100-Å Si film and (b) a 100-Å $Si_{0.5}Ge_{0.5}$ film deposited at room temperature on NaCl showing dark film areas ≃ 40 Å surrounded by a network of cracks.

fine defect structure, one could assume as in the case of Ge[1] that the higher resistivity of sputtered films may be the result of the higher density of cracks. Furthermore, the higher density of cracks may occur at the expense of the number of localized states, thus increasing T_0. The temperature dependence of the planar resistance for films deposited and kept at 77 °K is shown in Fig. 3. Below 120 °K the data can be fitted very well again by relation (1) but with a lower value of $T_0 \simeq 5\times 10^7$ °K (leaving aside Si No. 6 which, as shown in Table I, also displays an anomalously low prefactor ρ_0). Just as in the Ge case,[1] this lower T_0 value can be ascribed to the higher density of localized states resulting from the more disordered structure following the low-temperature deposition. The films anneal around 120 °K as shown by the deviation from the low-temperature data towards higher resistance. If one extrapolates the low-temperature data to room temperature, one obtains a $\rho_{\text{extr RT}}$ on the order of a few Ω cm, which is lower than the value for room-temperature-deposited films. After annealing, it is clear from Table I that the films regain the values of the parameters characteristic of a room-temperature-deposited film ($T_0 \simeq 10^8$ °K and ρ_{RT} on the order of a few hundred Ω cm). The increase in resistivity taking place upon annealing can be mostly explained by the increase in T_0 leaving ρ_0 approximately constant. Indeed, as shown by Table I, while T_0 increases upon annealing for Si Nos. 3 and 4, Pb-Si-Pb No. 3, and Pb-Si-Pb No. 9 (to 300 °K), ρ_0 increases only for Si No. 3 and Pb-Si-Pb No. 3. This is the same inconsistency previously reported by Brodsky and Gambino.[14] Although this may indicate either that the $T^{-1/4}$ law is an artifact and phonon-assisted tunneling does not predominate or that Mott's calculation of ρ_0 is incorrect. I would rather suggest that ρ_0 reflects certain structural defects of the film (such as cracks) which may have erratic and unpredictable effects on ρ_0 upon annealing. As films deposited and kept at 77 °K are most probably crackfree[1,2] and as the cracks are present upon annealing to room temperature, the results of annealing on the electrical properties would tend to suggest that cracks have little if any effect on the electrical properties except possibly in very thin films. The cracks may contribute at most an isotropic term to the prefactor ρ_0.

TABLE I. Properties of Si films.

Film	d_{Si}(Å)	T_D(°K)[a]	ρ_{RT}(Ω cm)[b]	T_0(°K)	ρ_0(Ω cm)
Si No. 1	13600	300	735	8×10^7	9.9×10^{-8}
Si No. 2	21600	300	390	8.8×10^7	3×10^{-8}
Si No. 3	5540	77	8.3	4.7×10^7	1.9×10^{-8}
Si No. 3 annealed 16 h[c]			637	9.6×10^7	3×10^{-8}
Si No. 4	345	77	10.3	6×10^7	6.7×10^{-9}
Si No. 4 annealed 16 h			690	1.3×10^8	5×10^{-9}
Si No. 5.	11000	77	5.9	4.5×10^7	1.7×10^{-8}
Si No. 6	1000		3.3	8.7×10^7	2.8×10^{-10}
Si No. 6 annealed to 300 °K			325	...	...
Pb-Si-Pb No. 3	3000	77	6	5.2×10^7	8.2×10^{-9}
Pb-Si-Pb No. 3 annealed 16 h			1120	5.8×10^7	8.8×10^{-7}
Pb-Si-Pb No. 4	610	77	7.1	3.1×10^7	5.2×10^{-8}
Pb-Si-Pb No. 4 annealed 16 h			7000	3×10^7	1.3×10^{-6}
Pb-Si-Pb No. 5	670	77	6.4	3.7×10^7	4.6×10^{-8}
Pb-Si-Pb No. 66	1700	77	8.5	3.3×10^7	1×10^{-7}
Pb-Si-Pb No. 8	2300	77	7	4.1×10^7	3×10^{-8}
Pb-Si-Pb No. 9	4750	77	6	4.6×10^7	1.5×10^{-8}
Pb-Si-Pb No. 9 annealed to 300 °K			34	7.2×10^7	8.3×10^{-9}
Pb-Si-Pb No. 9 annealed 64 h			250	5.4×10^7	2.8×10^{-7}
Morgan and Walley[d]				6.1×10^7	6×10^{-8}

[a] T_D is the temperature of deposition of the film.

[b] This is the room-temperature resistivity for a film deposited or annealed at 300 °K; it is $\rho_{\text{extr RT}}$ for films deposited at 77 °K (see text).

[c] The anneal unless otherwise indicated was performed at 300 °K.

[d] References 9 and 10.

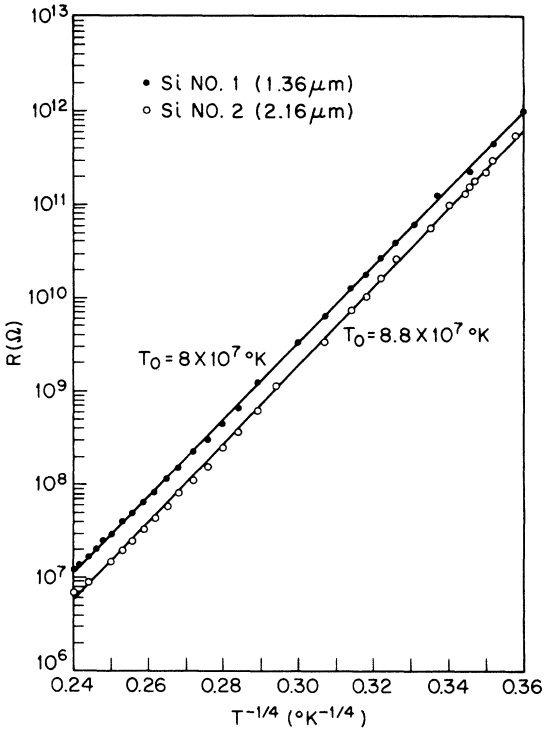

FIG. 2. Temperature dependence of the planar resistance for Si films deposited at room temperature.

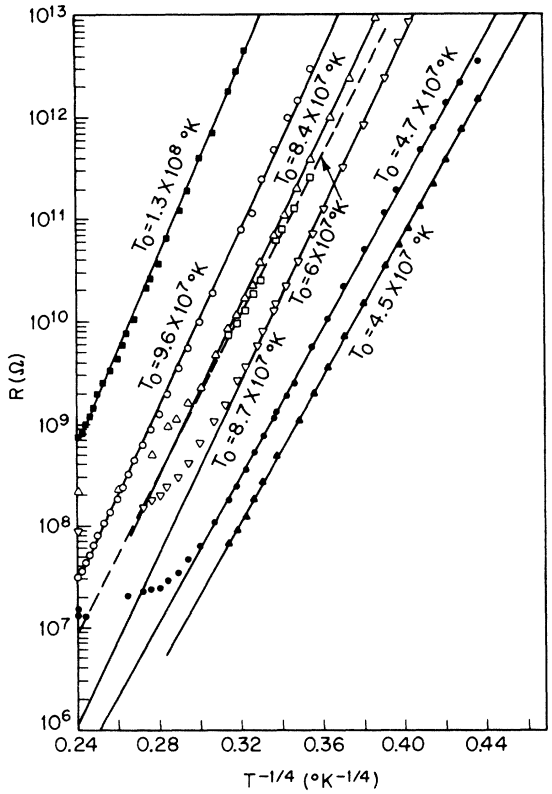

FIG. 3. Temperature dependence of the planar resistance for Si films deposited at 77 °K showing the effect of room-temperature annealing. Si No. 3, 5540 Å (●) as deposited, (○) annealed 16 h; Si No. 4, 345 Å (□) as deposited, (△) warmed up to 103 °K, (■) annealed 16 h; Si No. 5, 1.1 μm, (▲); Si No. 6, 1000 Å (▽).

The temperature dependence of the resistance for very thin films is shown in Fig. 4. While in Ge we found[2] that T_0 increased as $d^{-1/2}$, and Knotek *et al.*[20] reported an increase proportional to d^{-1} (where d is the film thickness) for films thinner than 300 Å, it is clear that no such simple law is apparent in Fig. 3. Hamilton[21] and Shante[22] have recently considered the planar electrical conduction in very thin films, and based on the fact that the electron hopping distance increases with decreasing temperature, they concluded that in very thin films at low temperatures the conduction will change from a three-dimensional to a two-dimensional behavior when the electron hopping distance becomes comparable with the film thickness. In the two-dimensional regime they[21,22] predict that the exponent 4 in relation (1) changes to 3 and that T_0 is inversely proportional to the film thickness. It is apparent from Fig. 4 that the data are well fitted by relation (1) with the exponent 4 replaced by 3. This is, however, no proof for the validity of the theory as the same is true for 5540-Å-thick film which is too thick for the theory to apply. Consequently, the fact that Si No. 3 can be fitted with exponent 4 (Fig. 3) and exponent 3 (Fig. 4) simply demonstrates that one cannot distinguish between these two exponents in this temperature range. Furthermore, Fig. 4 indicates that T_0 increases as the film thickness decreases from 5000 to 1000 Å and remains approximately constant as the film thickness is further decreased to 150 Å. This behavior cannot possibly be explained by the above theory and must be the result of some structural change occurring in that film thickness range. Furthermore, the increase in T_0 for the 100-Å film is certainly the result of a structural change as the resistance of that film shows a discontinuous increase with respect to the thicker films. Consequently, the fact that in contradistinction with Ge one does not observe a two-dimensional behavior may simply result from the fact that the parameters for Si are such that the effect would occur below 150 Å, and at this point, it becomes entangled with the structural effects.

The temperature dependence of the transverse resistance as a function of temperature for films deposited and kept at 77 °K is shown in Fig. 5. We shall first discuss the data below the annealing

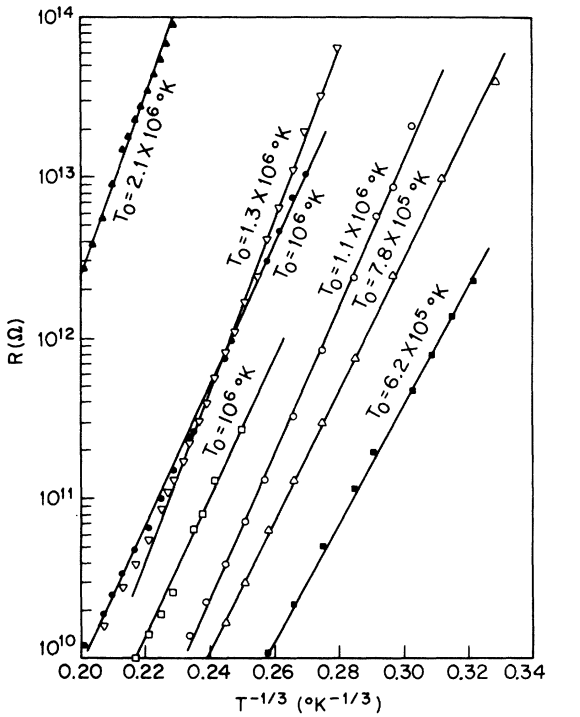

FIG. 4. Temperature dependence of the planar resistance for thin films deposited at 77 °K. Si No. 10, 100 Å (▲); Si No. 11, 150 Å (▽); Si No. 8, 200 Å (●); Si No. 4, 345 Å (□); Si No. 6, 1000 Å (○); Si No. 9, 1630 Å (△); Si No. 3, 5540 Å (■).

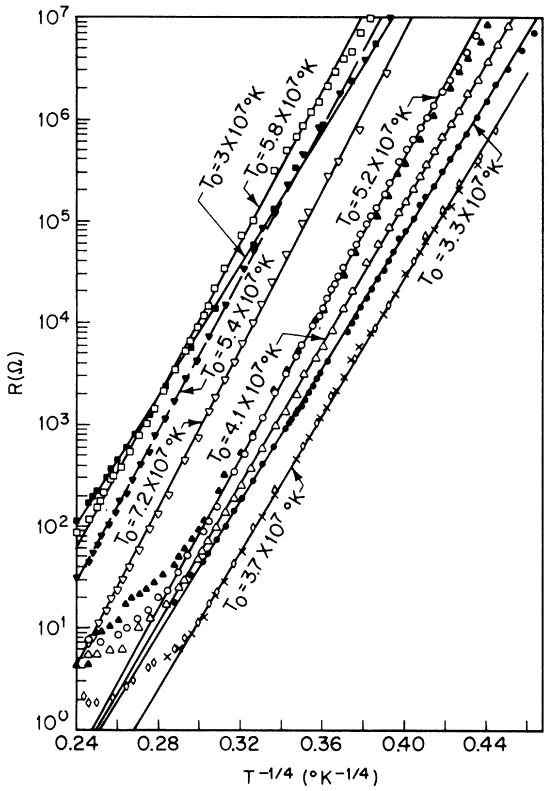

FIG. 5. Temperature dependence of the transverse resistance for films deposited at 77 °K showing the effect of room-temperature annealing. Pb-Si-Pb No. 9, 4750 Å (▲) as deposited, (▽) annealed to 300 °K, (▼) annealed 64 h; Pb-Si-Pb No. 3, 3000 Å (●) as deposited, (□) annealed 16 h; Pb-Si-Pb No. 8, 2300 Å, (△); Pb-Si-Pb No. 6, 1700 Å (•); Pb-Si-Pb No. 5, 670 Å (◇); Pb-Si-Pb No. 4, 610 Å (×) as deposited, (■) annealed 16 h.

temperature which is approximately 120 °K. It is clear from both Fig. 5 and Table I that as the film thickness is reduced below 3000 Å down to 610 Å that T_0 decreases from 5 to 3×10^7 °K. Consequently, films 2300 Å and thinner display a transverse value of T_0 which is lower than the planar value (5×10^7 °K) and therefore similar to Ge [1,2] there is an anisotropy in the value of T_0. On the other hand, the transverse values of the $\rho_{\text{extr RT}}$ are of the order of a few Ω cm even for the thinnest film measured (610 Å) which is approximately the same as the planar values (Table I). This empirically means that the decrease in T_0 is compensated by an increase in ρ_0, thus leaving $\rho_{\text{extr RT}}$ essentially unchanged. This is quite different from the anisotropy in Ge [1,2] which started at about 4000 Å and resulted in lower transverse values for both T_0 and $\rho_{\text{extr RT}}$. Consequently, although the crack network is quite similar in Si and Ge as shown by Fig. 1(a), the anisotropy is quite different, which suggests again that the cracks seen in electron transmission micrographs do not play an important role in the electrical conductivity. On the other hand, it would seem that larger density deficient volumes of the type proposed by Cargill[8] may be responsible for the anisotropy. The present results would indicate that these regions are smaller in Si than in Ge or possibly that their shapes and directions are different in the two cases.

Let us now turn our attention to the result of annealing in the transverse resistance measurements. Just as in the planar measurements, above 120 °K the resistance increases as shown by the deviation from the low-temperature data. However, while in the planar Si resistance measurements and in both planar and transverse Ge resistance measurements,[1,2] T_0 increased upon annealing to a value close to the room-temperature value, one can judge from Table I that in the case of Pb-Si-Pb No. 4 the value of T_0 actually decreases upon annealing. This strange result is, as we shall demonstrate, the result of diffusion of Pb into Si as a result of annealing. If such is the case, one expects the effect to be greatest in the

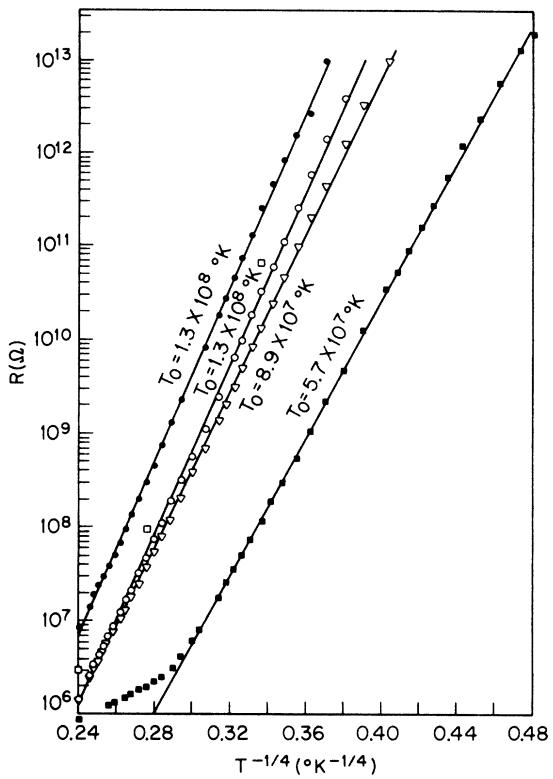

FIG. 6. Temperature dependence of the planar resistance for $Si_{0.5}Ge_{0.5}$ films deposited at 300 and 77 °K. $Si_{0.5}Ge_{0.5}$, No. 1, 1.95 μm (•); $Si_{0.5}Ge_{0.5}$, No. 3, 3.8 μm (□); $Si_{0.5}Ge_{0.5}$, No. 2, 7.9 μm (○). All three previously listed films were deposited at 300 °K. $Si_{0.5}$ $Ge_{0.5}$, No. 4, 1.4 μm (■) as deposited at 77 °K, (▽) annealed 2 h at 300 °K.

TABLE II. Properties of $Si_{0.5}Ge_{0.5}$ films.

Film	$d_{Si_{0.5}Ge_{0.5}}$	T_D(°K)[a]	ρ_{RT}(Ω cm)[b]	T_0(°K)	ρ_0(Ω cm)
$Si_{0.5}Ge_{0.5}$ No. 1	19 500	300	710	1.3×10^{8}	5.1×10^{-9}
$Si_{0.5}Ge_{0.5}$ No. 3	38 000	300	515	1.3×10^{8}	3.7×10^{-9}
$Si_{0.5}Ge_{0.5}$ No. 2	79 000	300	570	1.3×10^{8}	4.1×10^{-9}
$Si_{0.5}Ge_{0.5}$ No. 4	14 000	77	2	5.7×10^{7}	1.7×10^{-9}
$Si_{0.5}Ge_{0.5}$ No. 4 annealed 2 h[c]			93	8.9×10^{7}	6.8×10^{-9}
Pb-$Si_{0.5}Ge_{0.5}$-Pb No. 1	1 500	77	3.6	5.5×10^{7}	3.7×10^{-9}
Pb-$Si_{0.5}Ge_{0.5}$-Pb No. 2	1 200	77	2	4.7×10^{7}	4.6×10^{-9}

[a] T_D is the temperature of deposition of the film.
[b] This is the room-temperature ressitivity for a film deposited or annealed at 300 °K; it is $\rho_{extr\,RT}$ for films deposited at 77 °K (see text).
[c] The anneal unless otherwise indicated was performed at 300 °K.

thinnest films; this is supported by the annealing of Pb-Si-Pb No. 3 which is made up of a 3000-Å Si film and shows a slight increase in T_0. T_0 increases from 5.2 to 5.8×10^{7} °K which is still lower than the room temperature value, although no anisotropy should be present, as shown above, at this film thickness. The presence of diffusion is better demonstrated by the annealing experiment on Pb-Si-Pb No. 9. After warming up to 300 °K, as the film is thick enough (4750 Å) to avoid appreciable diffusion, T_0 increases from 4.6 to 7.2×10^{7} °K which is almost the room-temperature value. However, after a long anneal at room temperature which results in appreciable Pb diffusion, T_0 decreases to 5.4×10^{7} (Table I). The decrease in T_0 following diffusion is the result of an increase in the number of localized states represented by Pb impurities. Anyhow, the transverse resistance measurements cannot be trusted for annealed sandwiches, and firm conclusions can only be drawn for sandwiches made and kept at 77 °K.

B. $Si_{0.5}Ge_{0.5}$ Alloy films

The electrical properties of $Si_{0.5}Ge_{0.5}$ films will now be studied very briefly in order to link the electrical properties of Si and Ge. The transmission electron micrograph for a 100-Å $Si_{0.5}Ge_{0.5}$ film shown in Fig. 1(b) reveals the same defect structure and on the same scale as observed in Si [Fig. 1(a)] and in Ge films.[2,5] At this point, one may comment on the origin of the cracks. Galeener suggested[3] that during growth of the film, two islands of ideally amorphous material are unable to coalesce because atoms cannot satisfy the angle and distance necessary for an ideal tetrahedral bond. One may have expected this condition to be relaxed in the case of a Si-Ge alloy but one may argue that Si is so much like Ge that the same bonds are required. We have, however, observed the same crack network in a Ge-Ni alloy where Ni acts as a strongly localized state[23] and also in amorphous InSb films[24] which suggests that the cracks do not form because of bond requirement, but simply because of the brittleness of these materials.

The planar temperature dependence of the resistance for $Si_{0.5}Ge_{0.5}$ films deposited at 300 and 77 °K is shown in Fig. 6. The values of the pertinent parameters are summarized in Table II. For room-temperature-deposited films the value of

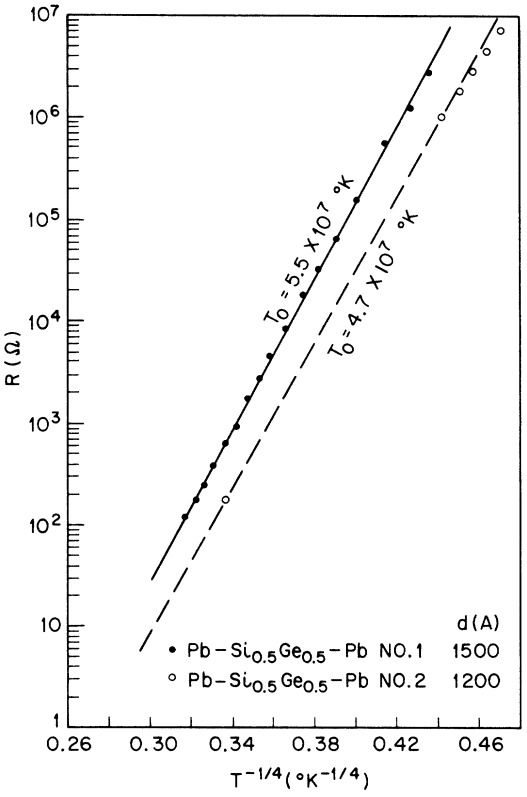

FIG. 7. Temperature dependence of the transverse resistance for films deposited at 77 °K.

$T_0 \simeq 1.3 \times 10^8$ °K is intermediate between the value for Si (8×10^7 °K) and that previously reported for Ge[1] (3×10^8 °K). Films deposited at 77 °K also display a value of T_0(5.7×10^7 °K) intermediate between Si (4.5×10^7 °K) and Ge[1] (10^8 °K), although closer to the Si value. On the other hand, the value of $\rho_{\text{extr RT}}$ for films deposited at 77 °K (2 Ω cm) is close to the value observed for Si. The annealing behavior of such films is very similar to the one reported for Si and Ge: The resistance increases around 120 °K as shown by the deviation from the low-temperature data and the electrical parameters of the annealed film (T_0 and ρ_{RT}) approach those of a room-temperature-deposited film (Table II and Fig. 6).

The temperature dependence of the transverse resistance for $Si_{0.5}Ge_{0.5}$ films deposited at 77 °K is shown in Fig. 7. For some unknown reason, it was impossible in the present case to prepare sandwiches with a $Si_{0.5}Ge_{0.5}$ layer thinner than 1200 Å because shorts would develop. We can, however, conclude from Table II that the values of $\rho_{\text{extr RT}}$ and T_0 for the transverse measurements are very close to those of the planar measurements. The anisotropy shown by the 1200-Å sandwich is very small and within experimental error. If any anisotropy is present at all, it must occur below 1200 Å, and consequently, one may conclude that alloying has the effect of reducing the anisotropy observed in the amorphous elements (Si and Ge).

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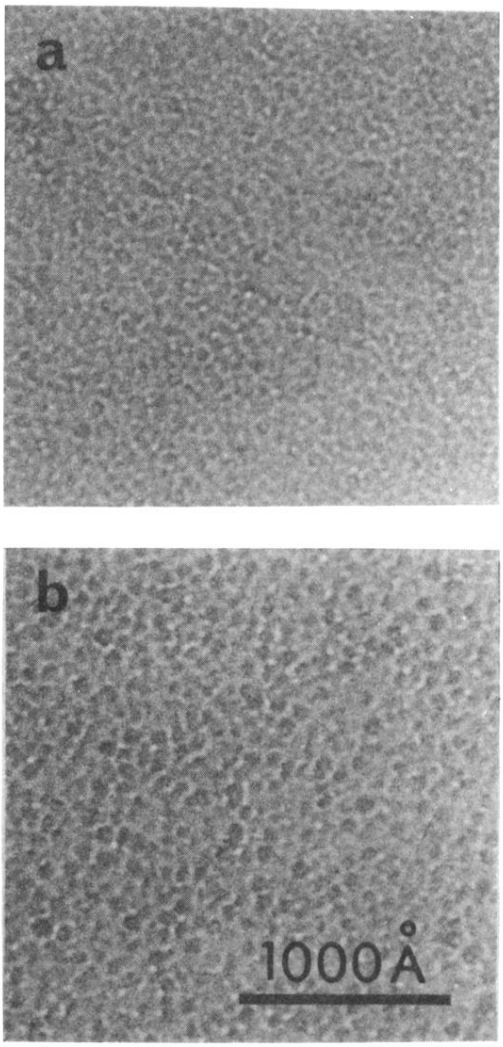

FIG. 1. Bright-field electron micrographs of (a) a 100-Å Si film and (b) a 100-Å $Si_{0.5}Ge_{0.5}$ film deposited at room temperature on NaCl showing dark film areas $\simeq 40$ Å surrounded by a network of cracks.