

## Enhanced annealing, high Curie temperature, and low-voltage gating in (Ga,Mn)As: A surface oxide control study

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Our x-ray photoemission, magnetization, and transport studies on surface-etched and annealed (Ga,Mn)As epilayers elucidate the key role of the surface oxide in controlling the outdiffusion of self-compensating interstitial Mn impurities. We achieved a dramatic reduction in annealing times necessary to optimize the epilayers after growth and synthesized (Ga,Mn)As films with the Curie temperature reaching 180 K. A  $p$ - $n$  junction transistor is introduced, allowing for a large hole depletion in (Ga,Mn)As thin films at a few volts. The surface oxide etching procedure is applied to controllably reduce the thickness of the (Ga,Mn)As layer in the transistor and we observe a further strong enhancement of the field-effect on the channel resistance. The utility of our all-semiconductor ferromagnetic field-effect transistor in spintronic research is demonstrated on the measured large field effect on the anisotropic magnetoresistance.

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### I. INTRODUCTION

(Ga,Mn)As and related diluted magnetic semiconductors<sup>1,2</sup> play a major role in spintronic research because of their potential to combine ferromagnetism and electrical gating in one physical system. High Curie temperatures require high concentrations of substitutional Mn<sub>Ga</sub>; however, self-compensation by interstitial Mn impurities<sup>3–20</sup> becomes a severe limiting factor on ferromagnetism in (Ga,Mn)As at Mn dopings  $\geq 4\%$ .<sup>21</sup> The limits and utility of electrical gating of this highly doped semiconductor are not yet established; so far electric-field effects have been demonstrated on magnetization with tens of volts applied on a top-gate field-effect transistor (FET) with an oxide dielectric separating the metal gate from the (Ga,Mn)As channel.<sup>22</sup> In the first part of the experimental Sec. II A, we elucidate the physical mechanism controlling the postgrowth removal of interstitial Mn. The work builds on the observation of a large enhancement of annealing efficiency due to surface oxide etching, and on complementary structural, magnetic, and transport characterization studies. In the second part (Sec. II B), we introduce an all-semiconductor, epitaxial  $p$ - $n$  junction FET, allowing for a large depletion of (Ga,Mn)As thin films at a few volts. We apply the surface oxide etching procedure to controllably thin the (Ga,Mn)As layer in a fabricated transistor and observe a further strong enhancement of the field effect on the channel resistance. Gatable spintronic characteristic of our  $p$ - $n$  junction ferromagnetic FET is demonstrated on anisotropic magnetoresistance (AMR) measurements.

### II. EXPERIMENT

#### A. Etch-assisted annealing

(Ga,Mn)As samples employed in our study were grown by low-temperature molecular-beam epitaxy (LT-MBE). In-

terstitial Mn impurities, which inevitably form during the LT-MBE growth at high dopings, act as compensating donors and reduce the magnetic moment by forming antiferromagnetically coupled pairs with substitutional Mn<sub>Ga</sub> acceptors.<sup>21</sup> They can be removed by postgrowth annealing at temperatures close to the growth temperature.<sup>5–9</sup> A number of complementary experiments have concluded that interstitial Mn ions out diffuse during annealing toward the (Ga,Mn)As surface. Nevertheless, whether the mechanism limiting the diffusion has its origin in the (Ga,Mn)As bulk or in the surface oxide has remained a controversial open problem.<sup>7,9–11,14,15,18–20</sup> Figures 1 and 2 provide a resolution to this question.

Figure 1(a) shows superconducting quantum interference device (SQUID) measurements of the remanent magnetic

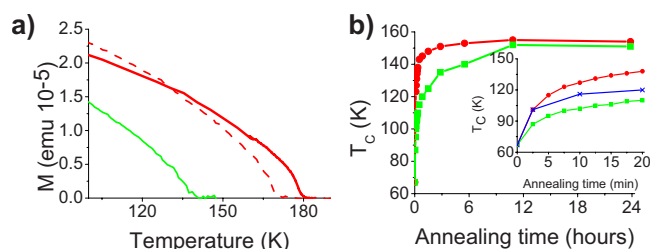


FIG. 1. (Color online) (a) Remanent magnetic moment measured by SQUID as a function of temperature for a 15 min continuously annealed sample (lower solid line), and for samples treated with the etch-anneal procedure for 15 min (dashed line) and 40 min (upper solid line). All samples were prepared from a 35 nm, approximately 11%-doped (Ga,Mn)As wafer. (b) Curie temperature as a function of the postgrowth treatment time for the continuous annealing (lower dependence), for the etch-anneal procedure including etching before each annealing interval (upper dependence), and for continuous annealing following a single etching of the as-grown film (middle dependence in the inset). A standard, 50 nm approximately 7%-doped (Ga,Mn)As wafer was used for this study.

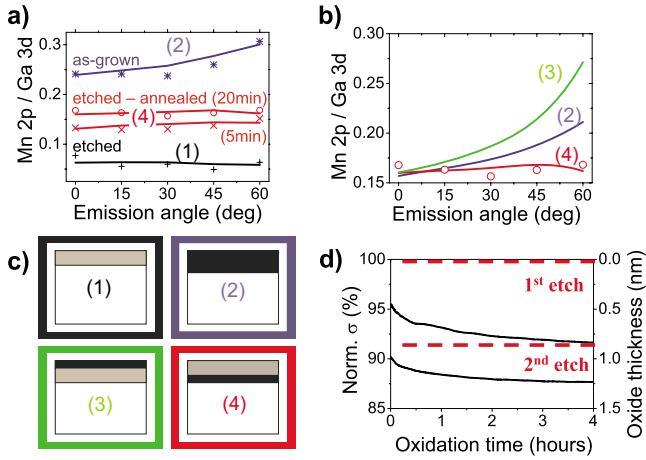


FIG. 2. (Color online) (a) Angle-resolved XPS measurements of the ratio of Mn- $2p$  and Ga- $3d$  photoelectron line intensities on an as-grown, etched, and etched-annealed 50 nm, 8% Mn-doped (Ga,Mn)As. Color coding of the symbols and fitted lines correspond to the models sketched in panel (c) of Mn distribution in the oxidized and unoxidized parts of the (Ga,Mn)As film assumed in the fitting. (b) XPS measurements on the etched and 20 min annealed sample (red symbols), and fitted curves with the color coding corresponding to Mn-distribution models of panel (c). (c) Schematic distribution of excess Mn (dark region) in the (Ga,Mn)As wafer consisting of the unoxidized (white region) and oxidized (gray region) parts. (d) Two subsequent measurements, starting from an as-grown 10 nm, 8% Mn-doped (Ga,Mn)As wafer, of time-dependent normalized conductance recorded from 2 min after etching. Oxide thicknesses are recalculated assuming the conductance to be proportional to the thickness of the unoxidized (Ga,Mn)As layer.

moment in a 35 nm (Ga,Mn)As film with approximately 11% nominal Mn doping. The annealing was performed in air by placing the sample on a hot plate with temperature 200 °C. Two different annealing procedures are compared for samples cleaved from the same wafer, which was rotated during growth to ensure homogeneity across the epilayer. Aside from the standard continuous annealing, a sequence of discrete etch-anneal steps has been applied, each consisting of 30 s etching in 30% HCl, rinsing in water, and subsequent annealing for 5 min. (The HCl etched surface is hydrophobic and dries off instantly after the rinsing.) With continuous annealing, the as-grown Curie temperature  $T_c=85$  K is increased to  $T_c=137$  K after 15 min of annealing and a maximum  $T_c=176$  K is reached in 100 min. By employing the etch-anneal technique,  $T_c=170$  K is reached in 15 min and a saturated value of  $T_c=180$  K is obtained in 40 min. We see a large reduction in the annealing time due to surface oxide etching. The procedure also yields a sizable increase in the maximum attainable Curie temperature in this wafer.

In Fig. 1(b) we present a detailed investigation of the etch-anneal process. To demonstrate that our findings are generic, we show results for a standard, approximately 7% Mn-doped 50-nm-thick (Ga,Mn)As epilayer. (Same qualitative conclusions on the essential role of the surface oxide were obtained in all studied epilayers with thicknesses ranging from  $\sim 10$  to 200 nm.) In the main panel of Fig. 1(b), we compare two sets of SQUID Curie temperature measure-

ments as a function of annealing time: one for continuous annealing and the other for the etch-anneal procedure. In the inset, we compare these two measurements with annealing of the sample exposed to a single etching before the first annealing step. The presence of the surface oxide layer clearly plays the crucial limiting role in the (Ga,Mn)As annealing process. By repeating several etch-anneal steps instead of annealing continuously, the postgrowth treatment time for reaching maximum  $T_c$  is slashed by a factor of ten. Furthermore, the inset indicates that the oxide layer formed after growth, which is very rich in Mn as discussed below, and the oxide layer regrown on a clean (Ga,Mn)As surface during annealing are comparably efficient in blocking the interstitial Mn removal.

Without passivation of out-diffused Mn ions by oxidation (or nitridation, etc.), the diffusion of the interstitial Mn ions toward the (Ga,Mn)As free surface is inhibited by the formation of an electrostatic barrier.<sup>7–11,15,18</sup> From this perspective, the key role of the surface oxide in the annealing process is plausible as it might prevent the Mn ions and free oxygen from interacting with each other. Indeed the shorter (by  $\sim 20\%$ ) metal-oxygen bond lengths, compared to the semiconductor bonds, less interstitial space, and amorphous structure, can effectively block the impurity diffusion channels through the oxide.<sup>23</sup> (Note that since these characteristics of the surface oxide are generic, our findings might apply to a wide range of heavily doped semiconductors with metastable self-compensating impurities.) To quantify these arguments, we performed a series of complementary x-ray photoemission spectroscopy (XPS), magnetization, and transport measurements.

The angular-dependent XPS study was done on a 50 nm (Ga,Mn)As epilayer with approximately 8% Mn doping from which we prepared four different samples: a piece of an as-grown material, a sample once etched after growth and unannealed, a piece etched and annealed for 5 min, and another sample etched and annealed for 20 min. Ga- $3d$ , Mn- $2p$ , and O- $1s$  photoelectron line intensities were recorded with the angle-dependent probing depth up to 3 nm, and we used SESSA software package to simulate the XPS data. The fit of the measured O- $1s$ /Ga- $3d$  ratios yields 9 Å thickness of the oxidized (Ga,Mn)As layer in the as-grown material; in the etched unannealed sample, measured 30 min after etching, the fitted oxidized layer thickness is 5.3 Å [comparable to results of XPS measurements in pure GaAs (Ref. 24)]. The angular dependencies of the Mn- $2p$ /Ga- $3d$  ratio for the four studied samples are plotted in Fig. 2(a). The best fit for the as-grown material is obtained by assuming 8.8% Mn concentration in the unoxidized (Ga,Mn)As, which is consistent with the nominal Mn doping, and a 44% Mn concentration in the 9 Å surface oxide. In the etched unannealed samples, the same fitted values of 8.8% Mn are found in the 5.3 Å oxidized layer and in the (Ga,Mn)As film underneath.

The analysis of the etched and 20 min annealed sample, which shows a sizable reemergence of Mn at the surface due to annealing, is detailed in Fig. 2(b). To fit the corresponding XPS data, we considered a Mn rich layer on top of the oxide, a uniform distribution of Mn in the Mn-rich oxide, and a Mn-rich layer at the interface of the oxide and unoxidized (Ga,Mn)As [see Fig. 2(c)]. Clearly the last model provides

the best fit to the measured data with an average thickness of the Mn-rich interfacial layer of 2 Å. We conclude that the Mn passivation takes place at the bottom of the oxide layer by oxygen that has diffused through the oxide and reached the interface with (Ga,Mn)As. Note that the picture is consistent with previous studies of GaAs oxidation, which found a substantially smaller diffusivity through the oxide film of metal atoms as compared to oxygen.<sup>25</sup>

Complementary estimates of the oxide thickness based on the measured reduction in the total moment and conductance, which can be readily performed in highly doped thin (Ga,Mn)As films, are consistent with the XPS analysis. In Fig. 2(d) we show two subsequent measurements of the time-dependent room-temperature resistance of a nominally 10 nm, approximately 8% Mn-doped (Ga,Mn)As wafer. Each experiment started with etching the surface oxide and then, after 2 min, we began monitoring for several hours the time evolution of the resistance due to reoxidation of the (Ga,Mn)As surface. Oxide layer thicknesses were obtained by assuming the conductance to be proportional to the thickness of the unoxidized (Ga,Mn)As. In a few minutes after etching, a several-Å-thick oxide layer quickly forms at the surface, followed by a significantly lower-rate oxidation process. Oxide etching and subsequent reoxidation can therefore be used for a controllable thinning of (Ga,Mn)As films in subnanometer steps when studying numerous scaling characteristics of ferromagnetic semiconductors with the film thickness and areal density of carriers. Gating of thin (Ga,Mn)As epilayers, discussed in the remaining paragraphs, is one example where this technique can be utilized.

### B. Low voltage gating

In Figs. 3(a) we show schematics of our (Ga,Mn)As FET together with the top view of the source and drain electrodes. A heavily doped ( $n=2 \times 10^{18} \text{ cm}^{-3}$ ) epitaxial *n*-GaAs buffer layer forms the gate electrode. It is separated from the *p*-type ( $p \sim 10^{20} \text{ cm}^{-3}$  hole concentration) (Ga,Mn)As film by a  $w_{\text{AlAs}}=20\text{-nm}$ -thick undoped AlAs barrier to eliminate channel-gate leakage currents. We verified that the leakage currents in all measurements shown in Figs. 3 are negligible. Figures 3(b) and 3(c) show two gating characteristics of the resistance of one physical device in which the electrodes were first patterned by optical lithography on a 4-nm-thick (plus a 1 nm oxidized surface layer), approximately 8% Mn-doped (Ga,Mn)As. After measuring this device, the (Ga,Mn)As layer was further etched to approximately 3 nm without removing the contacts and again measured. In both cases we find a marked decrease in the (Ga,Mn)As channel conductance upon depletion induced by gating. The gating efficiency is enhanced in the thinned sample, consistent with the increased relative depletion at a given voltage. Note that the large amplification of the field-effect with decreasing temperature we observed is attributed to the vicinity of the metal-insulator transition in the studied (Ga,Mn)As.

Theoretically, we can confirm the viability of the *p-n* junction FET approach to low-voltage gating of thin (Ga,Mn)As films by assuming abrupt depletion in the *p*-type region (with depletion length  $w_p$ ) and in the *n*-type region on

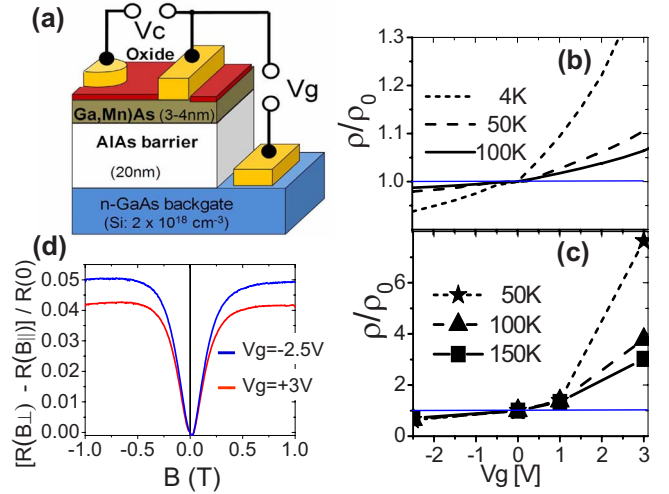


FIG. 3. (Color online) (a) Schematic side view of the (Ga,Mn)As FET structure. (b) Gate voltage dependence of the source-drain resistivity relative to the resistivity at zero gate voltage for the FET device with 4-nm-thick (Ga,Mn)As (plus a 1 nm oxidized surface layer) measured at different temperatures. (c) Same as (b) after thinning the (Ga,Mn)As layer to 3 nm by etching. (d) Difference between in-plane and out-of-plane magnetoresistance curves (at 37 K) corresponding at saturation to the AMR.

either side of the AlAs barrier, the respective dielectric constants  $\epsilon_{\text{GaAs}}=12.85$  and  $\epsilon_{\text{AlAs}}=10.06$  of GaAs and AlAs, and the GaAs band gap  $\Delta_{\text{GaAs}}=1.5 \text{ eV}$ :

$$w_p = -\frac{\epsilon_{\text{GaAs}}}{\epsilon_{\text{AlAs}}} \frac{n}{n+p} w_{\text{AlAs}} + \left[ \left( \frac{\epsilon_{\text{GaAs}}}{\epsilon_{\text{AlAs}}} \frac{n}{n+p} w_{\text{AlAs}} \right)^2 + 2\epsilon_{\text{GaAs}} \frac{n(\Delta_{\text{GaAs}} + V_g)}{p(n+p)} \right]^{1/2}.$$

For the 4-nm-thick (Ga,Mn)As, one obtains 18% depletion at 3 V and 34% depletion at 10 V. These estimates of sizable relative depletions at low voltages are fully supported by our numerical modeling, using SILVACO-ATLAS simulator, in which the depletion edge is smeared out over a distance of about 0.7–1 nm.<sup>26</sup>

Detailed investigation of magnetic characteristics of a series of our (Ga,Mn)As *p-n* junction FETs, including observed field-induced shifts in  $T_c$  on the measured  $d\rho/dT$  peak positions,<sup>27</sup> will be discussed elsewhere.<sup>26</sup> Here we present the data sets, measured in the above 4 nm (Ga,Mn)As FET, which illustrate the utility of the device as a three-terminal spintronic element. Since AMR is at the very foundation of spintronics, it is a particularly suitable phenomenon for our demonstration. In Fig. 3(d) we plot the difference between field-sweep measurements for in-plane magnetic field and for perpendicular-to-plane field orientations. At saturation, the difference gives the AMR.<sup>28,29</sup> We find that the AMR decreases from 5% at  $-2.5 \text{ V}$  (accumulation) to 4% at  $+3 \text{ V}$  (depletion), i.e., the field effect on the AMR is of the same order as the AMR itself.

### III. SUMMARY

To summarize we have presented several advancements toward the understanding of basic physical limits of (Ga,Mn)As as a functional ferromagnetic semiconductor for spintronics. By introducing the etch-anneal postgrowth treatment, we have elucidated the mechanism controlling the passivation of self-compensating interstitial Mn ions at the surface and significantly enhanced their outdiffusion during annealing. Electrical gating of thin (Ga,Mn)As films was explored on a *p-n* junction (Ga,Mn)As FET operating at a few volts. Its free (Ga,Mn)As surface geometry allows for a controllable thinning of the (Ga,Mn)As layer in subnanometer steps by etching and reoxidation, resulting in a significant enhancement of the gating efficiency. The three-terminal spintronic device characteristic was demonstrated on field-effect AMR measurements.

After we submitted this manuscript, the technique reported here inspired growth efforts in the range of approximately 11%–13% nominal Mn dopings, leading to the achievement of a record  $T_c=185$  K simultaneously in two independent MBE laboratories, Nottingham<sup>30</sup> and Prague.

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