Using granular film to suppress charge leakage in a single-electron latch

Alexei O. Orlov,[1] Xiangning Luo,[1] Kameshwar K. Yadavalli,[1,2] I. S. Beloborodov,[3,4] and Gregory L. Snider[1]
[1]*Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana 46556, USA*
[2]*Department of Electrical Engineering, University of California, Los Angeles, Los Angeles, CA 90095, USA*
[3]*Materials Science Division, Argonne National Laboratory, Argonne, IL 60439, USA*
[4]*James Franck Institute,University of Chicago, IL 60637, USA*
(Received 8 September 2007; published 15 February 2008)

A single-electron latch is a device that can be used as a building block for quantum-dot cellular automata circuits. It consists of three nanoscale metal "dots" connected in series by tunnel junctions; charging of the dots is controlled by three electrostatic gates. One very important feature of a single-electron latch is its ability to store ("latch") information represented by the location of a single electron within the three dots. To obtain latching, the undesirable leakage of charge during the retention time must be suppressed. Previously, to achieve this goal, multiple tunnel junctions were used to connect the three dots. However, this method of charge leakage suppression requires an additional compensation of the background charges affecting each parasitic dot in the array of junctions. We report a single-electron latch where a granular metal film is used to fabricate the middle dot in the latch which concurrently acts as a charge leakage suppressor. This latch has no parasitic dots, therefore the background charge compensation procedure is greatly simplified. We discuss the origins of charge leakage suppression and possible applications of granular metal dots for various single-electron circuits.

DOI: 10.1103/PhysRevB.77.075414 PACS number(s): 85.35.Gv

INTRODUCTION

Quantum-dot cellular automata[1,2] (QCA) is an inherently nanostructure-compatible binary architecture that uses interaction between nominally identical bistable building blocks ("cells") that are locally connected to each other solely by field-coupling forces to encode and process binary information with minimal power dissipation. The logic function performed by QCA is defined by the physical placement of the array of cells, which can be realized in different physical systems.

In the electronic version of QCA,[1] the information is represented by a spatial location of two excess electrons within an arrangement of four semiconductor quantum dots (or any other "dots" exhibiting Coulomb blockade phenomenon, such as small metal islands, appropriate molecular complexes,[3] etc.) situated in the corners of a square [Fig. 1(a)]. Due to the Coulomb repulsion, the excess electrons can assume two diagonal arrangements that represent two degenerate ground states. Two such cells placed in close proximity will interact by field-coupling forces and, by properly placing such cells, it is possible to build binary logic elements. The presence of the external clocking field is critical to the proper operation of QCA-based systems. It acts as an additional source of energy (on top of the energy supplied by the input), resulting in the predictable switching dynamics that ensures the directionality of the computation. Similar to a power supply in conventional electronics, the energy supplied by the clocking field enables logic level restoration and power gain.

A single-electron latch [Fig. 1(b)], sometimes also referred to as "parametron,"[4] is an elementary building block for QCA architecture that forms a clocked QCA "half-cell." Two such latches form a full QCA cell, also shown in Fig. 1(b). In its metal-tunnel junction implementation,[4,5] a latch consists of three metal dots separated by tunnel junctions, where the tunneling through the center dot D_2 can be controlled by the clock bias V_{CLK}, so that there is a tunable Coulomb barrier separating the end dots. In a single-electron latch, a binary bit of information is represented by the spatial location of an excess electron within the device. It has three input terminals [Fig. 1(b)]: differential signal inputs V_{IN}^{+} and V_{IN}^{-}, and clock input V_{CLK} and two differential output terminals V_{OUT}^{+} and V_{OUT}^{-}, by means of which two latches are coupled. There are three possible states of the latch: (1)

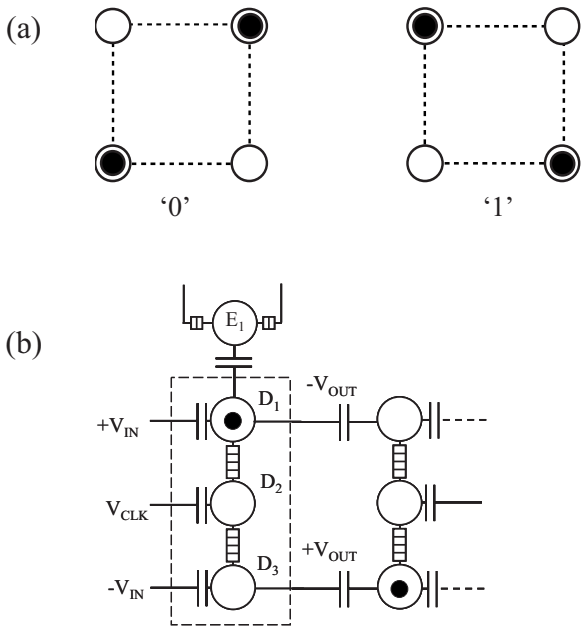

FIG. 1. (a) A four dot QCA cell. Two diagonal electron configurations represent two possible binary states. (b) Functional scheme of a clocked QCA cell based on single-electron latches. Single-electron latch is outlined by a dashed box. E_1 is a SET electrometer to read out the cell polarization.

"null," when it stores no information (and is electrically neutral); (2) "active," when switching of an electron takes place; and (3) "hold," when binary information is preserved in the form of differential output voltage (positive or negative for "0" or "1"), which then acts as an input for the next latch in the QCA circuit, also shown in Fig. 1(b). The state of a latch could be noninvasively readout using a single-electron transistor (SET) (electrometer E_1), capacitively coupled to one of the end dots in the latch [D_1 in Fig. 1(b)].

The operation sequence of a single-electron latch is defined by the combination of applied clock and input voltages. Initially, both clock and input signals are set to zero, so the latch is electrically neutral (null state). In this state, it does not carry any information. When a small differential input voltage, V_{IN}, is applied to end dots (D_1 and D_3), the latch remains in the null state because the input signal is insufficient to lift the Coulomb blockade for tunneling within the dots. Only when the clock signal, V_{CLK}, is applied is an electron forced from D_2 to the end dot coupled to positive input, $+V_{IN}$. The magnitude of V_{CLK} is chosen to maximize the Coulomb blockade for tunneling from the end dot after a single electron is transferred, thus trapping ("latching") an electron. Once the electron is latched, the input signal can be removed, and the electron remains trapped until V_{CLK} is set back to zero.

However, once an electron is latched and input signal is removed, there is a finite probability for it to escape to the opposite end dot (it cannot return to the middle dot since it is energetically unfavorable). The escape of an electron during the hold time of the latch is called a "leakage" or "decay" error, which is characterized by a leakage error rate, Γ_L (s^{-1}). There are several mechanisms which can cause this process: (1) thermal excitation over the Coulomb barrier, (2) simultaneous tunneling of several electrons (cotunneling[6]), (3) photon-assisted tunneling and cotunneling (PAT),[7] and (4) random background charge (RBC) fluctuations.

One way to reduce the leakage rate in single-electron devices is to increase the number of junctions N connecting the dots. In single-electron devices such as pumps[8] and traps,[9] the use of multiple tunnel junctions (MTJs) reduces the leakage rate because each of the above leakage mechanisms is a strong function of the number of junctions N. Indeed, an increase in N raises the height (W) of the Coulomb barrier[10] ($W \propto N$), thus reducing the leakage rate due to the thermal activation: $\Gamma_{\mathrm{LTherm}} \sim \exp(-W/k_BT)$. It also reduces the leakage rate due to cotunneling[6] $\Gamma_{LCot} \propto \{[(eV)^2+(k_BT)^2]/E_C^2\}^{N-1}$ under the influence of small bias $V \ll E_C/e$ across the array of N junctions (E_C is charging energy). The rate of photon-assisted electron leakage,[11] Γ_{LPAT}, is also reduced because it is inversely proportional to the barrier height: $\Gamma_{\mathrm{LPAT}} \propto 1/W$. Leakage processes in single-electron devices containing MTJs were extensively studied in recent publications.[11–18] Experimental and theoretical investigations[17,19] suggest that in metal single-electron devices with MTJs at moderately high temperatures ($\geqslant$150 mK) or in the presence of a bias across the junctions ($V \geqslant 50\ \mu$V), the leakage errors are dominated by thermal activation over the Coulomb barrier.[17,20–22] At lower temperatures ($<$100 mK) and for $N<4$, cotunneling is deemed to be the dominant mechanism of leakage errors,[23] and for $N \geqslant 5$, a large number of experiments suggest that leakage errors are dominated by photon-assisted tunneling and cotunneling driven by nonequilibrium $1/f$ noise associated with heat dissipation in the substrate.[24] Theory and experiments show that this noise has enough power at microwave frequencies to trigger the PAT processes.[11,16] These results explain the large discrepancy (by many orders of magnitude) between the observed leakage rate and that predicted by the orthodox theory of single-electron tunneling and cotunneling[6,10] for metal-tunnel junction devices. Finally, leakage errors could be caused by the RBC fluctuations which affect the long-term stability of the single-electron devices. The RBC fluctuations change the potential profile around the device and, therefore, require retuning of the entire device (since they affect the entire device operation and not just the leakage errors). The time scale of the fluctuations is typically on the order of hours. The RBC fluctuations and photon-assisted tunneling apparently have the same physical origin (relaxation of nonequilibrium traps resulting in nonequilibrium $1/f$ noise) and tend to decay in time if the device is kept at cryogenic temperatures for long periods of time ($\geqslant$100 h).[24,25]

To reduce the leakage errors in a latch at low temperatures ($<$100 mK) and without a bias between the end dots (hold state) occurring within the stability time when the system remains immune to RBC fluctuations ($\geqslant$1000 s in our experiments), the dominant error mechanism, i.e., photon-assisted tunneling, must be suppressed. For the four junction ($N=4$) traps,[9] the experimentally determined leakage rate was found to be $\Gamma_L > 1\ s^{-1}$, and in pumps with no gate bias applied ("hold state"), the measured rates are $\Gamma_L \sim 10\ s^{-1}$ ($N=4$) (Refs. 11 and 25) and $\Gamma_L \sim 10^{-2}\ s^{-1}$ ($N=6$).[11] Experimentally determined leakage rate in the latch with $N=6$ (Ref. 26) in the hold state was found to be $\Gamma_L \sim 2\ s^{-1}$. The higher leakage rate in the latter experiment compared to a six-junction pump[11] is expected because the electrostatics for the latch in hold state is not the same as for a pump: the equivalent of "hold state" for the pump is a "null state" of the latch,[5] when it carries no information. This is the ground state of the latch and is, therefore, more stable. The hold state in the latch is more similar to that of a single-electron trap in equilibrium, where probabilities for trapping and escape are equal.[20] The major difference between the trap and a latch is how they store the trapped electron: while a trap is usually designed to store the charge after the gate bias is removed, a latch stores an electron while the clock signal is applied and must return to the initial neutral state once the clock signal is set to zero.

The fabrication of latches with MTJs has its own drawbacks, because it leads to the unavoidable formation of additional dots that are affected by the random background charges. This requires additional compensation of these charges for each extra dot, drastically complicating the tuning and operation of the device.

One alternative way to suppress the leakage caused by cotunneling is to use resistive microstrips in series with tunnel junctions instead of increasing N.[27,28] The cotunneling current I_C in N-junction arrays in series with two resistors of value R in the Coulomb blockade regime obeys a power law,

$$I_C \propto V^{\eta}, \quad \eta = 2(N+z) - 1, \tag{1}$$

where V is the bias across the array, R_Q h/e^2 is the resistance quantum, and $z=R/R_Q$ is a dimensionless parameter. The simple implication of Eq. (1) is that resistive strips with resistance $R=R_Q z$ act as MTJs with z junctions, thus reducing the cotunneling rate.[29] The use of embedded resistors reduces the number of junctions required, eliminating the problem of random background charge compensation for the additional dots of MTJs as well as simplifying the design of devices. Experiments have demonstrated the feasibility of the proposed design for electron traps[30] ($N=4$) and pumps ($N=3$),[23] where cotunneling sets the limits to the accuracy of charge transfer. It must be noted that it is extremely difficult to fabricate metallic resistive microstrips of small size, consequently increasing the minimum possible size of the device. Moreover, the use of such microstrips for latches is not practical due to the large self-capacitance of the mictrostrips, $\approx$60 aF/μm,[29] which would severely degrade the charging energy of the dots if such microstrips are embedded in the latch. The increase of the resistance per square can be obtained by using granular metals, however the theory[27,28] is derived only for diffusive conductors where the charge equilibrium is established before a tunneling event occurs. The operation of a SET with granular metal microstrips connecting an Al island to the environment was studied in Ref. 31 The observed strong nonlinearity in the $I_{ds}(V_{ds})$ characteristics of the SET in the blockade region $I \sim V^{\alpha}$, $\alpha \approx 10$, suggests that the cotunneling was strongly suppressed. In our recent work,[32] we demonstrated the operation of a single-electron transistor where a granular metal film was used as an island material and two traditional AlO_x tunnel junctions connected the island to the source and drain wires. We showed that such a device also exhibits strong nonlinearity in the blockade region: $I \sim V^{\alpha}$, where $\alpha \approx 9$. [It must be noted that the direct application of formula (1) would lead to a different conclusion based on an estimate of parameter $\eta \gg 10$, which is not surprising since the theory was developed for linear diffusive resistors, whereas the conduction mechanism in granular film is attributed to hopping of electrons between the remote grains.[33]] The temperature dependence of the conductance of the film forming the island, G, is of variable-range hopping type, commonly observed in granular metal films on the insulating part of metal-insulator transition:[34]

$$G \propto G_0 \exp(-T_0/T)^{\alpha}, \tag{2}$$

where $\alpha \approx 0.5$, $G_0 < 10^{-5}$ S, and $T_0 \leqslant 10$ K (for the details of these measurements, see Refs. 32, 35, and 36). The "insulating" type of behavior implies that the conduction in the film occurs by means of tunneling between the isolated grains (or clusters of grains). Therefore, the model of interconnected tunnel junctions is relevant here. Based on these observations, we speculate that the use of such granular films must not only affect the cotunneling, but also reduce the photon-assisted tunneling through the middle island. This makes it appropriate for use in the single-electron latches. A strong nonlinearity of the I-V characteristic of the film is expected to increase the barrier for tunneling in the hold state. Also, the size of the granular metal dot can be made much smaller than that of diffusive linear resistors, so the self-capacitance of such a dot can be made very small. To verify the relevance of this approach, we fabricated and characterized a single-electron latch with granular metal (GM) middle-dot connected to the two Al end dots by single AlO_x junctions.

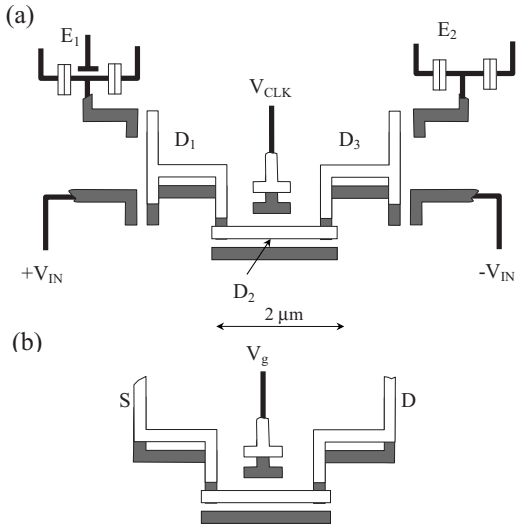

FIG. 2. Sketches of single-electron devices employing granular metal islands. Aluminum (Al) with thin oxide on top is shown in gray, white bars represent CrO_x film deposited on top of Al. (a) Single-electron latch. Middle dot D_2 is made of granular metal. Differential input signals ($+V_{IN}$ and V_{IN}), clock signal (V_{CLK}), and electrometers (E_1 and E_2) are capacitively coupled to D_1, D_2, and D_3 as shown in the figure. Electrometers E_1 and E_2 are fabricated in the second step of e-beam lithography. (b) Single-electron transistor with granular metal (CrO_x) island. Source and drain leads, and the gate, are shown.

The ease of adjusting electronic properties of granular metal films is one of their most attractive assets for fundamental studies of disordered solids as well as for the applications. An early determination and understanding of the properties of granular materials will have far reaching consequences for future electronics devices.

FABRICATION AND MEASUREMENT TECHNIQUE

The device was fabricated by two steps of e-beam lithography and shadow evaporation.[37] In the first e-beam lithography step, the latch is fabricated, and in the second step, two SET electrometers[38] are fabricated. The sketch of the device is shown in Fig. 2(a). To fabricate the latch, two Al end dots [D_1 and D_3 in Fig. 2(a)] and a "dummy" middle dot are first deposited at an angle of +6.2° with respect to the normal, followed by *in situ* oxidation of the surface of the Al layer. Then, a CrO_x GM film (the middle dot D_2) is formed by evaporating Cr at a negative angle, −6.2° with respect to the normal in oxygen ambient. As a result, in the overlap region, we obtain a thin AlO_x layer sandwiched between Al and CrO_x layers. The resistivity of the GM strip is controlled by adjusting the oxygen pressure in the evaporator chamber.[31,35] The sheet resistance of the GM strip is estimated from the

measurements of SET with CrO_x island [Fig. 2(b)] fabricated along with the latch with the same design of the island and the junctions;[32] sheet resistance ~3–5 kΩ/□ at room temperature is obtained. At low temperatures (~100 mK), the value of the sheet resistance of the GM strip with zero bias across it is on the order of 10 MΩ/□, but it drops exponentially down to about 100 kΩ/□ for 0.5 mV of applied bias. The value of the junction resistance was obtained from the measurements of the SET at high source-drain bias when the Coulomb blockade is completely suppressed ($eV_{ds} \geqslant 10E_C$), $R_J \sim 10$ MΩ. Two Al-AlO_x SET electrometers (E_1 and E_2), and the input and clock wires [Fig. 2(a)] are formed in the second layer e-beam lithography step followed by shadow evaporation of Al. (Only one SET is needed to determine the charge state of the latch. The second electrometer is added to improve the chances for measurements in case of junction failure in the SET.) Differential input signals ($+V_{IN}$ and $-V_{IN}$) and the clock signal (V_{CLK}) are capacitively coupled to D_1, D_3, and D_2, respectively. The alignment tolerance between the two steps of e-beam lithography is about 300 nm according to the pattern design, and an alignment accuracy of 200 nm between features defined in the two steps of e-beam lithography is achieved by using predefined alignment marks. For comparison, an Al/AlO_x latch with the same design as above, except that the CrO_x island is replaced by an Al island, is fabricated on the same substrate. In addition, an Al/AlO_x latch with four junctions and similar size dots and coupling capacitors is also fabricated.

The low temperature transport measurements are performed in a dilution refrigerator with a base temperature of 15 mK. Standard lock-in techniques are used in all of the low temperature measurements, with small excitation voltages (10–50 μV) applied to the electrometers to avoid excessive heating of the latch.[15] SET conductance is measured at a frequency ~3 kHz with time constant ~3 ms to provide adequate temporal resolution for phase detection of the pulses with duration ⩾100 ms. The typical electron temperature of the device is estimated to be about 70 mK.[38] A magnetic field of 1 T was applied to suppress the superconductivity of Al.

EXPERIMENTAL RESULTS

The major goal of the experiments described below is to determine the ability of the latch with GM middle dot to suppress charge leakage. The observation of bistability is a direct evidence of single-electron latching that can only be observed when undesired tunneling is strongly suppressed,[38] whereas a lack of bistability clearly points to an excessive leakage rate.[39] One way to observe bistable behavior is to measure "phase plots" in V_{IN}, V_{CLK} coordinates for the two directions of input bias voltage.[38,39] A phase plot is a three-dimensional plot obtained by measuring the voltage on D_1 (D_3) (*Z* axis) using the SET electrometer E_1 (E_2) while linearly scanning input (*X* axis) and stepping clock (*Y* axis) voltages. The electrometer is biased in the middle of the rising slope of a Coulomb blockade oscillation so that a positive voltage increment on D_1 leads to an increase of conductance and vice versa. Black color on the plot corresponds to a negative voltage increment, and white color corresponds to a positive voltage increment on the dot. Figures 3(a) and 3(b) show two phase plots acquired for different directions of the input bias scans for a latch with two junctions and CrO_x middle dot. Bistability in the latch is clearly visible and marked by opposing triangular areas on the phase plot in Figs. 3(a) and 3(b). For comparison, a phase plot for an Al/AlO_x latch with the same design (two junctions) and Al middle dot is shown in Fig. 3(c) (since the phase plots for two directions of the input voltage scans are indistinguishable, only one plot is shown). In this case, we observe no signs of bistability. The transition from one charge state to the other (at $V_{IN} \approx 2$ mV) appears smooth, meaning that the electron moves back and forth in the transitional region and the electrometer measures the time average of the dot potential. The Al/AlO_x latch with four junctions shows only hints of bistability indicated by abrupt transitions, but the bistable area was undeveloped and no latching was observed.[40] The results of these experiments indicate that in the latch with

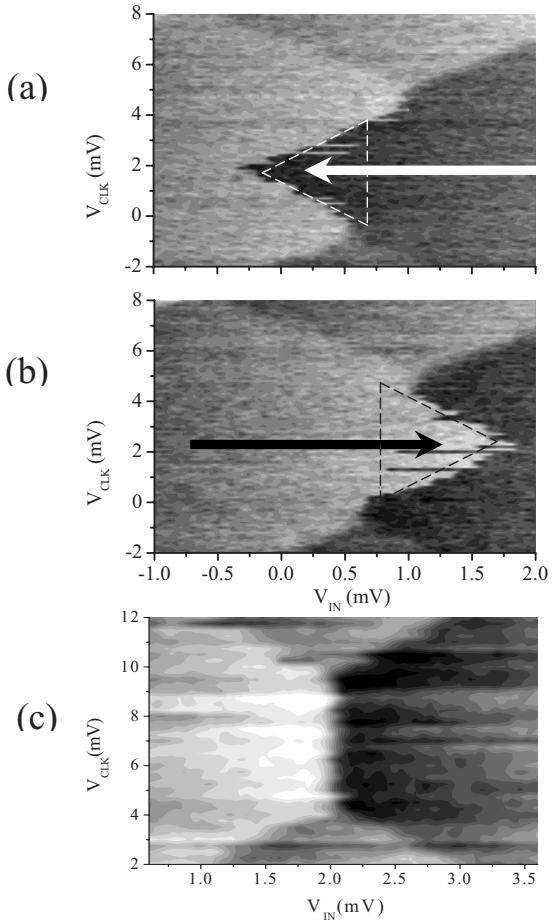

FIG. 3. Phase plots of single-electron latches: [(a) and (b)] Single-electron latch with CrO_x middle dot. Dot potential (of D_1) is measured by electrometer E_1 for two directions of the differential input signal as shown by the arrows (*X* axis is the same for both directions of the input voltage). Triangularly shaped areas outlined with dashed lines indicate bistable behavior. (c) An Al/AlO_x latch with the same design (two junctions). Only one plot is shown because plots for the opposite directions of the scans are indistinguishable in this case. No bistability is seen in this plot.

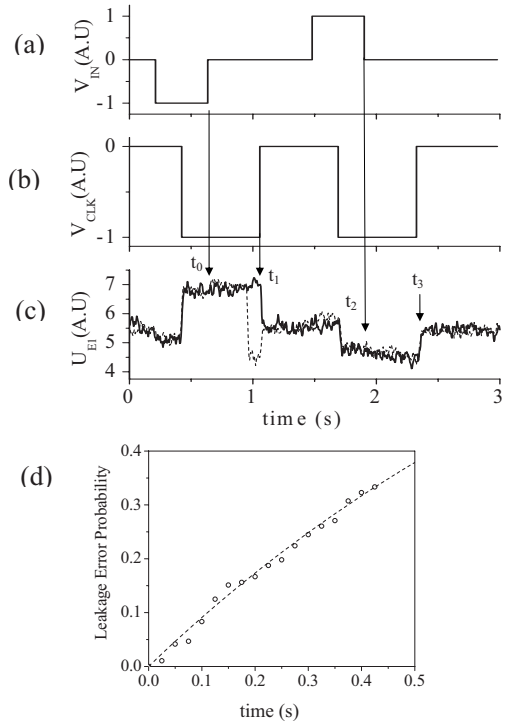

FIG. 4. Operation of the QCA latch with CrO_x middle dot: (a) applied input bias, (b) clock bias, and (c) potential of D_1 measured by electrometer E_1. An instance of a leakage error is shown by the dashed line. (d) Leakage error probability for the latch in the hold state as a function of time elapsed from the moment the electron is latched. Cumulative leakage error probability is plotted for 192 scans as a function of time elapsed from the moment the differential input bias is removed (t_0, t_2). The dashed line is a fit using formula (3) with parameter $\tau = 1.05$ s.

GM middle dot, charge leakage is suppressed much more strongly than in two-junction and four-junction latches having Al middle dots.

The functional operation of a latch with GM middle dot is demonstrated with the input and clock pulse sequence shown in Figs. 4(a) and 4(b) (the detailed description of the setup for this test is given elsewhere[38,39]). The electrostatic potential of dot D_1, monitored by electrometer E_1, is shown in Fig. 4(c). Here, we concentrate on the leakage errors occurring when an electron is trapped on one of the end dots (by the application of the clock signal) and the differential input signal is removed [from t_0 to t_1 and from t_2 to t_3 in Fig. 4(c)]. An instance of such an error is shown by a dashed line in Fig. 4(c). To determine the leakage rate, we repeated the latching sequence in Figs. 4(a) and 4(b) multiple times, and then analyzed the statistical distribution of the cumulative number of leakage errors as a function of time [Fig. 4(d)]. The probability of the leakage error changes in time as:[26]

$$P_{\mathrm{err}}(t) = n_{\mathrm{err}}(t)/n_{\mathrm{total}} = 1 - \exp(-t/\tau), \tag{3}$$

where τ is the retention time constant, $n_{\mathrm{err}}(t)$ is the total number of leakage errors that happened within time interval t, and n_{total} is the total number of clock cycles. By fitting our data to Eq. (3), we extracted the value of $\tau = 1/\Gamma_L \approx 1$ s.

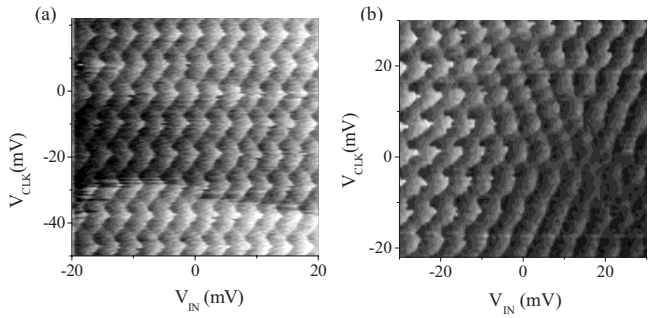

FIG. 5. Large scale phase plots of the two single-electron latches: (a) Latch with two AlO_x junctions and CrO_x middle island. (b) An Al/AlO_x latch with six tunnel junctions (two branches connecting the middle dot to the end dots each have three junctions). Note that a distinct triangular pattern is clearly seen throughout the whole plot for the latch with CrO_x island, whereas it appears only on a small portion of the plot for the Al/AlO_x latch.

Hence, the average electron leakage rate is $\Gamma_L \approx 1\ \mathrm{s}^{-1}$. Thus, we conclude that the presence of GM film reduces leakage error rate to the level observed in an Al/AlO_x latch with six junctions.[38]

Another remarkable feature of the latch with GM middle dot is the uniformity of the observed charging diagram pattern for large scale scans of clocking and input biases depicted in Fig. 5(a). For comparison, the data obtained from the six-junction Al/AlO_x device[41] is shown in Fig. 5(b). Due to the presence of the random background charges on the parasitic islands in the six-junction Al/AlO_x device, the pattern in Fig. 5(b) is nonuniform and only small areas in the plot (where the distinct triangular pattern is present) can be used for latch operation. In these areas, the random background charges on the parasitic dots are compensated by particular combination of the offset voltages on the input and clock electrodes. A change in the RBC configuration beyond the stability time changes *the pattern* observed in Fig. 5(b) so that latching may not be achievable for the same areas where the triangular pattern is currently seen in the plot, requiring retuning of the latch operating conditions $(V_{\mathrm{IN}}, V_{\mathrm{CLK}})$. In contrast, the pattern in Fig. 5(a) experiences no such change: the latch with GM middle dot shows uniform periodic bistable behavior, where the periods are defined by the coupling capacitors; a change in the RBC configuration leads only to an offset of the pattern as a whole along axes V_{CLK} and V_{IN}. Therefore, it can be easily compensated by small adjustments of the offset biases applied to the input and clock electrodes, as there are no extra parasitic dots which require individual compensation. This result correlates with the observation that the gate voltage dependence of the conductance for a SET with GM island[32] only exhibits single period of Coulomb blockade oscillations, i.e., the island behaves as a uniform metal dot.

DISCUSSION

Two pertinent questions will be addressed here: (1) why is it possible to achieve control over single-electron charge transfer in a latch with GM middle dot? (2) What causes the

suppression of charge leakage in such a device?

As discussed above, the GM film forming the middle dot in the latch can be viewed as an array of interconnected nanometer-sized metal dots intermixed with the oxide. The unavoidable presence of the background charge in the film randomly shifts the Coulomb blockade thresholds for the individual grains, affecting their charging energy such that there is no hard gap in the density of states in the GM dot.[42] The value of capacitance coupling the gate to an individual grain can be estimated based on the average grain size $\sim$10 nm,[32] and it is orders of magnitude less than the capacitance from the gate to the whole GM dot. Thus, the periods of Coulomb blockade oscillations are expected to be far greater for the individual grains than for the whole GM dot. As a result, a change in the gate voltage does not influence individual grains (for the same reason, frustrated two-dimensional arrays of tunnel junctions studied in Ref. 43 exhibit no gate voltage dependence) and the GM dot behaves as a single metal dot with respect to the external gate despite the fact that its conductance exhibits nonmetallic temperature dependence.[32] This makes it possible to control the electron transfer between the end dots in the single-electron latch, with V_{CLK} applied to the GM middle dot.

As regards the suppression of charge leakage, the presence of a MTJ, either lithographically defined or "naturally formed," is expected to attenuate tunneling processes responsible for charge leakage, including the dominant PAT mechanism, as more photons are required to transfer charge over a larger number of junctions.[16] It is, therefore, reasonable to assume that the GM film will act as charge leakage suppressor. The details of the conduction mechanism in granular films have recently attracted a great deal of theoretical attention.[44–46] The common conclusion is that conduction through GM film at low temperatures and small biases is due to tunneling through virtual states ("multiple cotunneling"[44]), which bypasses simple activation over the Coulomb barriers separating nearest neighbor grains. This mechanism explains why GM films remain conductive even at very low temperatures despite the high charging energies of the individual grains. At the same time, the conductance through a GM film at low biases across it is much lower than in any diffusive microstrip resistor, so that any undesired tunneling is strongly suppressed. This is the condition required for low leakage rate. On the other hand, once the bias is applied, the conductance of the GM dot rises exponentially, resulting in fast switching of an electron. These are very attractive characteristics for a single-electron latch since it is not necessary to give up switching speed to obtain low leakage. Clearly, a more accurate theoretical model is required to describe the details of charge transfer in this device, particularly to find out the effectiveness of charge leakage suppression and to determine the important parameters of the GM films which can be used to optimize the performance of the devices.

In conclusion, we have fabricated and tested a single-electron QCA latch with a middle dot made of granular metal film (CrO_x) connected to the end Al dots with single AlO_x tunnel junctions, to investigate the applicability of GM charge leakage suppressors for single-electron logic devices. We observe latching with a leakage error rate, $\Gamma_L \approx 1\ \mathrm{s}^{-1}$, comparable to that obtained for the Al-AlO_x latches using six junctions. The observed charge leakage suppression is provided by the granular media of the central island. The size of the devices with GM leakage suppressors can be made much smaller than by using metallic resistive microstrips, thus alleviating the reduced charging energy associated with the large self-capacitance of the metallic microstrips. We believe that granular metal films can be used for the fabrication of the devices, providing precise charge transfer (pumps and turnstiles) with reduced size and smaller number of lithographically defined tunnel junctions. It also can be potentially used for the fabrication of single-electron memory devices, where strong nonlinearity of the *I-V* characteristic can be beneficial for short write time and long retention time.

ACKNOWLEDGMENTS

The authors wish to thank N. M. Zimmerman for reading the paper and for numerous valuable suggestions. The critical comments of S. V. Demishev and N. E. Sluchanko are gratefully acknowledged. The work was supported by the MRSEC Center for Nanoscopic Materials Design of the National Science Foundation under Contract No. DMR-0080016 and NSF Grant No. CCR-0210153.

[1] C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernstein, Nanotechnology **4**, 49 (1993).
[2] P. D. Tougaw and C. S. Lent, J. Appl. Phys. **75**, 1818 (1994).
[3] C. S. Lent, B. Isaksen, and M. Leiberman, J. Am. Chem. Soc. **125**, 1056 (2003).
[4] K. K. Likharev and A. N. Korotkov, Science **273**, 763 (1996).
[5] G. Toth and C. S. Lent, J. Appl. Phys. **85**, 2977 (1999).
[6] D. V. Averin and A. A. Odintsov, Phys. Lett. A **140**, 251 (1989).
[7] J. M. Martinis and M. Nahum, Phys. Rev. B **48**, 18316 (1993).
[8] H. Pothier, P. Lafarge, P. F. Orfila, C. Urbina, D. Esteve, and M. H. Devoret, Physica B **169**, 573 1991.
[9] T. A. Fulton, P. L. Gammel, and L. N. Dunkleberger, Phys. Rev. Lett. **67**, 3148 (1991).
[10] D. V. Averin and K. K. Likharev, in *Mesoscopic Phenomena in Solids*, edited by P. A. L. B. L. Altshuler and R. A. Webb, (Elsevier, Amsterdam, 1991), pp. 173-260.
[11] M. Covington, M. W. Keller, R. L. Kautz, and J. M. Martinis, Phys. Rev. Lett. **84**, 5192 (2000).
[12] M. W. Keller, J. M. Martinis, N. M. Zimmerman, and A. H. Steinbach, Appl. Phys. Lett. **69**, 1804 (1996).
[13] M. W. Keller, J. M. Martinis, and R. L. Kautz, Phys. Rev. Lett. **80**, 4530 (1998).
[14] R. L. Kautz, M. W. Keller, and J. M. Martinis, Phys. Rev. B **60**, 8199 (1999).
[15] V. A. Krupenin, S. V. Lotkhov, H. Scherer, T. Weimann, A. B. Zorin, F. J. Ahlers, J. Niemeyer, and H. Wolf, Phys. Rev. B **59**,

10778 (1999).
[16] R. L. Kautz, M. W. Keller, and J. M. Martinis, Phys. Rev. B **62**, 15888 (2000).
[17] X. Jehl, M. W. Keller, R. L. Kautz, J. Aumentado, and J. M. Martinis, Phys. Rev. B **67**, 165331 (2003).
[18] N. M. Zimmerman, E. Hourdakis, Y. Ono, A. Fujiwara, and Y. Takahashi, J. Appl. Phys. **96**, 5254 (2004).
[19] H. D. Jensen and J. M. Martinis, Phys. Rev. B **46**, 13407 (1992).
[20] P. D. Dresselhaus, L. Ji, S. Han, J. E. Lukens, and K. K. Likharev, Phys. Rev. Lett. **72**, 3226 (1994).
[21] V. A. Krupenin, S. V. Lotkhov, and D. E. Presnov, J. Exp. Theor. Phys. **84**, 190 (1997).
[22] R. K. Kummamuru, L. Mo, A. O. Orlov, C. S. Lent, G. H. Bernstein, and G. L. Snider, Microelectron. J. **36**, 304 (2005).
[23] S. V. Lotkhov, S. A. Bogoslovsky, A. B. Zorin, and J. Niemeyer, Appl. Phys. Lett. **78**, 946 (2001).
[24] N. M. Zimmerman and W. H. Huber, Proceedings of the Conference on Precision Electromagnetic Measurements Digest, IEEE, Sydney, NSW, Australia, 2000, pp. 14-15.
[25] J. M. Martinis, M. Nahum, and H. D. Jensen, Phys. Rev. Lett. **72**, 904 (1994).
[26] R. K. Kummamuru, A. O. Orlov, R. Ramasubramaniam, C. S. Lent, G. H. Bernstein, and G. L. Snider, IEEE Trans. Electron Devices **50**, 1906 (2003).
[27] A. A. Odintsov, V. Bubanja, and G. Schon, Phys. Rev. B **46**, 6875 (1992).
[28] D. S. Golubev and A. D. Zaikin, Phys. Lett. A **169**, 475 (1992).
[29] A. B. Zorin, S. V. Lotkhov, H. Zangerle, and J. Niemeyer, J. Appl. Phys. **88**, 2665 (2000).
[30] S. V. Lotkhov, H. Zangerle, A. B. Zorin, and J. Niemeyer, Appl. Phys. Lett. **75**, 2665 (1999).
[31] V. A. Krupenin, A. B. Zorin, M. N. Savvateev, D. E. Presnov, and J. Niemeyer, J. Appl. Phys. **90**, 2411 (2001).
[32] X. Luo, M. Tomcsanyi, A. O. Orlov, T. H. Kosel, and G. L. Snider, Appl. Phys. Lett. **89**, 043511 (2006).
[33] I. S. Beloborodov, A. V. Lopatin, V. M. Vinokur, and K. B. Efetov, Rev. Mod. Phys. **79**, 469 (2007).
[34] I. S. Beloborodov, A. V. Lopatin, and V. M. Vinokur, Phys. Rev. B **72**, 125121 (2005).
[35] X. Luo, A. O. Orlov, and G. L. Snider, J. Vac. Sci. Technol. B **22**, 3128 (2004).
[36] X. Luo, A. O. Orlov, and G. L. Snider, Microelectron. J. **36**, 308 (2005).
[37] T. A. Fulton and G. D. Dolan, Phys. Rev. Lett. **59**, 109 (1987).
[38] A. O. Orlov, R. K. Kummamuru, R. Ramasubramaniam, G. Toth, C. S. Lent, G. H. Bernstein, and G. L. Snider, Appl. Phys. Lett. **78**, 1625 (2001).
[39] A. O. Orlov, I. Amlani, R. K. Kummamuru, R. Ramasubramaniam, G. Toth, C. S. Lent, and G. H. Bernstein, Appl. Phys. Lett. **77**, 295 (2000).
[40] X. Luo, Ph.D. thesis, University of Notre Dame, 2005.
[41] A. O. Orlov, R. K. Kummamuru, J. Timler, C. S. Lent, G. L. Snider, and G. H. Bernstein, in *Mesoscopic Tunneling Devices*, edited by H. Nakashima (Research Signpost, Kerala, India, 2004), pp. 125-160.
[42] J. Zhang and B. I. Shklovskii, Phys. Rev. B **70**, 115317 (2004).
[43] D. M. Kaplan, V. A. Sverdlov, and K. K. Likharev, Phys. Rev. B **68**, 045321 (2003).
[44] I. S. Beloborodov, K. B. Efetov, A. V. Lopatin, and V. M. Vinokur, Phys. Rev. Lett. **91**, 246801 (2003).
[45] M. V. Feigel'man and A. S. Ioselevich, JETP Lett. **81**, 277 (2005).
[46] I. P. Zvyagin and R. Keiper, Philos. Mag. B **81**, 997 (2001).