Ultralarge area MOS tunnel devices for electron emission

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A comparative analysis of metal-oxide-semiconductor (MOS) capacitors by capacitance-voltage (*C-V*) and current-voltage (*I-V*) characteristics has been employed to characterize the thickness variations of the oxide on different length scales. Ultralarge area (1 cm^2) ultrathin (~5 nm oxide) MOS capacitors have been fabricated to investigate their functionality and the variations in oxide thickness, with the use as future electron emission devices as the goal. *I-V* characteristics show very low leakage current and excellent agreement to the Fowler-Nordheim expression for the current density. Oxide thicknesses have been extracted by fitting a model based on Fermi-Dirac statistics to the *C-V* characteristics. By plotting *I-V* characteristics in a Fowler plot, a measure of the thickness of the oxide can be extracted from the tunnel current. These apparent thicknesses show a high degree of correlation to thicknesses extracted from *C-V* characteristics on the same MOS capacitors, but are systematically lower in value. This offset between the thicknesses obtained by *C-V* characteristics and *I-V* characteristics is explained by an inherent variation of the oxide thickness. Comparison of MOS capacitors with different oxide areas ranging from 1 cm^2 to 10 μm^2, using the slope from Fowler-Nordheim plots of the *I-V* characteristics as a measure of the oxide thickness, points toward two length scales of oxide thickness variations being ~1 cm and ~10 μm, respectively.

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I. INTRODUCTION

Solid-state low energy electron emitters have a variety of potential application in science and technology. Several of such potential applications require inexpensive electron emitters.[1] Free electrons can be obtained by heating a filament and extracting electrons with a high voltage extractor. In many applications, the use of such a filament is a problem due to its size, the heat evolved, outgassing,[2] or the light emitted. It has been a goal for decades to be able to substitute these traditional electron sources with inexpensive compact silicon-based cold-cathode emitters.

Most on-chip electron emitters available today are based on the field effect type emitter structure. The field effect emitter has to be operated in vacuum, since it cannot withstand operation at high pressure due to the high fields involved. Another approach to achieve a semiconductor electron emitter is by using a metal-oxide-semiconductor (MOS) structure with an ultrathin oxide acting as a tunnel barrier.[3–5] Oxide film thicknesses on the nanometer scale allow electrons to tunnel from the semiconductor substrate into the top metal film. Applying a voltage larger than the work function of the metal film across such a structure will lead to electrons being emitted into vacuum[3,6,7] if the gate metal film is sufficiently thin. These devices work at low voltages (<10 V), low temperatures, and have a nearly pressure-independent emission.[8] The drawback compared to the field emitter is the low emission current density.

In order to increase the emission current, the area of the thin oxide forming the tunnel barrier must be enlarged. The great challenge of implementing MOS structures as electron emitters lies in the fabrication process, since it is extremely difficult to produce an ultrathin oxide film which is still electrically insulating and nearly defect-free over an ultralarge area, e.g., 1 cm^2. When scaling up the oxide area, the number of statistical defects leading to electric breakdown of the oxide increases dramatically,[9] which leads to a high probability of having a significant fraction of nonfunctional devices. This underlines the necessity of having a means to characterize large area oxides if these devices are to be successfully implemented in electronic devices.

The variation of oxide thickness is of great importance to large area electron emitters for several reasons. One reason is the breakdown of the oxide being of the weakest-link nature.[9] The number of weak points due to spots of thin oxide will scale with the area and, therefore, be more important the larger the oxide area is since breakdown in one of these weak spots is enough to render the whole oxide useless. Another reason is the exponential dependence of the tunneling current on the thickness. The average thickness of the device is, in this way, very important for the absolute brightness of the emission from the device. Furthermore, a variation in thickness will lead to "hot" and "cold" spots in the electron emission being a nuisance in applications where an even distribution of electrons is needed on a certain length scale.

Two possible, unique applications for MOS electron emitters are in electronic catalysis and hot electron emission lithography (HEEL).[10] It has previously been proposed by Gadzuk[11–14] that hot electrons injected from the substrate into the gate in metal-insulator-metal tunnel devices, and thus similar MOS based devices, can be used to enhance surface reactivity on the surface of the ultrathin gate metal. This phenomenon has been investigated experimentally by several groups.[15–19] In HEEL, a MOS electron emitter is used as a combined electron source and mask to illuminate an electron sensitive polymer resist.[10] The patterning is

achieved by forming the tunnel oxide or gate metal as a 1:1 mapping of the pattern to be transferred to the substrate. In this way, electron beam lithography can be combined with the massive parallelism known from standard UV lithography.

The MOS capacitor, being one of the most important components in very large scale integration technology as the heart in the field effect transistor (FET), has received a considerable amount of attention in the literature.[20] With regard to FET technology, the thickness variations of the oxide in the MOS structure are important in relation to fluctuations in threshold voltages and electrical breakdown of the oxide, leading to excessive power consumption[21] and possible malfunction. The oxide thickness variations have been characterized on a microscopic length scale by transmission electron microscope,[22] atomic force microscope,[22–24] and scanning tunneling microscope[22,25] measurements. These types of measurements yield valuable information on the micrometer length scale, which is relevant, for example, in FETs, but they do not give the full picture for large area MOS devices, where also longer length scales of variations in the oxide thickness might be important.

Our work is devoted to electronically promoted chemical phenomena, and the devices presented here have been developed to be a platform for delivering hot electrons to a metal surface from within. In this work, we report on the results of the characterization of ultralarge area (1 cm^2) MOS devices with ultrathin tunnel oxides by *I-V* and *C-V* characteristics. Insights into the oxide thickness variations across these large devices are extracted from a comparative analysis of obtained *C-V* and *I-V* characteristics, and are reported here.

Breakdown statistics[23,26–28] are, besides oxide thickness variations, one of the most important characteristics for ultralarge area MOS electron emitters employed in technological applications, but perhaps not as crucial in our future work of studying electronically promoted chemical phenomena. For this reason, we have not devoted serious attention to this aspect, even though we recognize its extreme importance in other applications.

II. EXPERIMENT

A. Fabrication of ultralarge area ultrathin metal-oxide-semiconductor capacitors

The MOS capacitors presented in this paper are fabricated in the cleanroom facilities at Danchip at the Technical University of Denmark. The wafers used are silicon wafers, fabricated by Okmetic, heavily doped with antimony ($\sim 3 \times 10^{18}$ cm^{-3}), resulting in a resistivity of <0.025 Ω cm. A thick oxide of 750 nm is grown by wet thermal oxidation at 1000 °C to serve as an underlayer for a contact pad for electrical measurement purposes. A wet-etch mask is formed by standard photolithography, and the thick oxide is etched back to the substrate in a standard buffered hydrofluoric acid solution to form the areas for the ultrathin tunnel oxide (SiO_2). The wafers are etched for 9 min continuously, and then inspected for a hydrophobic surface. If this has not been achieved, the wafers are etched in steps of 30 s until a hydrophobic Si surface is observed. It is critical to avoid overetching due to the risk of increasing the surface roughness.[29]

The resist is stripped and a standard RCA cleaning procedure[30] is performed. An ultrathin SiO_2 tunnel barrier is grown thermally in a dedicated ultraclean three-zone drive-in furnace at 800 °C in 1 atm of O_2 for 40 min, with a flow of 6 SLM (SLM denotes standard liters per minute). The oxide growth is followed by a 20 min anneal in 1 atm N_2 at 800 °C, with a flow of 6 SLM. Ti/Au (10/100 nm) gate electrodes are deposited using electron-beam physical vapor deposition (PVD), where Ti serves as a wetting layer. Finally, the native oxide is stripped from the backside of the wafer using a 5% HF solution, and a Ti/Au (10/100 nm) backside electrode is deposited using electron-beam PVD.

B. Measurements of the capacitance and current

Due to the large capacitance (~ 0.6 μF) in combination with a high tunneling current of the fabricated MOS capacitors, a special technique for measuring the capacitance-voltage (*C-V*) characteristics is adopted. The technique is designed to measure large capacitances and correct for current from parallel conductance due to tunneling. The capacitance is measured by the use of a switched analog integrator (Fig. 1).

The capacitance of a MOS capacitor can be obtained by applying a signal of the form shown in Fig. 2. For each voltage step in the *C-V* characteristics, a square voltage signal is applied to the MOS capacitor. The reason for using a square signal instead of a simple step is to be able to correct for the current signal due to tunneling electrons.

The voltage versus time signal on the integrator increases or decreases in steps when the MOS capacitor is charged or discharged as a consequence of the applied square voltage signal. In between each charging or discharging step, the integrator signal changes at a constant rate due to the current passing through the MOS capacitor (tunneling or leakage current). The voltages V_0, V_1, V_2, and V_4 are measured since there is no decaying charging or discharging current at these points which would otherwise influence the measurement. The signal from a constant current and charging or discharging of the MOS capacitor can be separated using the following procedure: V_0 is used as the reference zero, and V_1 is subtracted from V_4 to obtain V_3. The signal due to the capacitance of the MOS capacitor, V_C, is $V_2 - V_3$. From this voltage difference, the MOS capacitance is calculated as

$$C_{\mathrm{MOS}} = \frac{(V_2 - V_3)C_{\mathrm{ref}}}{\Delta V}, \tag{1}$$

where C_{ref} is the capacitance of the reference capacitor in the integrator and ΔV is the height of the square voltage signal. The current through the oxide of the MOS capacitor and any other leakage currents in the system during Δt are proportional to $V_T = V_3 - V_1$:

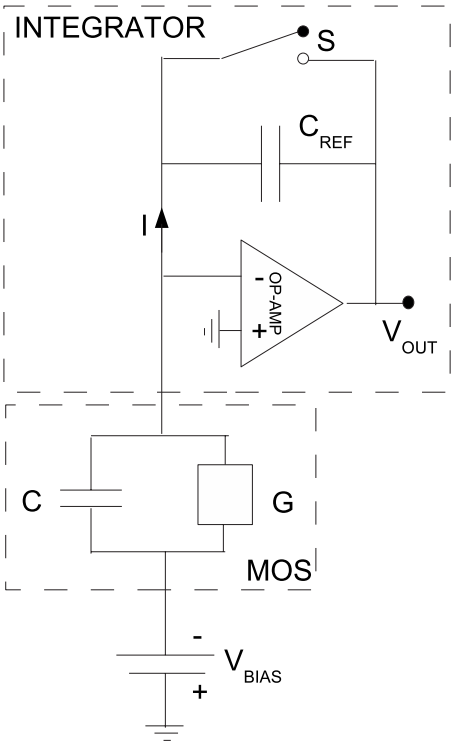

FIG. 1. Diagram of the analog integrator used to measure the *C-V* characteristics presented in this paper. The MOS capacitor under test is modeled as a capacitance C in parallel with a conductance G. The operational amplifier stores the charge flowing to and from the MOS capacitor on the reference capacitor C_{ref}. The switch S is used to reset the integrator before each measurement point. V_{bias} is the bias voltage applied to the MOS capacitor and V_{out} is the readout voltage of the integrator used to calculate the capacitance and current.

$$I_{\text{MOS}} = \frac{(V_3 - V_1)C_{\text{ref}}}{\Delta t}, \tag{2}$$

where Δt is the duration of the applied voltage pulse. In practice, the current is determined by integration of the current for a period of between 100 μs and 1 s at a constant voltage for better accuracy. Here, the current can be made up of any physical or electronic phenomena in the system such as oxide tunnel current, oxide leakage current, noise induced current, and amplifier bias current.

C. Instrumentation

The bias voltage was generated using a National Instruments PCIe-6259 DAQ card, where the current output was enhanced with a TI BUF634T high speed buffer enabling a maximum current of 250 mA continuously. The MOS capacitors were contacted using Accuprobe *Z*-adjustable probes with gold plated Be and/or Cu tips. The voltage output was measured at the output pin of the TI BUF634T to account for offset and nonunity gain.

The instrument has seven reference capacitors, each covering one decade (4.7 pF–47 μF), switched using standard reed relays. This combined with the variation of the integration time results in a theoretical dynamic range of 14 decades. In practice, this is limited to 11 decades due to the current limitation of the output amplifier (250 mA) and the noise level of the instrument (picoamperes).

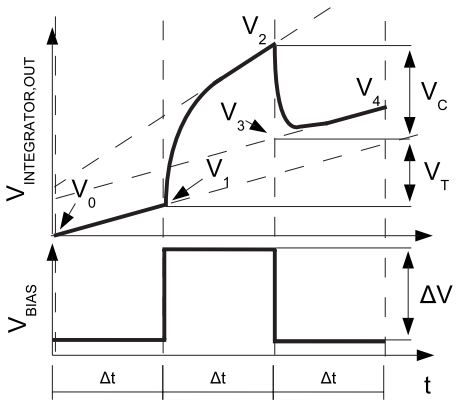

FIG. 2. A sketch of the applied square voltage signal which makes the MOS capacitor charge and discharge, and above, the resulting signal on the integrator. The MOS capacitor is equivalent to a capacitor in parallel with a conductor. The signal on the integrator can be divided into two parts: fast decaying charging and/or discharging signals from the capacitance, and constant increasing signals due to the current flowing through the MOS capacitor. By measuring the voltages V_0, V_1, V_2, and V_4, the current and capacitance of the MOS capacitor can be obtained as explained in the text.

I-V characteristics were also measured using a Keithley 485 ampere meter with a dynamical range from 0.1 pA to 2 mA.

D. Extraction of the oxide thickness

From the *C-V* characteristics, the oxide capacitance is extracted from the total capacitance of the MOS capacitor by fitting it to the exact solution to Poisson's equation for the system using Fermi-Dirac statistics for the electrons in the semiconductor. It is important to use Fermi-Dirac statistics for this system due to the high dopant concentration in the silicon wafers used and due to the very high surface field. Using Boltzmann instead of Fermi-Dirac statistics typically returned 1 Å higher values for the thickness of the oxides. Since the *C-V* characteristics are obtained at high frequency, interface traps are neglected in the extraction of the oxide thickness. The model assumes spatially constant dopant impurity concentration, and interface traps and minority carrier capacitances are neglected. This model, known as the McNutt-Sah-Walstra algorithm, has earlier been used as the benchmark for five other *C-V* oxide thickness extraction algorithms by Walstra and Sah.[31] In addition to fitting the thickness, we also allow for a variation in the dopant concentration to circumvent any misleading changes in the oxide thickness from variations in dopant concentration, which could give rise to changes in the semiconductor capacitance in series with the oxide capacitance.

The oxide thickness is calculated from the oxide capacitance as[32]

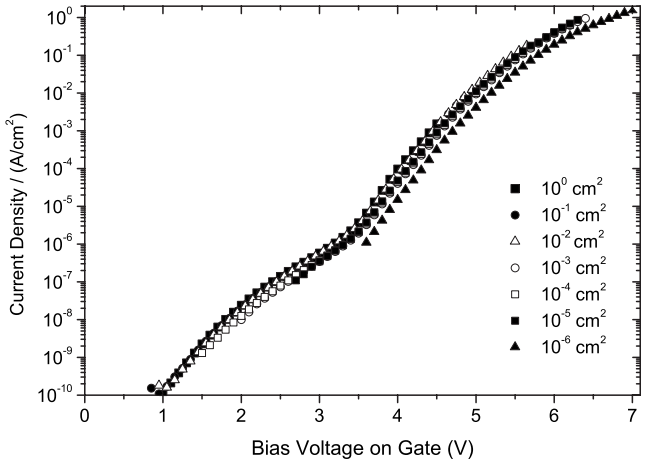

FIG. 3. The current density as a function of gate voltage for seven MOS devices, with oxide areas ranging from 10^{-6} to 1 cm^2. The reason for the different voltage range of measurements on different area devices is the dynamical range of the ammeter.

$$X_{\mathrm{ox}} = \frac{\epsilon_0 \epsilon_{\mathrm{ox}} A}{C_{\mathrm{ox}}}, \tag{3}$$

where ϵ_0 is the permittivity of vacuum, ϵ_{ox} is the relative dielectric constant of the oxide (SiO_2:3.9), A is the MOS capacitor area, and X_{ox} is the oxide thickness.

III. RESULTS

The results presented here are measured on MOS capacitors on wafers from a single batch. This means that when parallel processing was possible, all wafers were processed in the same run. The MOS capacitors are enumerated according to host wafer and position on same, e.g., W24D02, where W24 is the wafer and D02 is the MOS capacitor.

In Fig. 3, *I-V* characteristics from MOS capacitors with oxide areas ranging from 100 μm^2 to 1 cm^2 with an increment in area of a decade are shown. The current is scaled with area to show the current density. It is seen that the six larger devices have similar current densities, while the smallest device lies a factor of 2–3 lower.

In Fig. 4, the *I-V* characteristics of a range of different 1 cm^2 area MOS capacitors are shown. The MOS capacitors measured are from four different wafers, but with several MOS capacitors from each wafer shown. The oxide thickness measured by ellipsommetry on each wafer is shown in parentheses after each wafer number. The oxide thickness extracted from *C-V* characteristics is shown after the number designating each MOS capacitor. From Fig. 4, it is seen that the thicknesses extracted from *C-V* characteristics and the relative position of the *I-V* characteristics show systematically and qualitatively good agreement. There is a variation in the oxide thickness between different wafers, but also between different MOS capacitors on the same wafer. Figure 4 shows a variation of typically 5 Å in oxide thickness on single wafers, and up to 15 Å from wafer to wafer. Variation in substrate dopant concentration is known to affect oxidation rates,[33,34] which can explain variations in oxide thickness.

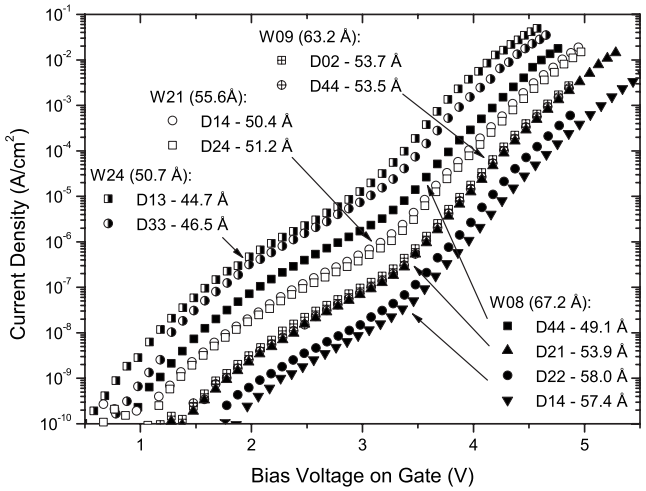

FIG. 4. Measured *I-V* characteristics of ten devices from four wafers, all with an oxide area of 1 cm^2. The oxide thickness measured by ellipsommetry measured on each wafer is shown in parentheses. There is a spread in the oxide thickness between devices, but the thickness extracted from *C-V* measurements agrees qualitatively well with the relative positions of the *I-V* characteristics and the thickness implied therefrom.

IV. DISCUSSION

A. Functionality of ultralarge area oxides

With the general motivation for creating ultralarge area, high current electron emitters in mind, it is important to determine the transport mechanism of the electrons through the oxide. In order to have electron emission, the electrons must have an energy equal to or higher than the work function of the gate metal. This kind of extreme electron heating can only occur if the electrons are tunneling through the oxide. To verify the tunnel nature of the electron transport through the oxide, the higher bias part ($\gtrsim$3.4 V) of the *I-V* characteristics is compared to the Fowler-Nordheim[35–37] (FN) model for the current density:

$$J_{\mathrm{FN}} = A F_{\mathrm{ox}}^2 \exp\left(-\frac{B}{F_{\mathrm{ox}}}\right), \tag{4}$$

where F_{ox} is the electric field in the oxide given by $F_{\mathrm{ox}} = \frac{V_{\mathrm{ox}}}{X_{\mathrm{ox}}}$; A and B are constants given by

$$A = \frac{e^3}{16\pi^2\hbar}\frac{m_{\mathrm{Si}}}{\phi_B m_{\mathrm{ox}}} \text{ and } B = \frac{4}{3}\frac{\sqrt{2m_{\mathrm{ox}}}}{e\hbar}\phi_B^{3/2}, \tag{5}$$

where e is the electron charge, $\hbar$ is the reduced Planck's constant, m_{Si} is the effective electron mass in silicon, m_{ox} is the effective electron mass in the oxide, and ϕ_B is the barrier height for electron tunneling, given by the difference between the Fermi level in the semiconductor and the conduction band edge of the insulator.

The model can be rewritten so as to yield a mean to linearize the *I-V* characteristics:

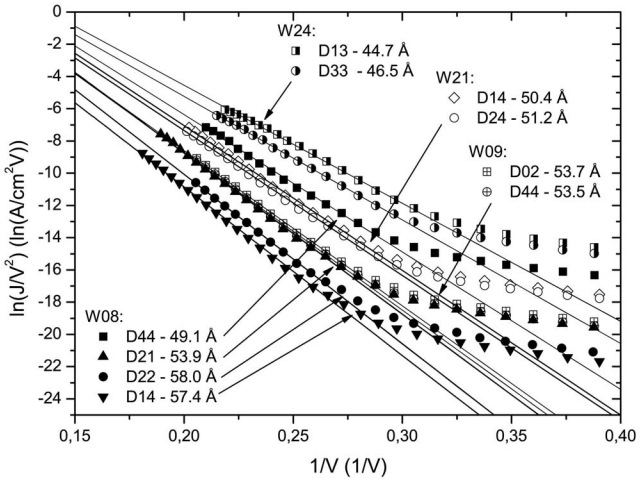

FIG. 5. The *I-V* characteristics from Fig. 4 shown in a Fowler plot. The data yield straight lines in the Fowler-Nordheim regime above 3.4 V, corresponding to ~0.29 on the inverse voltage axis. The slope of the Fowler-Nordheim fit should be proportional to the thickness, as seen from Eq. (6).

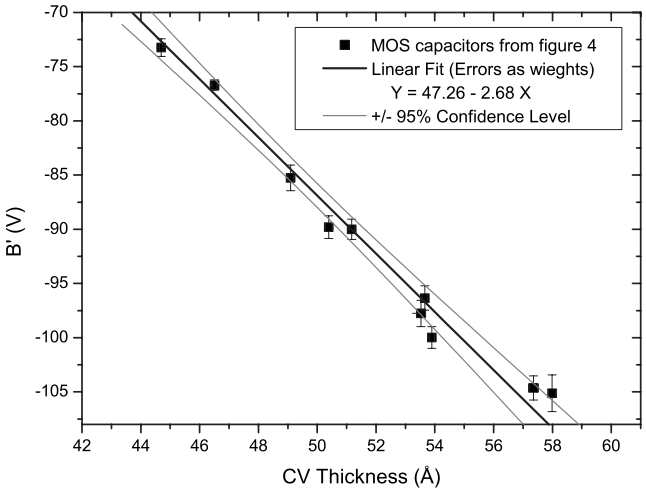

FIG. 6. The extracted slope from fits to the Fowler-Nordheim model (B') plotted against the oxide thickness extracted from *C-V* characteristics on the same devices.

$$\ln\left(\frac{J}{V_{\mathrm{ox}}^2}\right) = \ln(A') - \frac{B'}{V_{\mathrm{ox}}}, \tag{6}$$

where $A' = \frac{A}{X_{\mathrm{ox}}^2}$ and $B' = BX_{\mathrm{ox}}$.

The *I-V* characteristics from Fig. 4 are shown as Fowler plots, using Eq. (6), in Fig. 5. The *I-V* characteristics fit the Fowler-Nordheim model very well above a bias voltage of ~3.4 V, which matches well the sum of typical values for the flatband (FB) voltage $eV_{\mathrm{FB}} = \Phi_{\mathrm{Ti}} - \Phi_{\mathrm{Si}} \approx 4.3\ \mathrm{eV} - 4.1\ \mathrm{eV} = 0.2\ \mathrm{eV}$ and the tunnel barrier height $\phi_B \sim 3.2$ eV.[38]

B. Variations in the oxide thickness

A significant variation of the oxide thickness between devices and certainly from wafer to wafer is observed using *C-V* characteristics, but also more qualitatively from the *I-V* characteristics (Fig. 4) and again quantitatively from the slopes of the Fowler plots in Fig. 5.

From Fig. 4, it can be seen that there is a systematic relation between the thickness measured by *C-V* measurements and the apparent thickness in the *I-V* measurement. In order to quantify this further, the slopes extracted from the Fowler plot in Fig. 5 are plotted against the thicknesses derived from the *C-V* measurements of the same 1 cm^2 MOS capacitors in Fig. 6. From Eq. (6), it is seen that the slope (B') is directly proportional to the thickness of the oxide X_{ox} and would, therefore, be expected to yield a straight line intercepting the origin (0,0) when plotted against the thicknesses extracted from *C-V* measurements. As seen from Fig. 6, plotting B' against the thicknesses extracted from *C-V* measurements yields a straight line, but it does not intercept the origin when extrapolated. The oxide will not be completely flat, but will have a certain roughness and thickness variation from fabrication. A roughness or oxide thickness variation is weighted as $\frac{1}{X_{\mathrm{ox}}}$ in the *C-V* measurement, as seen from Eq. (3), but weighted as $\exp(-X_{\mathrm{ox}})$ in the *I-V* measurement, from which B' is extracted. As a direct consequence of those two different nonlinear weighings, the FN slopes (B') and the thickness probed by the *I-V* measurements will appear thinner than in the corresponding *C-V* measurements. From the fact that the *I-V* measurements give thinner areas exponentially more weight than areas with relatively thicker oxide, the offset in Fig. 6 can be explained by a thickness variation in the oxide. The characteristic length scale of the thickness variation must be on the order of 1 cm or larger, since the oxide thickness variations are clearly not averaged out in measurements on the square (1 cm^2) MOS capacitors.

In Fig. 7, the relative offset of the slope extracted from a Fowler plot is plotted against the nominal area of the devices for four series of devices. A series contains seven devices from 1 to 10^{-6} cm^2 in oxide area, situated close to each other on the same wafer. Since the slope of the Fowler plot is proportional to the thickness [see Eq. (5)] the relative offsets can be interpreted as relative differences in thickness. From Fig. 7, it is seen that there is a typical variation in thickness of ~3%, which for a 50–60 Å thick oxide corresponds to ~2 Å. The thicknesses of the smallest MOS capacitors (10^{-6} cm^2) are significantly larger than those of the larger area MOS capacitors.

The larger apparent thickness of the smallest oxide area MOS capacitors can be understood as a consequence of the variation in oxide thickness. In the simplest model, the thickness variation with a certain length scale is considered in two extreme regimes of MOS capacitor oxide areas. In the first regime, an area of oxide that is far larger than the length scale of the oxide thickness variation is considered. In this situation, an *I-V* measurement samples the entire distribution of oxide thicknesses, and each is weighted exponentially with regard to the thickness, and the total current is the surface integral of the current from each part of the thickness distribution:

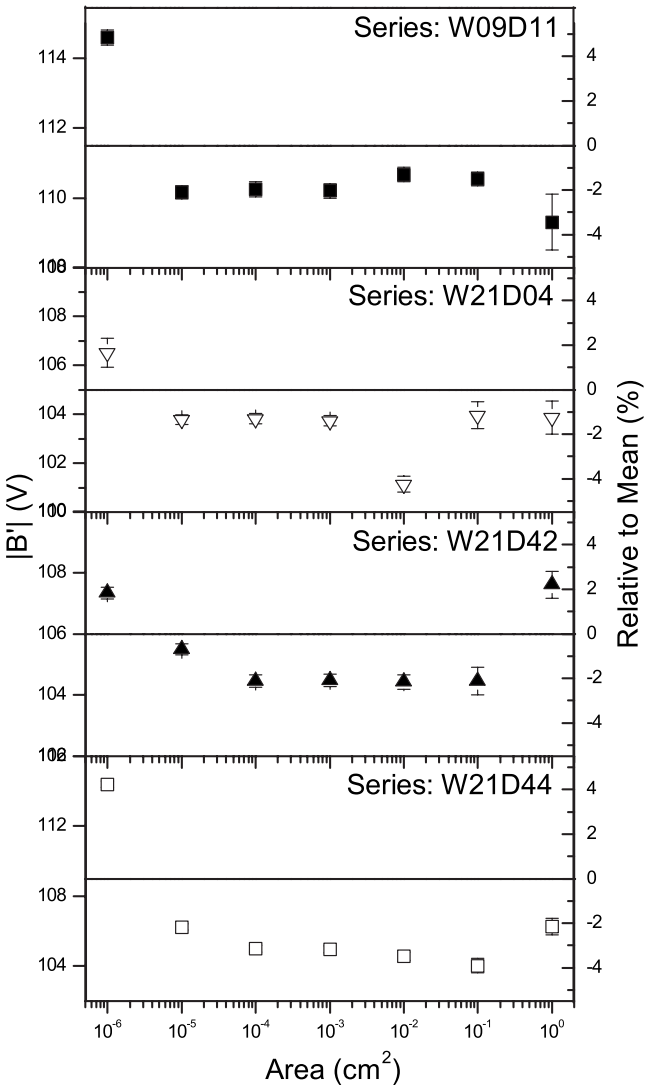

FIG. 7. Slopes (B') extracted from Fowler plots for four series of MOS capacitor, each series includes seven MOS capacitors of increasing area. The left axis shows the absolute value of the slopes, which are proportional to the oxide thickness. The right axis shows the relative deviation of each slope compared to the mean of each series. The error bars express the standard deviation of each slope value from the linear fit to the data plotted in a Fowler plot, not the statistical variation in oxide thickness for a particular MOS capacitor area.

$$I_{\text{tot}} = \int J_{\text{FN}}(X_{\text{ox}}(x,y))dA, \tag{7}$$

where I_{tot} is the total current of the MOS capacitor and $J_{\text{FN}}(X_{\text{ox}}(x,y))$ is the Fowler-Nordheim current density of a part of the oxide, with the thickness X_{ox} situated at (x,y). The current is integrated over the entire oxide area.

In the opposite extreme, the area of the MOS capacitor is very small compared to the length scale of the roughness or thickness variation; in this case, an *I-V* measurement samples one thickness of oxide and the *I-V* measurements for a series of MOS capacitors yield a distribution of current densities reflecting the variation in oxide thickness. Due to the exponential weighting by the tunnel current, the thicknesses extracted from the *I-V* measurements will be lower than the arithmetic mean of the distribution of oxide thicknesses present in the area sampled. Therefore, depending on the exact nature of the oxide thickness variation distribution, there will always be a larger probability of finding a larger than a smaller thickness of the smaller MOS capacitors compared to the larger MOS capacitors.

Taking an oxide thickness variation and an accompanying characteristic length scale into account make Fig. 7 relatively straightforward to interpret as expressing variations in oxide thicknesses with a characteristic length scale being ~ 10 μm. Another explanation for the larger apparent thickness of the smallest area (100 μm^2) MOS capacitors could be an edge effect arising from the fabrication technique, where back etching of a thick wet oxide to the Si substrate defines the area of the MOS capacitor as described in Sec. II A. In this case, one has to remember that the FN slope (B') is not directly dependent on the area of the MOS capacitor, but only indirectly through the integration of the current distribution [Eq. (7)].

The fact that the FN slope (B') is independent of area and no assumptions of the tunneling parameters, such as barrier height (ϕ_B) and effective electron mass in the oxide (m_{ox}), have been made makes this method of characterization very robust.

V. CONCLUSION

MOS devices with ultralarge area (1 cm^2) and ultrathin oxides ($\sim$5 nm) have been fabricated and characterized electrically by *C-V* and *I-V* measurements. The oxide thickness has been extracted from *C-V* characteristics by fitting to a model incorporating band bending and Fermi-Dirac statistics. The thicknesses obtained are realistic from an absolute perspective, by comparing with ellipsommetry, and they show qualitatively and systematically good agreement with the *I-V* characteristics. The thicknesses extracted from *C-V* characteristics as well as the *I-V* characteristics show a significant variation in the oxide thickness between MOS capacitors on the same wafer as well as between wafers. The spread in thicknesses measured on a single wafer is $\sim$5 Å, while between wafers it is $\sim$15 Å. The *I-V* characteristics of the MOS capacitors fit the Fowler-Nordheim model well in the region where the model is applicable, which is a strong evidence for the tunnel transport mechanism being dominant, and indicates that the MOS capacitors will work as electron emitters with a thinner gate metal layer. The *I-V* characteristics for the 1 cm^2 MOS capacitors are comparable to those with smaller oxide areas (10^{-1}–10^{-6} cm^2). The smallest area MOS capacitors are significantly different from the others, which is well explained by the variation of the oxide thickness on a length scale comparable to the side length of these. The slopes extracted from Fowler plots give a different method of characterizing the oxide thickness and, when comparing several orders of magnitude of area, also a good quantitative measure of the oxide thickness variations and the characteristic length scales of these. For the MOS capacitors

fabricated in this work, two length scales of importance, namely $\sim 10\ \mu$m and ~ 1 cm, were found. Of course, the data presented here are just a few samples of statistical phenomena and it is, therefore, not possible to conclude on the exact nature of the oxide thickness variations. It would be very interesting to see more elaborate studies of oxide thickness variations using slopes extracted from Fowler plots to gain information on the thickness variation of ultrathin oxides.

With regards to the motivation for the fabrication of ultralarge area electron emitters and the issues of oxide thickness variation discussed in the Introduction, there might be a problem with the large variation of thicknesses that is seen between different and across single large area MOS capacitors, since this can easily lead to a large difference in current density both between devices and from one side of a device to the other. These thickness variations might be improved upon by implementing alternative oxide growth methods and annealing, or, perhaps, by using alternative insulating materials for tunnel barriers.

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[1] N. S. Xu and S. E. Huq, Mater. Sci. Eng., R. **48**, 47 (2005).
[2] B. R. F. Kendall, J. Vac. Sci. Technol. A **17**, 2041 (1999).
[3] J. Cohen, J. Appl. Phys. **33**, 1999 (1962).
[4] J. Cohen, Appl. Phys. Lett. **1**, 61 (1962).
[5] T. Sumiya, H. Fujinuma, T. Miura, and S. Tanaka, Appl. Surf. Sci. **130–132**, 36 (1998).
[6] D. J. DiMaria, M. V. Fischetti, J. Batey, L. Dori, E. Tierney, and J. Stasiak, Phys. Rev. Lett. **57**, 3213 (1986).
[7] S. D. Brorson, D. J. DiMaria, M. V. Fischetti, F. L. Pesavento, P. M. Solomon, and D. W. Wong, J. Appl. Phys. **58**, 1302 (1985).
[8] H. Mimura, Y. Neo, H. Shimawaki, T. Matsumoto, and K. Yokoo, Appl. Surf. Sci. **144**, 498 (2005).
[9] E. Y. Wu and J. Sune, Microelectron. Reliab. **45**, 1809 (2005).
[10] M. Poppeller, E. Cartier, and R. M. Tromp, Microelectron. Eng. **46**, 183 (1999).
[11] J. W. Gadzuk, Phys. Rev. Lett. **76**, 4234 (1996).
[12] J. W. Gadzuk, J. Vac. Sci. Technol. A **15** 1520 (1997).
[13] J. W. Gadzuk, Phys. Rev. B **44**, 13466 (1991).
[14] J. W. Gadzuk and C. W. Clark, J. Chem. Phys. **91**, 3174 (1989).
[15] D. Diesing, G. Kritzler, M. Stermann, D. Nolting, and A. Otto, J. Solid State Electrochem. **7**, 389 (2003).
[16] T. Wadayama, A. Kojim, and A. Hatta, Appl. Phys. A: Mater. Sci. Process. **79**, 1891 (2004).
[17] D. Diesing, H. Janssen, and A. Otto, Surf. Sci. **331–333**, 289 (1995).
[18] R. G. Sharpe, S. J. Dixon-Warren, P. J. Durston, and R. Palmer, Chem. Phys. Lett. **234**, 354 (1995).
[19] T. Wadayama and M. Yokawa, Chem. Phys. Lett. **428**, 348 (2006).
[20] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley, New York, 1982).
[21] M. Hirose, M. Koh, W. Mizubayashi, H. Murakami, K. Shibahara, and S. Miyazaki, Semicond. Sci. Technol. **15**, 485 (2000).
[22] P. Mur *et al.*, Appl. Surf. Sci. **175–176**, 726 (2001).
[23] M. Houssa, T. Nigam, P. W. Mertens, and M. M. Heyns, Solid-State Electron. **43**, 159 (1999).
[24] O. Maida, H. Yamamoto, N. Okada, T. Kanashima, and M. Okuyama, Appl. Surf. Sci. **130–132**, 214 (1998).
[25] A. Crossley, C. J. Sofield, J. P. Goff, A. C. I. Lake, M. T. Hutchings, and A. Menelle, J. Non-Cryst. Solids **187**, 221 (1995a).
[26] S. Lombardo, J. H. Stathis, B. P. Linder, T. Watson, K. L. Pey, F. Palumbo, and C. H. Tung, J. Appl. Phys. **98**, 121301 (2005).
[27] B. P. Linder and J. H. Stathis, Microelectron. Eng. **72**, 24 (2004).
[28] J. Verweij and J. Klootwijk, Microelectron. J. **27**, 611 (1996).
[29] A. Crossley, C. J. Sofield, J. P. Goff, A. C. I. Lake, M. T. Hutchings, and A. Menelle, J. Non-Cryst. Solids **187**, 221 (1995b).
[30] W. Kern, *Handbook of Semiconductor Wafer Cleaning Technology—Science, Technology, and Applications* (Noyes, New York, 1993).
[31] S. V. Walstra and C.-T. Sah, IEEE Trans. Electron Devices **44**, 1136 (1997).
[32] E. Vincent, G. Ghibaudo, G. Morin, and C. Papadas, Proceedings of the IEEE International Conference on Microelectronic Test Structures, Monterey, CA, 1997 (unpublished), pp. 105–110.
[33] C. P. Ho and J. D. Plummer, J. Electrochem. Soc. **126**, 1516 (1979).
[34] C. P. Ho and J. D. Plummer, J. Electrochem. Soc. **126**, 1523 (1979).
[35] R. H. Fowler and L. W. Nordheim, Proc. R. Soc. London, Ser. A **119**, 173 (1928).
[36] M. Lenzlinger and E. H. Snow, J. Appl. Phys. **40**, 278 (1969).
[37] Z. Weinberg, J. Appl. Phys. **53**, 5052 (1982).
[38] H. C. Card, Solid State Commun. **14**, 1011 (1974).