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Electronic properties of atomically abrupt tunnel junctions in silicon

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We explore the influence of atomically sharp phosphorus doping profiles in laterally patterned tunnel junctions in crystalline silicon on the electronic transport properties at low temperatures. Atomically precise patterning is realized using scanning-tunneling-microscope-based hydrogen lithography in combination with low-temperature Si growth by molecular beam epitaxy. We show the conductance modulation of a 48-nm tunnel gap with a barrier height of 0.5 meV and highlight how such devices can act as sensitive charge sensors.

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The versatility of the scanning tunneling microscope (STM) for imaging and manipulating matter at the atomic scale has sparked interest for its use in the creation of atomically precise devices in Si.[1–4] Recently our group has overcome the challenge of reliably making electrical contact to buried, STM-patterned dopants in silicon once they are removed from the ultrahigh-vacuum environment.[3,5] This has resulted in the fabrication of highly conducting, planar P-doped nanowires with widths down to ~8 nm that still exhibit Ohmic behavior.[6]

As commercial silicon devices continue to downscale in size, the use of scanning probes and molecular beam epitaxy (MBE) has been highlighted as a means to investigate key requirements for the semiconductor industry including atomically sharp dopant profiles,[7] atomically smooth interfaces,[8] and exact dopant placement.[9] An important step toward the goal of using atomically precise dopant profiles in device architectures is to understand the nature of the electrical barrier formed between two highly doped, planar P-doped regions patterned with atomic precision. Such an understanding is essential before we can develop more complex devices, such as single electron transistors (SETs),[10] resonant tunneling diodes,[11] ordered dopant arrays,[12] and single or coupled planar quantum dots.[13]

In principle, lateral nanoscale tunnel junctions in a semiconductor environment can be realized using more conventional techniques, such as ion implantation.[14] However, even at low implant energies down to 14 keV, the lateral and longitudinal straggle is typically 8 and 11 nm, respectively, meaning that such devices are neither atomically precise nor planar. It is well known that the lateral extent of the donor electron wave function in silicon is given by the Bohr radius a_B,

$$a_B = \frac{4\pi\epsilon_s\hbar^2}{m^* e^2} \approx 3 \text{ nm}, \tag{1}$$

where m^* is the effective mass. It should therefore be possible to realize electrical barriers between doped regions if the width of the gap between them is much larger than the Bohr radius. While atomically abrupt barriers or junctions down to ~10 nm have been discussed theoretically,[2] tunneling between atomically abrupt laterally doped regions in silicon has not been demonstrated to date. For this purpose we present a detailed study of the tunneling characteristics of a 48-nm planar, atomically sharp P-doped $[n^{++}/n/n^{++}]$ tunnel junction STM-patterned on a lightly P-doped Si substrate (10^{15} cm^{-3}). By cooling the substrate with an applied bias, we demonstrate modulation of the conductance across the gap, and from temperature-dependent *I-V* measurements, we extract a tunnel barrier of 0.5 meV between the Si:P leads. Finally, we demonstrate how such an atomically precise junction can be used as a sensitive charge detector.

Figure 1(a) shows a schematic of the device architecture used to lithographically define the dopants within the two-dimensional (2D) plane. The black areas define the regions where a hydrogen resist on the Si(100) 2×1 surface has been desorbed to pattern the inner tunnel junction region separated by a gap of 48 nm together with two sets of large-area regions consisting of (i) a 300×680 nm^2 region used to extend to the (ii) 3.5×2 μm^2 large-area contact region. The narrowest separation between doped regions is a channel of

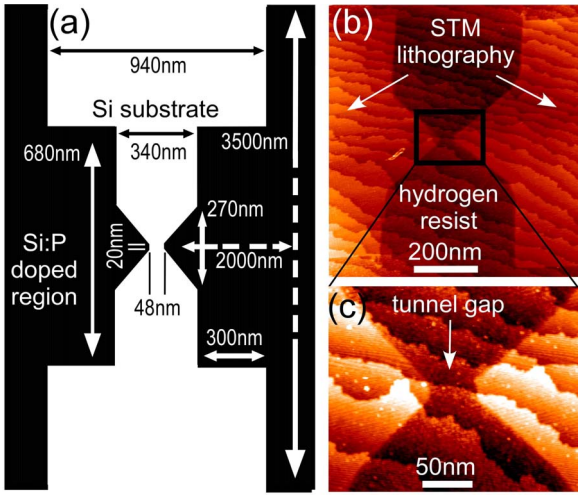

FIG. 1. (Color online) STM-patterned highly planar, atomically abrupt P-doped Si tunnel junction. (a) Device schematic (not to scale) with exact dimensions showing the central tunnel gap extending out to micron-sized contact regions. (b) Filled-state STM image (bias −2.2 V) of the device with small side extensions to large-area contact regions. Note that the large-area contact regions (3.5×2 μm^2) are not shown. (c) High-resolution STM image (bias −2.2 V) of the 48-nm tunneling gap.

Si substrate which is 48 nm long and 20 nm wide forming the tunnel junction. Figure 1(b) shows a filled-state STM image of the tunnel gap region on the H:Si(100) surface after STM lithography. We can see the underlying terrace structure of the surface with ~24 atomic steps. The brighter regions, superimposed on the natural step structure, correspond to areas where the hydrogen resist has been desorbed exposing the dangling bonds.[15] Figure 1(c) shows a magnified view of the central region of the tunnel gap, highlighting the sharp lithographic boundaries achieved.

After hydrogen lithography, the sample is exposed to phosphine gas which only adsorbs[16] to the exposed dangling bonds in the source-drain regions. A critical anneal[9] incorporates the P atoms into the silicon surface with a high doping density of 1.7×10^{14} cm^{-2}. *In situ* device encapsulation with epitaxial silicon at 250 °C (Refs. 17 and 18) limits P dopant segregation to ~0.6 nm.[19] Finally, electrical contact is achieved after removal from the ultrahigh vacuum system by alignment of surface Al contacts to the buried device in a four-terminal configuration. In addition, control devices are made on the same chip where Al contacts are annealed down to regions that have not been patterned by the STM. Such devices should contain no deliberately patterned P atoms and can be used to test at what temperature the lightly P-doped Si substrate (~10^{15} cm^{-3}) starts to conduct. Electrical measurements were performed from 1.5 to 35 K. Direct-current *I-V* characteristics were measured with a Keithley 236 Source-Measure unit. Standard lock-in techniques were also used to measure the differential conductance using a lock-in frequency of 77 Hz with an ac excitation voltage of 50 μV.

Before electrically characterizing the central tunnel gap region, we first ensure that we have good Ohmic contact to the large outer (3.5×2 μm^2) buried 2D Si:P contact regions, shown at the edges of Fig. 1(a). In Fig. 2(a), we show the two-terminal dc *I-V* characteristics of the 2D Si:P contact regions (1-3) and (2-4). Both sides exhibit linear, Ohmic behavior with two terminal resistances of 40 kΩ (1-3) and 4 kΩ (2-4), respectively. However, despite showing Ohmic behavior there is a clear difference in the two resistances either side of the tunnel gap. This arises due to the different extent of overlap between the buried P-doped contact regions and the corresponding surface aluminum leads due to limited alignment[5] achieved using the etched registration markers. The *I-V* characteristics of these contact regions have been tested under different cooldowns and under different experimental conditions, such as applying a source-drain bias across the junction or after we have induced gate leakage from a metal plane located 300 μm away at the backside of the substrate. In all cases the *I-V* characteristics remain the same, highlighting that they are robust forming good electrical contact to the device. Second using the control devices, we first confirm that at 4 K, charge carriers in the Si substrate (with a bulk P background doping of ~10^{15} cm^{-3}) are frozen out; i.e., no current flow occurs between the surface contacts.

We now turn our attention to the *I-V* characteristics of the contact regions across the junction using a four-terminal measurement configuration to eliminate the influence of contact resistances. Figure 2(b) shows nonlinear *I-V* characteristics across the junction [red (light gray) trace] where tunneling occurs through the barrier formed by the insulating substrate between the two tapered, highly doped Si:P regions. As we increase the source-drain bias, we observe a monotonic increase in differential conductance, resulting in a larger tunnel current caused by the higher charge carrier energy at higher biases with respect to the tunnel barrier. The four-terminal nature of our device allows us to exclude poor electrical contacts as the origin of the observed nonlinear behavior.

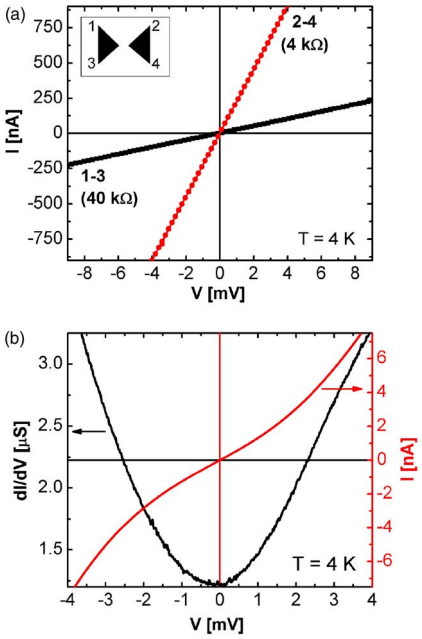

FIG. 2. (Color online) Electrical characterization of the tunnel junction. (a) *I-V* characteristics of the P-doped contact regions show linear behavior with two terminal resistances of 4 and 40 kΩ between left and right contact patches. (b) Four-terminal differential conductance of the 48-nm atomically abrupt tunnel junction (black) and the red (light gray) integrated *I-V* curve demonstrating nonlinear behavior.

The linear *I-V* characteristics seen in Fig. 2(a) unequivocally confirm that the nonlinear *I-V* behavior originates from the STM-patterned tunnel junction. Measurement of the differential conductance allows a more sensitive characterization of the tunnel junction. Figure 2(b) shows the differential conductance at large negative source-drain voltages decreasing to a minimum at zero source-drain voltage, before increasing again at large positive source-drain voltages (black curve). It is important to note that the differential conductance shows no sign of jumps, random telegraph signals, or evidence of resonant tunneling.[11,20,21] This indicates that the substrate between the Si:P source-drain leads provides a stable potential landscape with the absence of any active charge traps, which would give rise to tunnel resonances. Mesoscopic devices are extremely sensitive to the local potential landscape which the system adopts upon cooling. Dislocations, charge traps, and dopant charge states may all contribute to variation in device characteristics. We found the differential conductance characteristics of the device were reproducible to within 30% variation (over a source-drain bias of 4 mV) during many thermal cycles. Both the high

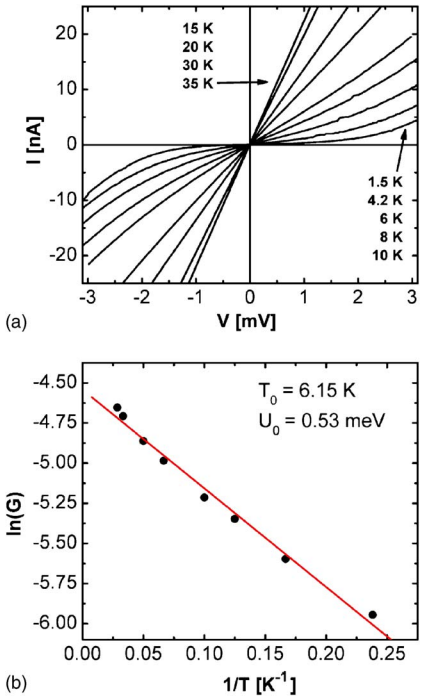

FIG. 3. (Color online) Determination of the tunnel barrier height. (a) Temperature-dependent *I-V* characteristics of the tunnel gap between 1.5 and 35 K. (b) The Arrhenius fit to the conductance (solid line) extracts a tunnel barrier of U_0=0.5 meV.

level of reproducibility and the absence of resonances are of great significance for the fabrication and interpretation of more sophisticated devices aimed at the study of single-electron effects. Using temperature-dependent *I-V* measurements, we extrapolate the height of the tunnel barrier.

Figure 3(a) shows the *I-V* characteristics of the device at various temperatures ranging from 1.5 to 35 K. Nonlinear behavior is maintained up to a temperature around 35 K at which point Ohmic conduction is observed. From the control device, we independently determined that the substrate only starts to conduct at temperatures >40 K. Therefore the results presented in Fig. 3 represent the activated behavior across the tunnel gap. The logarithm of the zero-bias conductance is plotted against inverse temperature in Fig. 3(b). Fitting the Arrhenius law for simple activated conduction to the temperature-dependent conductance, we obtain an activation energy of $U_0 \sim 0.5$ meV (corresponding to a characteristic temperature of T_0=6.15 K). The height of the tunnel barrier is determined by a number of factors including the planar device geometry, the doping density of the source-drain leads, and the substrate background doping in the insulating Si region. One way to alter the height of the tunnel barrier is to cool the device from room temperature below the substrate conduction threshold with a bias applied to the substrate.[22] As a result, the applied potential is frozen into the substrate. This technique has recently been applied to gated GaAs/$Al_xGa_{1-x}As$ (Ref. 22) structures to reduce gate-induced noise by electrically saturating charge traps and impurities in the vicinity of the gate. It has also been used to change the channel conductance in silicon inversion layers.[23] Applying a positive (negative) bias effectively increases (depletes) the carrier concentration in the silicon substrate region between the ultrahigh P-doped contact regions. Due to the high doping level and Fermi level pinning in the source-drain leads, bias cooling affects the substrate potential much more than the P-doped STM-patterned source-drain regions. Consequently, the barrier potential can be manipulated by application of different bias voltages.

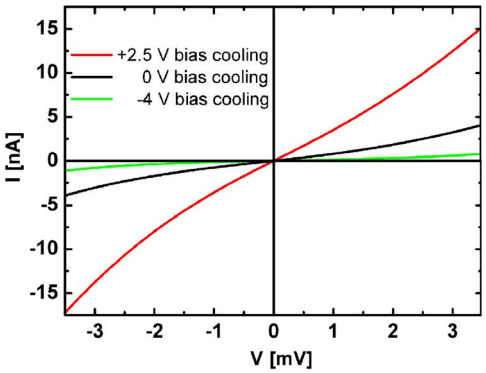

FIG. 4. (Color online) Bias-dependent substrate cooling as a means of tuning the tunnel barrier height demonstrated for three separate cooldowns with substrate biases of +2.5 V, −4 V, and 0 V, respectively.

From Fig. 4, we see that bias cooling with a substrate potential of +2.5 V increases device conductance fourfold whereas a bias of −4 V decreases conductance threefold

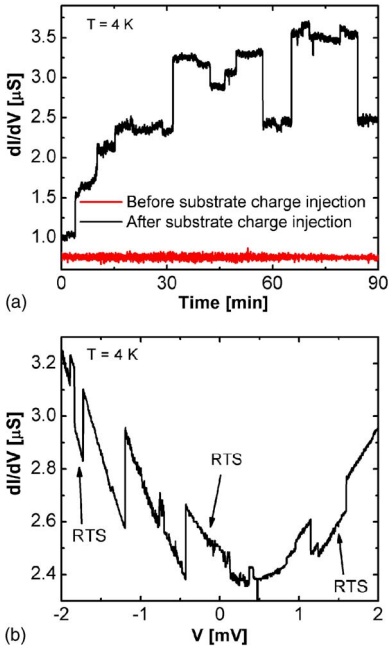

FIG. 5. (Color online) The tunnel junction as an active charge sensor. (a) The red (gray) line represents the zero-bias differential conductance of the tunnel gap which shows a stable differential conductance over the time scale of several hours. After deliberate charge injection, achieved by biasing the substrate beyond breakdown, random telegraph signals from local charge motion are observed (black trace). (b) The effect of deliberate charge injection on the differential device conductance as a function of source-drain bias.

compared to zero applied bias. Such behavior is expected since applying a positive (negative) bias effectively lowers (increases) the tunnel barrier. This demonstrates that bias cooling provides a means of adjusting the tunnel barrier at a given temperature and may be a regarded as a way to modulate the conductance in STM-patterned tunnel junctions.

We then test the possibility of STM-fabricated tunnel junctions to act as a local charge sensor by deliberately injecting charge from the conducting base of the chip package into the substrate. At 4 K, it was found that charge injection into the substrate occurs if the metal plane of the chip package under the silicon substrate is biased beyond a voltage range of −9 V to +5 V. The effect of this charge injection on the conductance of the tunnel junction is shown in Fig. 5. Figure 5(a) shows the zero-bias differential conductance before (red (gray) trace) and after (black trace) intentional substrate charge injection. In the absence of excess charge, the differential conductance is stable over (at least) a time scale of several hours. After substrate charge injection, we observe random telegraph signals which appear as characteristic jumps in the differential conductance due to charge motion. It is worth noting that thermal cycling to room temperature will eliminate these random telegraph signals and reconfigure the potential landscape. The influence of induced charge motion is further evidenced when considering the change in differential conductance with source-drain voltage after deliberate substrate breakdown as shown in Fig. 5(b). Here, random telegraph signals, previously absent in Fig. 2(b), are found to be superimposed on the parabolic shape. Both observations are a direct result of charge movement in the vicinity of the tunnel junction which locally changes the potential landscape, resulting in sharp jumps in the differential conductance. Random telegraph signals are most likely due to charging and discharging of a two-level system in the proximity of the tunnel gap. Such a two-level system could either be a defect-related charge trap or a P dopant from the background doping. Similar behavior due to charge traps has also been observed in narrow silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) by Ishikuro *et al.*[24]

In summary, we have electrically characterized highly planar tunnel junctions with atomically abrupt P dopant profiles in Si separated by 48 nm. At 4 K, we obtain reproducible, nonlinear *I-V* characteristics without the presence of any resonant structure. Temperature-dependent *I-V* measurements allow us to determine a thermally activated tunnel barrier of ~0.5 meV. We find significant tuning of the tunneling conductance when cooling the device with an applied bias. Finally, we demonstrate the ability of an STM-fabricated tunnel junction to act as local charge sensor.

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