Identifying single-electron charging islands in a two-dimensional network of nanocrystalline silicon grains using Coulomb oscillation fingerprints

M. A. H. Khalafalla,[1] H. Mizuta,[1] and Z. A. K. Durrani[2,*]

[1]*Quantum Nanoelectronics Research Center, Tokyo Institute of Technology, Ookayama, Meguro-ku, Tokyo 152-8552, Japan and SORST JST (Japan Science and Technology Corporation), 4-1-8, Honcho, Kawaguchi-shi, Saitama 332-0012, Japan*

[2]*Department of Engineering, University of Cambridge, Trumpington Street, Cambridge CB2 1PZ, United Kingdom and SORST JST (Japan Science and Technology Corporation), 4-1-8, Honcho, Kawaguchi-shi, Saitama 332-0012, Japan*

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We determine, at 4.2 K, the location of dominant single-electron charging islands in a multigrain system formed by a nanocrystalline silicon thin film. The film is 40 nm thick, with ~10–30 nm size silicon grains separated by ~1 nm thick grain boundaries. Cross-shaped, single-electron transistors are fabricated in the film, with four current terminals connected to a ~100 nm central region containing ~10 grains. Four side gates control the device current. We measure single electron oscillations in the current systematically through each of the four terminals, as a function of the gate voltages. Patterns in the Coulomb oscillations are used as "fingerprints" to identify the location of four major charging grains. In addition, electrostatic coupling effects can occur between the grains. Our results may suggest that six major bidirectional current paths form between the different terminals across the device.

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I. INTRODUCTION

Nanocrystalline silicon (nc-Si) materials, consisting of crystalline silicon grains ~10 nm in size separated by thin amorphous silicon or silicon oxide grain boundary (GB) tunnel barriers, are of great promise for the fabrication of quantum dots (QDs) and single-electron transistors (SETs) compatible with large-scale integration (LSI) processes.[1–3] The silicon grains "naturally" form large numbers of nanometer-scale QDs with high electron-confinement and single-electron charging energy,[4] raising the possibility of QDs and SETs operating at room temperature.[1,5] The high density of the QDs is also of great interest for LSI, and for silicon-based quantum information processing applications.[6–8]

Nanocrystalline Si thin films consists of a disordered network of grains and GBs of varying size and structure.[9] It has been proposed that the low temperature electronic conduction mechanism through these films consists of a combination of percolation transport and single-electron charging effects.[7,8,11] The percolation transport process is dominated by conduction along low resistance current pathways[10] and in a nc-Si film, a chain of grains with low GB tunnel barrier resistances can form these pathways. Single-electron charging effects in the grains may divert a current path by creating high resistance regions. If the single-electron charging energy $E_c = e^2/2C$ of a nc-Si grain of capacitance C is large compared to the thermal energy $k_B T$ at a measurement temperature T, Coulomb blockade of the electron transport at low bias leads to a high resistance path. In a macroscopic region of the film, it is possible for the current path to bypass this high resistance path. However, in transport across a nanoscale region with only a few grains, single electron effects can dominate, as the current path may not be able to avoid grains in a Coulomb blockade. Due to the random distribution of the grain size, the single-electron charging energy varies from grain to grain, modulating the resistance of the various possible current paths. The associated path resistance is high if the constituent grains are in Coulomb blockade and low otherwise.

Danilov *et al.*[12] have investigated theoretically the transport mechanism through multigrain single-electron transistors with strongly different tunneling resistances. They demonstrate that it is possible to deduce, from the characteristics of the differential conductance as a function of the bias voltage and the gate voltage, the topology of the multigrain system. However, this method may not apply to systems of grains linked with equivalent tunnel barriers (i.e., tunnel barriers with similar resistances and capacitances).

In this paper, we perform a series of current measurements at multiple biasing terminals to investigate the location of the dominant charging grains, and the major current paths, through a system of single-electron charging islands formed in a nc-Si thin film at 4.2 K. The nc-Si film is 40 nm thick, with crystalline silicon grains ~10–30 nm in size separated by ~1 nm thick amorphous silicon GBs. Cross-shaped, SETs are fabricated in the film. These devices consist of a ~100 nm × 100 nm center region connected to four terminals via ~30 nm wide "point contacts," with four side-gates to control the current. It is possible for the grains in our system to couple electrostatically to each other.[7,13] Our approach measures multiple current paths through the device, and in contrast to Danilov's method, the technique is independent of the symmetry of the tunnel barrier. Furthermore, the orthodox theory used by Danilov *et al.* may be modified and combined with our experimental method to deduce the topology of a carefully prepared sample, which is less disordered than the nc-Si sample used in our present work. Our approach may also be used to better understand the operation of scaled thin film transistors, and nc-Si single-electron devices such as memories,[11] where it is believed that charge is stored in grains randomly located near a percolation path. This approach may not determine the actual, complex, current percolation paths. Therefore the term "current path," used in the context of our data analysis, is simply defined as

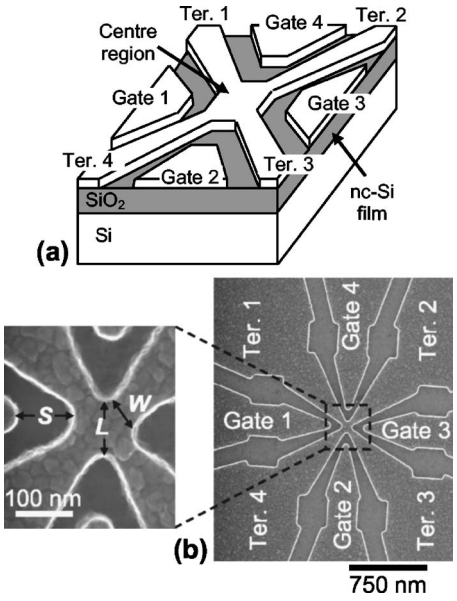

FIG. 1. (a) Schematic diagram of a nanocrystalline silicon cross SET (b) Scanning electron micrographs of a cross SET.

a simplified smooth line connecting any two terminals in our devices.

The paper is organized as follows. Section II describes the device fabrication process. Section III presents single-electron transport measurements at 4.2 K, used to determine the location of dominant grains located along major current paths through the device. Section IV analyzes these measurements and identifies the location of the dominant grains. Section V concludes the paper.

II. FABRICATION

Figure 1(a) shows a schematic of the cross nc-Si SET. The device consists of a 100 nm$\times$100 nm center region, with four constricted ($\sim$30 nm wide) point contacts at the edges. Each point contact leads into a wider terminal region. The four terminals form source and drain contacts to the device. Four side gates lay between the terminals, isolated from the center, point contact, and terminal regions. The gates can be used to control electrostatically conduction through the center region and the point contacts.

The cross SETs were fabricated in a $\sim$40 nm thick nc-Si film, deposited by low-pressure chemical vapor deposition (LPCVD) on a 150 nm SiO_2 layer grown thermally on a crystalline silicon substrate. The grain size varies from $\sim$10–30 nm, and the GBs are $\sim$1 nm thick amorphous Si tissues. The nc-Si films were doped n type with phosphorus, at a concentration of 1×10^{19} cm^{-3}. High-resolution electron beam lithography was used to define the transistor pattern in a polymethyl methacrylate (PMMA) resist, followed by reactive ion etching in CF_4 plasma to trench isolate the center region from the sidegates. The fabricated devices were then oxidized in dry O_2 gas at 750 °C for 30 min. This process converts the amorphous Si GBs into SiO_x, raising the associated tunnel barrier energy and improving electron confinement on the grains.[14]

Figure 1(b) shows a scanning electron micrograph of the device. The size of the center region L is $\sim$100 nm, the width of the point contacts W is $\sim$30 nm, and the gate-to-center region separation S is $\sim$100 nm. Approximately 10 grains are visible within the center region.

III. RESULTS

We carry out a series of electrical measurements at 4.2 K, to identify the number and location of grains with single-electron charging, using the following approach. The cross SET center region contains $\sim$10 nc-Si grains, with additional grains in the point contacts. Due to their random size distribution, not all of these grains may show single electron charging at 4.2 K. The cross SET can then be assumed to be a "black box" with an unknown number and location of charging grains. To locate these grains, we measure four sets of current vs gate voltage characteristics. Each set corresponds to one of the four terminals grounded, and the other three terminals biased at a small voltage. The four gates are connected in pairs to form two "doublegates." The current, measured as a function of either of the two double-gate voltages, shows Coulomb oscillations associated with tunnelling through the single-electron energy levels on the grains.[13] These oscillations shift diagonally across the plot as a function of both double-gate voltages as the energy of the single-electron energy levels changes electrostatically as a function of either gate voltage. The random distribution of the grains leads to a complex pattern of lines. By comparing features in the pattern formed by the oscillations, in conjunction with the various possible current paths between the biased and grounded terminals, in the 12 plots possible, the locations of the dominant charging grains can be identified. Here, the features act as "fingerprints" of a given grain, or stable combination of grains, and the slopes of the features help approximating the locations of these grains relative to the side gates. Our approach does not require a detailed analysis of the very complex oscillation patterns of each plot to determine the grain location.

Figure 2(a) shows the three-dimensional (3D) gray-scale electrical characteristics of a device similar to Fig. 1(b). The currents I_1, I_2, I_3, and I_4 are measured at terminals "1," "2," "3," and "4," respectively, as a function of the double-gate voltages $V_{g1,g2}$ [applied simultaneously to gates 1 and 2, Fig. 1(b)] and $V_{g3,g4}$ (applied simultaneously to gates 3 and 4). The dark regions have low current and the white regions have high current (max. current: 6 pA). We arrange these plots in 12 blocks in a matrix layout. The rows, 1g, 2g, 3g, and 4g [Fig. 2(a)] of this matrix contain, respectively, the characteristics corresponding to terminals 1, 2, 3, and 4 grounded. The columns correspond to the currents I_1, I_2, I_3, and I_4, measured at terminals 1, 2, 3, and 4, respectively. A bias of 3 mV is applied to the ungrounded terminals in each plot. In a set of three plots corresponding to the same ground terminal, e.g., row "1g" [Fig. 2(a)], each plot shows the current in an ungrounded terminal. For example, in row 1g [Fig. 2(a)], these are the currents I_2, I_3, and I_4. The diagonal blocks [hashed squares, Fig. 2(a)] are empty because no currents have been measured at a grounded terminal. We will refer to

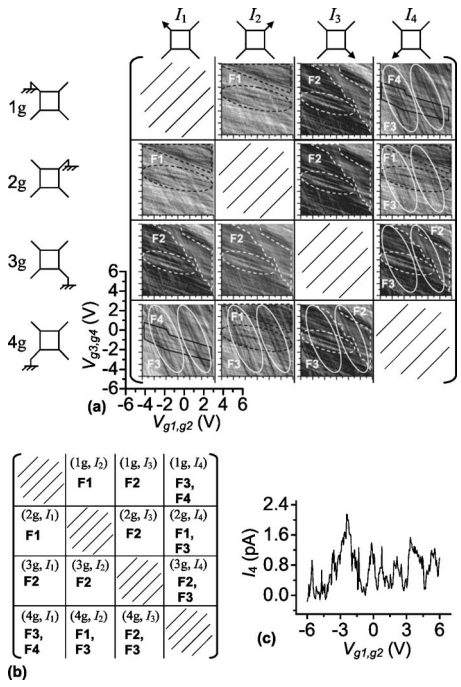

FIG. 2. (a) 3D gray scale characteristics at 4.2 K, of a cross transistor, of the currents I_1, I_2, I_3, and I_4 as a function of the gate voltages $V_{g1,g2}$ (applied simultaneously to gates 1 and 2) and $V_{g3,g4}$ (applied simultaneously to gates 1 and 2) where I_1, I_2, I_3, and I_4 are measured respectively at terminals 1, 2, 3, and 4 with a terminal bias of 3 mV. The dark regions have low current (Min: 0 A) and the white regions have high current (Max: 6 pA). F1 (dashed black lines), F2 (dashed white lines), F3 (solid white lines), and F4 (solid black lines) are Coulomb oscillation features used as fingerprint patterns to locate the dominant charging Si grains in the cross transistor. The characteristics are arranged in a matrix layout where the columns are represented by the currents. The rows, 1g, 2g, 3g, and 4g, correspond to terminals 1, 2, 3, and 4 grounded, respectively. (b) Schematic of the matrix in (a). Here the 3D plots are replaced by their matrix indices, (i_g,I_j), where $i \neq j$: 1, 2, 3, 4, and I_j is the current at terminal j while terminal i is grounded. (c) A single line plot of I_4 vs $V_{g2,g3}$ at $V_{g1,g2}=-0.775$ V across $(3g,I_4)$ characteristics.

each plot of the matrix using the row indices (1g, 2g, 3g, and 4g) and the columns indices (I_1, I_2, I_3, and I_4) as "(ig,Ij)" where $i \neq j$: 1, 2, 3, 4. For example the plot in the top-left corner of the matrix in Fig. 2(a) is referred to as $(1g,I_4)$. This plot is measured at terminal 4 while terminal 1 is grounded. Figure 2(b) shows a schematic of the matrix where, for clarification, we omitted the 3D plots and replaced them by their corresponding matrix indices.

Coulomb oscillations are observed in each plot [Fig. 2(a)], forming a complex set of lines as the single-electron levels in many grains vary with gate voltage. We identify various features in the patterns formed by the lines, e.g., "F1" (dashed black lines), "F2" (dashed white lines), "F3" (solid white lines), and "F4" (solid black lines). Figure 2(c) shows a single line plot of I_4 vs $V_{g1,g2}$ at $V_{g3,g4}=0.775$ V across (3g, I_4) characteristics. We note that some features are reproduced with high accuracy in the current measured in *different* terminals, e.g., feature F1 can be seen in Figs. 2(a) and 2(b) in

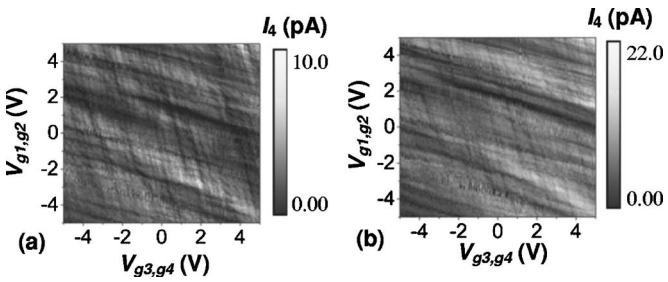

FIG. 3. (a) Measurement on a second cross transistor of the current I_4 at 4.2 K vs $V_{g1,g2}$ and $V_{g3,g4}$ [see Fig. 2(a) caption], with terminals 1, 3, and 4 biased at 3 mV and terminal 2 connected to ground (b) I_4 measured with only terminal 4 biased at 3 mV and terminals 1 and 3 floating.

$(1g,I_2)$, $(2g,I_1)$, $(4g,I_2)$, and $(2g,I_4)$. We also notice that the features above the diagonal of the matrix [hashed blocks, Figs. 2(a) and 2(b)] are mirror images of the features below the diagonal, forming a highly symmetrical arrangement about the diagonal. Similar measurements have been performed on a second cross SET, and qualitatively similar behavior is observed.

In the measurement in Fig. 2, a source voltage is applied to three terminals and one terminal is connected to ground. In Fig. 3, we investigate the effect of reducing the number of terminals with applied voltage, using the second cross SET. In this measurement, a voltage is applied to three terminals [Fig. 3(a)] and to only one terminal [Fig. 3(b)]. Figure 3(a) shows the current I_4 at 4.2 K as a function of the gate voltages $V_{g1,g2}$ and $V_{g3,g4}$, with terminals 1, 3, and 4 biased at 3 mV and terminal 2 connected to ground, i.e., our usual bias configuration. Figure 3(b) shows I_4 measured with only terminal 4 biased at 3 mV and terminals 1 and 3 floating. Comparison between these two measurements showed that the Coulomb oscillation patterns in both characteristics are similar and differ only in the average current level.

We also observe electrostatic coupling effects between grains along a given current path in another cross SET, in a manner similar to our previous work on point-contact SETs.[7,8] Figure 4 shows a gray-scale plot at 4.2 K of the current I_4 vs V_{g1} and V_{g2}, where V_{g1} and V_{g2} are the voltages on gates 1 and 2. Here, a voltage $V_4=5$ mV was applied to terminal 4 and terminal 2 was connected to ground. The other two terminals were not used and were left "floating." A constant voltage $V_{g3}=1$ V and $V_{g4}=0$ V was applied to gates 3 and 4, respectively. The single-electron pattern shows hexagonal regions, e.g., region "B," a signature of electrostatic coupling between two quantum dots.[13] The current varies from 28 pA (white region) to ~0 pA (dark region) and the average current decreases with more positive gate voltages.

IV. DISCUSSION

We will now determine the location of the dominant charging nc-Si grains in a cross device (Fig. 1), which lead to the features F1, F2, F3, and F4 in the characteristics of Fig. 2. To simplify the discussion we use the diagrams of Figs. 5(a)–5(d), which show schematically the current paths and

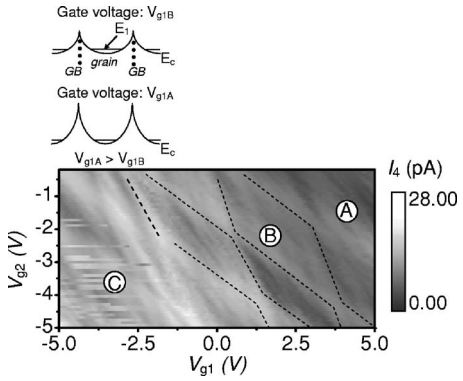

FIG. 4. Gray scale plot, at 4.2 K, of terminal 4 current, I_4, vs gate 1 and 2 voltages, V_{g1} and V_{g2}. Terminal 2 and gate 4 are grounded. Terminal 4 voltage V_4=5 mV and gate 3 voltage V_{g3} =1 V. Terminals 1 and 3 are floating. Top left inset: Schematics of the conduction band across a grain and two grain boundaries, at gate 1 voltage V_{g1A} and V_{g1B}, where $V_{g1A} > V_{g1B}$. E1 is the intergrain Fermi level.

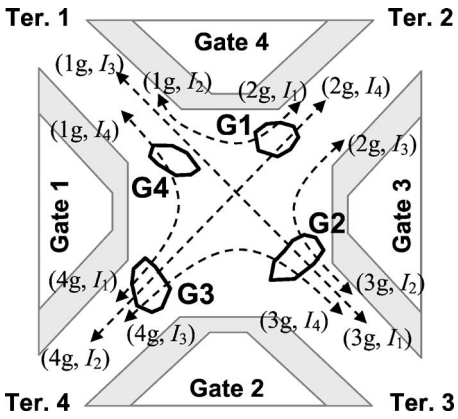

FIG. 6. (a) A schematic diagram showing the approximate locations of the dominant charging grains (G1, G2, G3, and G4) in a cross transistor. These locations were estimated using the patterns of the Coulomb oscillation features, F1, F2, F3, and F4 (Fig. 2), as fingerprints. The dashed arrows are the possible current paths through these grains.

terminals involved in the observation of the features of Fig. 2. While the actual shape of a current path, as current percolates through the grains, may be very complex, the point of origin and the end point are similar to the schematic paths of Fig. 5. We use each schematic path as a simplified means to represent and count an actual current path through the charging grains. Using this picture, as well as features F1–F4, enables us to investigate the locations of the charging grains associated with the features approximately.

We start with feature F1, which appears in the current paths shown in Fig. 5(a), i.e., between terminals 1 and 2, and between terminals 2 and 4. Here, the arrows indicate the bidirectionality of the current paths. This bidirectionality is associated with the symmetry of the matrix in Fig. 2 about the diagonal (hashed blocks, Fig. 2). The observation of F1

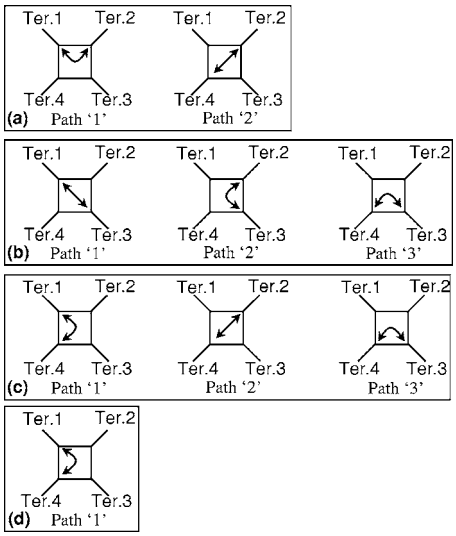

FIG. 5. Schematic diagrams of the possible current paths (double headed arrows) between the terminals (Ter. 1, Ter. 2, Ter. 3, and Ter. 4) of a cross transistor. These paths are associated with the observed Coulomb oscillation features in Fig. 2.

in (1g,I_2) and (2g,I_1) [Fig. 2(b)] results in the current path between terminal 1 and terminal 2 [Path "1," Fig. 5(a)]. Similarly, the observation of F1 in (2g,I_4), and (4g, I_2) results in the current path between terminal 2 and terminal 4 [Path "2," Fig. 5(a)]. These are the only plots in Fig. 2 where we can see F1. We also note that F1 occurs when terminal 2 is involved in a measurement with terminals 1 and 4, but not with terminal 3. We associate F1 with a charging grain, or a set of grains, "G1" near terminal 2. The slope of the lines in "F1" implies that G1 has stronger capacitive coupling to $V_{g3,g4}$ than to $V_{g1,g2}$. This suggests that G1 may be located closer to gates 3 and 4. The position of G1 is shown schematically in Fig. 6. The current path between terminal 2 and terminal 3 bypasses G1.

Secondly: Feature F2 is observed in the current paths shown in Fig. 5(b). Path 1 gives rise to the characteristics of (1g,I_3), and (3g,I_1) [Fig. 2(b)]. Paths 2 and 3 correspond to the characteristics of (2g,I_3) and (3g,I_2), and (3g,I_4) and (4g,I_3) [Fig. 2(b)], respectively. Since F2 occurs in the characteristics whenever terminal 3 is involved, we associate this feature with a charging grain, or grains, G2 near terminal 3 (Fig. 6). G2 intercepts all the current paths originating or terminating at terminal 3. The slope of the lines in F2 also suggests stronger coupling to $V_{g3,g4}$. We therefore locate G2 closer to gate 3 so that the capacitive coupling to $V_{g3,g4}$ is larger than that to $V_{g1,g2}$.

Thirdly: Feature "F3" is observed in the current paths shown in Fig. 5(c). Paths 1, 2, and 3 are associated with the characteristics of (1g,I_4) and (4g,I_1), (2g,I_4) and (4g,I_2), and (3g,I_4) and (4g,I_3) [Fig. 2(b)], respectively. F3 appears in the current path between terminal 4 and any other terminal. We associate F3 with a grain, or grains, "G3" near terminal 4 (Fig. 6). G3 intercepts all the current paths originating or terminating at terminal 4. Here the slope of the lines in F3 is consistent with the approximate location of G3 near gate 1 or gate 2.

Finally: Feature F4 is observed in the current paths shown in Fig. 5(d). F4 is only observed in the characteristics of

$(1g, I_4)$ and $(4g, I_1)$ [Fig. 2(b)], when conduction occurs between terminal 1 and terminal 4. Here, the corresponding grain, or grains, "G4" are bypassed by any current paths associated with terminal 2 and terminal 3. We locate G4 near the edge of the center region, between terminal 1 and terminal 4 (Fig. 6). Here G4 is close to both gate 1 and gate 4 while gate 2 and gate 3 are distant. The slope of the lines in F4 suggests that there is a stronger coupling of G4 to gate 4 rather than gate 1.

Figure 6 shows schematically the various current paths and grains (G1–G4) in the layout of the cross SET. There are six current paths between the terminals passing through the four grains. We represent the current paths in a simplified manner by dashed lines connecting the terminals. The lines connect the terminals involved in each current path. The current flow is bidirectional between any two terminals (shown by arrowheads on the dashed lines). The path index near the arrowhead refers to the corresponding characteristics in Fig. 2. When two charging grains are both located along a current path, their corresponding features coexist in the characteristics, e.g., features F1 and F3, associated with grains G1 and G3, respectively, coexist in $(2g, I_4)$ in Fig. 2. We observe that we do not see the distortion of a feature due to the simultaneous presence of the other, indicating that interactions between the corresponding grains are negligible in the device. This is likely if the grains are spatially far apart. This is discussed in more detail with reference to Fig. 7, later in this section.

The Coulomb oscillation pattern in the conduction between a ground terminal and a biased terminal is reproduced with high accuracy when the setup is reversed, i.e., when a previously biased terminal is changed to a ground terminal. This suggests that a unique current path forms between any two terminals. Some of these paths may contain parallel branches through grains electrostatically coupled in parallel, as we will see in the discussion concerning the characteristics of Fig. 4.

As commented on in Sec. III, we have observed qualitatively similar behavior in a second cross SET. A similar analysis to the above again allowed us to locate the single-electron charging grains in the device. We observe in both devices that the grains tend to occur at the edges of the center region, in particular at the point contact constrictions [i.e., the region with width "W" in Fig. 1(b)] between the terminals and the center region. In this region, the effect of the gate electric field on the charging grains is strongest, and least likely to be screened by charge trapped in other grains not along the current path. The point-contact grains are most likely to be controlled by the gate voltages and our plots therefore reflect single-electron charging of these grains. Similarly, grains near the edges of the center region are more likely to show up in the characteristics than those within the center of the device.

We now consider the effect of a change in the number of biased terminals (Fig. 3) measured on the second cross SET. A reduction in the number of biased terminals from three [Fig. 3(a)] to one [Fig. 3(b)] does not change the pattern of Coulomb oscillation. This suggests that there is a dominant, unique path for the current between the two terminals, independent of the bias and current of the other terminals.

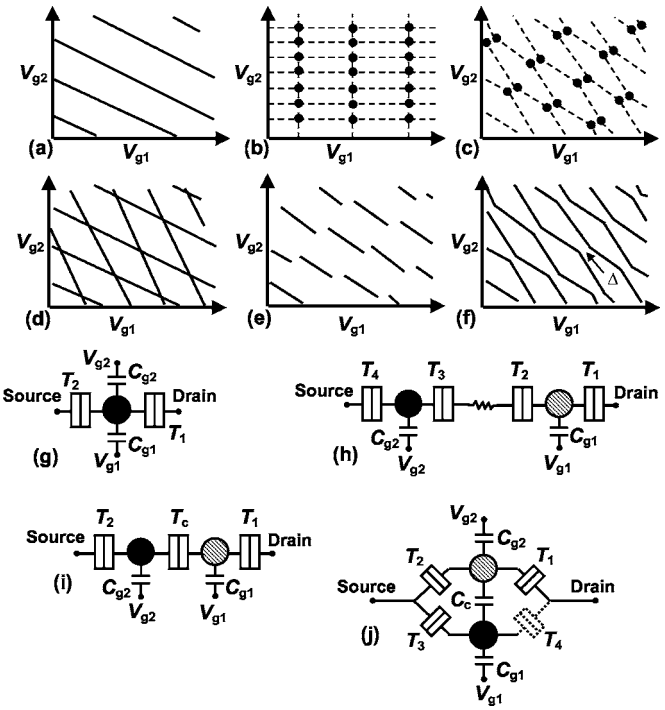

FIG. 7. (a) A plot of the position of the Coulomb oscillations (diagonal black lines) for a single charging grain in the configuration of (g), connected by tunnel junctions T_1 and T_2 to the source and drain, and coupled capacitively to two gate voltages V_{g1} and V_{g2}. (b) A plot of the Coulomb oscillation positions for the configuration in (h) of two grains along series current paths, without any capacitive interaction between the grains. The dashed lines form the boundaries of regions of stable charge on the grains. Conduction occurs at the black dots. (c) Charge stability diagram for two grains tunnel coupled in series, as shown in (i). Conduction occurs at the triple points (black dots). (d) A plot of the Coulomb oscillation positions for two grains along parallel current paths, without interaction between the grains. (e) The Coulomb oscillation position (solid lines) for the configuration of (j), excluding tunnel junction T_4. (f) The Coulomb oscillation lines for the configuration of (j), including the tunnel junction T_4.

In the above analysis, we have considered the Coulomb oscillation patterns simply as fingerprints of the single-electron charging grains, without attempting to analyze each complex pattern in detail. It is, however, possible to obtain further information about the configuration of the grains by analyzing a given pattern. Six possible grain configurations, and their corresponding "ideal" patterns, are shown in Fig. 7. Figure 7(a) shows a schematic of the oscillation pattern for a single charging grain in the configuration of Fig. 7(g), connected by tunnel junctions T_1 and T_2 to the source and drain, and coupled capacitively to two gate voltages V_{g1} and V_{g2}. The Coulomb oscillations then trace diagonal lines of the same slope in the plot [Fig. 7(a)]. Figure 7(b) shows the pattern of the configuration of Fig. 7(h) where two grains are connected in a series by a resistive path. The dashed lines are the boundaries for the regions of stable charge on the grains. Conduction can occur only at the crossing points between these boundaries (black dots), where both grains are not in a Coulomb blockade. If only a single gate couples to a grain,

then the dashed lines form a rectangular grid as shown. If both gates capacitively couple to each grain, then the dashed lines cross each other at an acute angle, forming diamond-shaped rather than rectangular regions. If these grains also couple to each other via a tunnel barrier T_c, Fig. 7(i), then the pattern of Fig. 7(c) is observed, where conduction is limited to the triple points[13] [black dots, Fig. 7(c)].

Figure 7(d) shows a plot of the Coulomb oscillation positions for a configuration of two grains along parallel current paths, without any interaction between the grains.[13] The Coulomb oscillations of each grain now trace out lines, but of a different slope due to different capacitive coupling to the gates. Figure 7(e) shows the Coulomb oscillation lines for the configuration shown in Fig. 7(j) by the solid lines, i.e., with "grain 1" and "grain 2" coupled by the capacitor C_C and without the tunnel junction T_4. Here, the Coulomb oscillations of grain 1 form lines, which switch in position each time an electron charges grain 2 (Ref. 7). Finally, Fig. 7(f) shows the Coulomb oscillation lines for the full configuration of Fig. 7(j), i.e., two capacitively coupled grains in parallel.[15] The pattern forms hexagonal regions of a constant charge number on the two grains, where the line splitting "Δ" is a measure of the electrostatic coupling between the grains.

In Fig. 2(a), different features coexist in a given plot, e.g., F1 and F3 coexist in plot (4g,I_2). Here, the low current (dark) lines from F3 cross similar lines from F1, e.g., within the oval dashed region of F1, without changes in the pattern of either F1 or F3. This suggests that the grains G1 and G3 associated with these features are far from each other along the current path. This may be similar to Fig. 7(h), or to Fig. 7(i) without the coupling capacitor C_c. The diamond-shape of the patterns formed by the intersecting lines suggests coupling of both gates to each grain. However, unlike the ideal pattern in Figs. 7(b) or 7(d), the characteristics of Fig. 2(a), (2g,I_4), show narrow low current (dark) regions and broadened Coulomb oscillation (white region) peaks. This suggests a large thermally activated current in the device. It is difficult to determine parallel or series coupling between grains associated with these features, due to the thermal broadening of the peaks. In this regime, the stability diagrams of series or parallel-coupled grains are almost equivalent and it can be difficult to distinguish between them.

The dark lines of F3 also break and switch in position. This may be attributed to an adjacent electrostatically coupled grain, with the switch corresponding to a change in the electron number of this grain.[7] G3 is then a grain combination, consisting of more than one electrostatically coupled grain.

The Coulomb oscillation patterns in Fig. 7 can be used to analyze in detail individual plots of the Coulomb oscillation lines in a cross SET, vs two gate voltages. Figure 4 shows the characteristics of the current I_4 between terminal 4 and terminal 2 as a function of the two nearby gates, V_{g1} and V_{g2}. These characteristics can be divided into regions "A," "B," and "C," reflecting different electrostatic coupling regimes between the nc-Si grains. The variation in coupling at different gate voltages can be attributed to an increase in the width of the GB tunnel barriers with gate voltage (inset, Fig. 4). The coupling is weak in region A (wide tunnel barriers) where the current is pinched off, and becomes strong in region C (narrow tunnel barriers). In between these two regimes (region B) intermediate coupling occurs between the grains. Here, some of the Coulomb oscillation peaks appear to define hexagonal electron stability regions (along black dashed lines, Fig. 4) similar to the schematic of Fig. 7(f), corresponding to two electrostatically coupled grains in parallel.[15] These grains can be placed on parallel branches along the current path between terminal 4 and 2. Additional, fine lines with a small oscillation period, which do not appear to interact with the hexagonal region lines, can be associated with a further grain that does not couple to the parallel-coupled grains.

We have also investigated (data not shown) the effect of the third gate, V_{g3}, on the characteristics of Fig. 2. We found that V_{g3} modulates the characteristics in a manner consistent with the effect of V_{g1} and V_{g2}, i.e., the coupling and the average current increases for more negative gate voltages. This behavior is opposite to the current enhancement expected in an *n*-type device at positive gate voltage. However, in our nc-Si SET, the effect of the GB tunnel barrier must be considered. The barriers are Schottky-like, becoming wider at lower energies relative to the top of the barrier.[16] With Fermi level pinning at the GB defect states, a more positive gate voltage lowers the electron levels in the nc-Si grain and electrons tunnel across a wider, higher resistance section of the barrier (Fig. 4, top left inset). This leads to a lower average current for more positive gate voltage.

We do not observe a clear gap Δ [Fig. 7(f)] between the triple points in region B in the characteristics of Fig. 4 due to the thermal broadening of the current peaks. Electron wave function delocalization may also occur between the coupled grains, across the thin grain boundary tunnel barriers, further contributing to the current between the triple points.[8] The small peak-to-valley ratio and the difficulty in observing a clear gap or splitting in the vicinity of the quasitriple points in region B (Fig. 4) also suggests a different interpretation of the data, e.g., two conducting grains in parallel without coupling, in analogy to Fig. 7(d).

V. CONCLUSION

This paper has investigated, at 4.2 K, the formation of current paths through a system of single-electron charging islands formed by the grains of a nc-Si thin film. Cross-shaped, single-electron transistors are fabricated in the film, with four current terminals connected to a ~100 nm central region containing ~10 grains. Four sidegates control the device current. We measure single electron oscillations in the current systematically through each of the four terminals, as a function of the gate voltages. Features in the Coulomb oscillations are used as fingerprints to identify the location of four major charging grains. By comparing similar features in different current paths, we determine the number and location of the charging grains, and the various current paths possible through these grains. Unique current paths can exist between any two terminals of the device. It is also possible to observe electrostatic coupling effects between grains along parallel branches.

Our work investigates the electron transport mechanism through a small number of grains in nanocrystalline silicon, and contributes to an understanding of the transition in electron transport in thin films from the local to the macroscopic scale. In addition, the cross SET forms a multiple QD system with a larger number of QDs than has been investigated previously. Our electrical results illustrate the rapid increase in the complexity of systems with multiple QD, compared to single or double QD systems. Our measurements also contribute to a better understanding of the electrical behavior of scaled thin film transistors. The results may also be used, along with numerical simulations, to further understand electron transport mechanisms in nanoscale, disordered, systems. The formation of stable, bidirectional, current paths in the device suggests the potential of nanocrystalline thin films for the fabrication of future QD based circuits.

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*Electronic address: zakd100@cam.ac.uk

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