Hybrid polymers as tunable and directly-patternable gate dielectrics in organic thin-film transistors

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The long-term target of producing all-organic devices requires custom-designed dielectric materials able to be applied and patterned with a wide range of new and fast deposition and patterning methods. Inorganic-organic hybrid polymers such as organic modified ceramics (ORMOCERs) have recently gained considerable attention in polymer electronics. Consisting of organically functionalized inorganic-oxidic units, their material properties can be tuned over a wide range and, in addition, their processing is very flexible providing good compatibility to many materials and substrates and allowing for direct patterning. A study on the application of different ORMOCER systems as gate dielectric layers in organic thin-film transistors (OTFTs) with pentacene as the organic semiconductor and directly structured contact holes is presented. Depending on the chemistry of the underlying ORMOCER system, different morphologies of the thermally evaporated pentacene were observed and correlated to the electrical characteristics of the transistor devices. In some cases, OTFTs with excellent electrical performance were achieved, showing intrinsic field-effect mobility values up to 1 $cm^2/V\,s$. Based on the high charge-carrier mobility of the pentacene-ORMOCER interface and the good dielectric, passivating, and patterning properties of the ORMOCER materials, these devices lay the foundation for a new generation of high-quality, fast, processable low-cost organic electronics.

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Many novel electronic applications, such as, for example, electronic wallpaper, wearable smart cards and sensors, or flexible rf ID tags, push for the market, involving new requests for the underlying electronic devices. Large-area coverage, structural flexibility, direct integration on plastic substrates, and ultralow-cost fabrication techniques are requirements that may be satisfied by organic electronics. Naturally, for a successful introduction of organic electronics into the market, an increase in the performance of the key elements of logic circuitry, the organic thin-film transistors (OTFTs), is essential. In recent years much effort has been spent to optimize and describe the chemistry and processing of the active organic semiconductor,[1–7] and the engineering of the contacts;[8–12] however, the performance of OTFTs is also essentially determined by the gate dielectric and the quality of its interface with the semiconductor.

Thin films of inorganic dielectrics, such as SiO_2,[13,14] Al_2O_3,[15] or Ta_2O_5,[16] have been fabricated in very reproducible quality, showing well-characterized dielectric properties and low leakage currents. However, as for SiO_2, the process temperatures are usually well above 200 °C and, especially for ceramic high-**k** materials, the specific mechanical properties intrinsically yield high brittleness. Thus, the demand for flexible plastic substrates and low-cost fabrication cannot be easily met with ceramic dielectrics.[17]

In contrast, organic dielectrics have many advantages. Their elasticity values are well adapted to flexible polymer substrates and foils. Furthermore, they are suited to level the underlying rough substrate surfaces[18] and form a "high-mobility" interface to the organic semiconductor.[19–21] Most importantly, they can be applied by fast low-cost processes such as printing technologies.[22] Very recently, a sufficiently thin and dense organic gate dielectric has been demonstrated on a SiO_2 substrate;[23] however, due to the extraordinarily high cross-linking temperatures of the benzocyclobutene, this material is not compatible with flexible polymer substrates.

In search of gate dielectric materials that satisfy the main requirements such as tuning of the dielectric properties (thickness, dielectric constant), low-temperature processing as a prerequisite for the compatibility with flexible substrates, and low-cost processing, which includes direct patternability, hybrid dielectrics are an interesting alternative.[17] Hybrid gate dielectrics with organic functional groups are well represented by solution-processed inorganic-organic hybrid polymers such as ORMOCERs.

ORMOCER systems of various compositions were synthesized by sol-gel processing, resulting in uv-patternable, storage-stable resins. Upon synthesis using commercially available alkoxysilanes, organically functionalized inorganic-organic units are established. For further processing, the organic moieties such as methacryl and/or epoxy groups have to be cross linked photochemically and/or thermally. The physical and chemical properties of ORMOCERs can be tuned over a wide range including the variation of the dielectric permittivity; they can be thermally treated at sufficiently low temperatures (<150 °C), thus allowing the use of thermally sensitive substrates such as polyethylenetherephtalate. In addition to the chemical stability against short dry etching processes and other common solvents, they can be patterned directly by uv lithography[24,25] and are passivation materials against humidity.[25]

In the scope of this work, it will be demonstrated that certain ORMOCER systems satisfy all requirements that are

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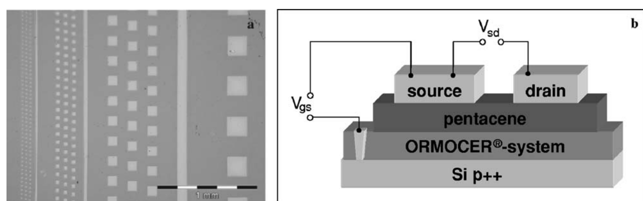

FIG. 1. (a) Micrograph of contact holes in ORMOCER VI directly patterned by uv lithography. (b) Layer sequence of an OTFT in top-contact geometry with an ORMOCER system as gate dielectric.

essential for their application as active gate dielectrics in OTFTs. This covers a low layer thickness (<500 nm), a low leakage current (10^{-10} A/cm^2), a sufficiently high dielectric strength (up to 300 V/μm), and the ability to be directly patterned. It is shown that the functional combination of an organic-inorganic dielectric hybrid polymer with an organic semiconductor is an excellent basis for a high-quality thin-film transistor. For pentacene thin-film transistors (TFTs), charge-carrier mobility values around $\mu = 1$ cm^2/V s were achieved, which are among the highest ever reported for organic dielectrics. The ORMOCER layer has been patterned prior to the application of the organic semiconductor by means of uv lithography. The device functionality strongly depends on the morphology of the semiconducting layer which, in a top contact configuration, is mainly triggered by the surface properties of the underlying ORMOCER. Two different ORMOCER systems were investigated and compared as active gate dielectrics. Both systems have in common that their organic moieties are epoxy and methacrylic groups. As network former either zirconium *n*-propoxide, 3-methacryloxypropyltrimethoxysilane, 3-glycidyloxypropyltrimethoxysilane, or epoxycyclohexylethyltrimethoxysilane was used. In order to achieve less brittle materials, diphenysilanediol and dimethyldimethoxysilane were used as network modifiers. The two systems are referred to as ORMOCER III (aryl-alkyl system) and ORMOCER VI (aryl-based system with zirconium), respectively.

The liquid ORMOCERs are spin coated on a highly doped or metallized silicon wafer serving as the gate contact. After a prebake step the gate dielectric layer was directly patterned by mask-assisted uv lithography in atmosphere or under inert gas conditions in order to form contact holes [Fig. 1(a)]. In the course of the processing the organic cross linking was performed via radical initiation. This only cross-links the methacryl groups, while the epoxy groups are not affected. The patterned ORMOCER layers are developed using standard developer solutions such as ketones. After final thermal curing, the organic semiconductor pentacene is directly deposited on the ORMOCER layers. The pentacene powder used for the deposition of polycrystalline thin films is acquired from commercial sources (Asahi Kasei) and preliminarily purified by a multistep sublimation-condensation process. The purified powder is then thermally evaporated from an effusion cell under high-vacuum conditions (10^{-6} mbar) with a deposition rate of 0.2 nm/min for the first 5 nm, and subsequently increased to 0.4 nm/min for thicker layers. The substrate temperature was set at 65 °C. The pentacene thin film is further characterized by using tapping-mode atomic force microscopy (AFM) for investigating the morphology and x-ray diffraction (XRD) for the determination of the structure and the volume distribution of the different crystallographic pentacene phases.

As is typical for OTFTs in top-contact configuration [see Fig. 1(b)], the source and drain electrodes are deposited onto the sensitive semiconductor via shadow-mask *e*-beam evaporation of 80 nm Au. The source-drain configuration consists of parallel structures with channel lengths between 20 and 200 μm; the channel width is 3 mm. For the electrical measurements, contact pads with an area of 250 μm^2 were used. For the ORMOCER VI system the resulting layer thickness was about 450 nm and the dielectric permittivity, as determined by impedance spectroscopy, was about 4.75. AFM measurements revealed rms roughness values of the dielectric surface around 6.8 Å.

In Fig. 2, AFM measurements illustrate the typical height [Fig. 2(a)] and phase [Fig. 2(b)] variations of the morphology of a pentacene layer evaporated on ORMOCER VI, showing highly correlated crystalline grain growth. The pentacene film consists of large, ramified islands of 2–4 μm in diameter, built up by individual terraces. The terraces are pronounced in the boundary-sensitive phase signal. The step height of the terraces corresponds exactly to the *c*-axis length of the elementary cell of single-crystalline pentacene (not shown in Fig. 2). Therefore, each grain forms a single-crystalline three-dimensional island with a preferred growth direction perpendicular to the ORMOCER substrate surface. From the difference in the direction of the terrace facets, it can be derived that the in-plane orientation of the crystallites is rotated with respect to each other. This is discussed as being the source of transport influencing barriers at the grain boundaries in the literature.[2,3,26,27] As the local distribution of the charge-carrier density in the accumulation layer is characterized by the Debye length which (depending on the vertical electric field) is in the range of one or two monolayers, practically the total charge is concentrated within the first layer in the accumulation regime.[28] Therefore, the morphology of the first pentacene monolayer (ML) has to be considered to be crucial for the charge-carrier transport in the channel region. In Figs. 2(e) and 2(f), the growth of pentacene islands on ORMOCER VI in the first monolayer is shown. For 0.2 ML coverage, well-separated single-crystalline grains with random in-plane orientation of the crystallographic *a*-*b* axis nucleate homogeneously distributed over the ORMOCER VI surface [Fig. 2(e)]. It has been shown that the nucleation density is strictly correlated to the deposition rate and the substrate temperature.[7,29] With increasing coverage, the clusters grow independently; at about 0.8 ML coverage they start to coalesce [Fig. 2(f)]. Depending on the mobility of adsorbed pentacene grains on the surface, which mainly is parametrized by the substrate temperature, some crystalline grains might rotate now and find a low-energy configuration characterized by an almost parallel crystalline orientation of neighboring islands. However, it is the number of actual grain boundaries that mainly influences the effective charge-carrier field-effect mobility. The potential barrier between individual grains at the grain boundary has been

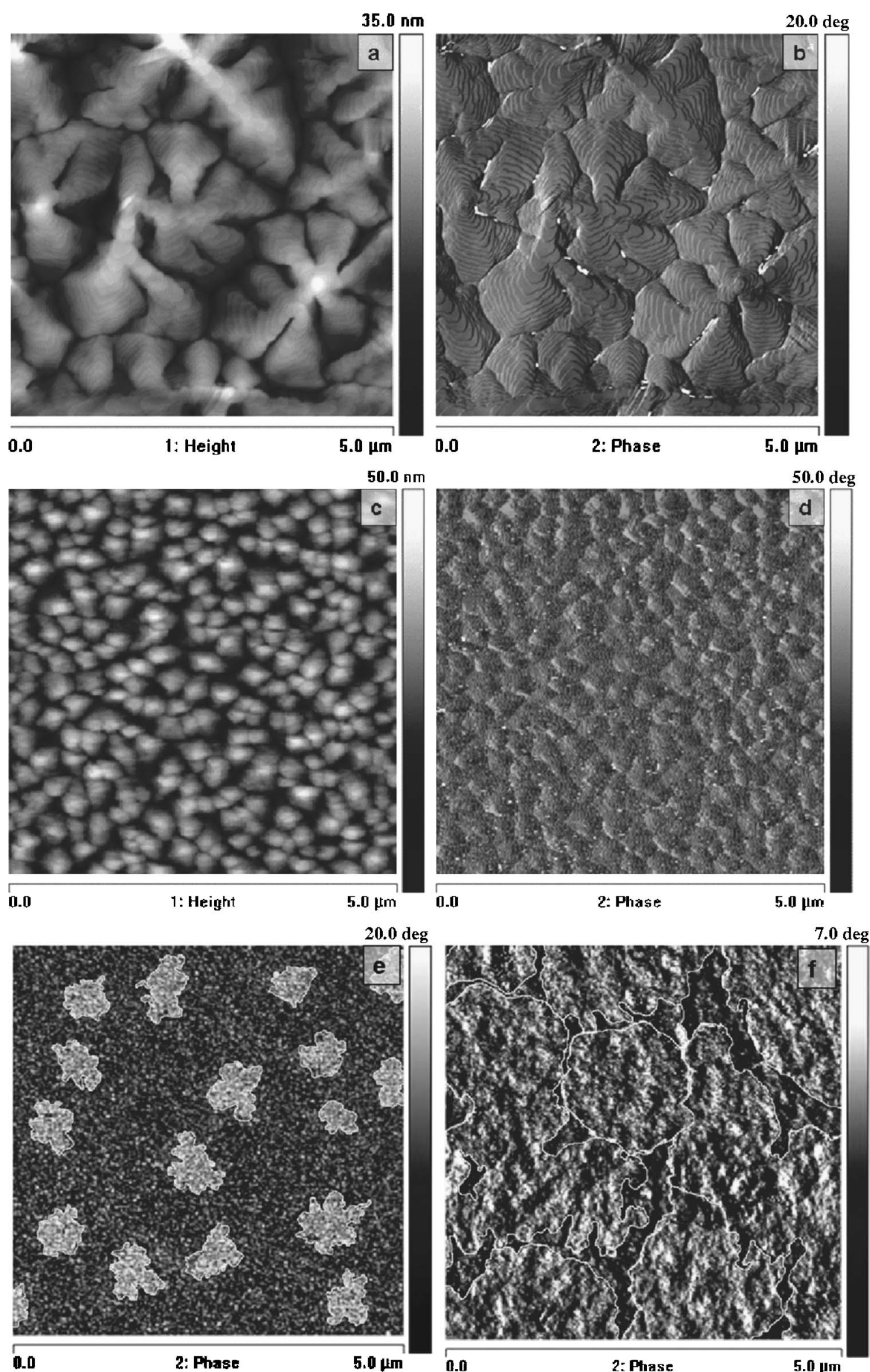

FIG. 2. AFM topography (left) and phase (right) images of a 50 nm pentacene layer on (a), (b) ORMOCER VI, and (c), (d) ORMOCER III. In the third row, AFM phase signals of (e) 0.2 and (f) 0.8 ML coverage of pentacene on ORMOCER VI are plotted. The grain boundaries are highlighted.

shown to be responsible for the mobility degradation observed in OTFTs with small semiconductor grain sizes.[3]

Information about the structure and the crystallinity of the films was obtained by XRD measurements. Pentacene polymorphs with different tilt angles of the parallel-arranged molecules with respect to the surface normal can be identified through the different locations of the (001) peaks, which are correlated to different *c*-axis lengths of the pentacene elementary cell. The XRD measurement of the pentacene grown on ORMOCER VI (Fig. 3, black curve) mainly shows the thin-film phase with its characteristic peak at $2\theta = 5.7°$. (001) reflexes up to the fourth order can be clearly observed. Due to the fact that the main maxima are sharp and intense a high ordering can be assumed. In the first and second orders, a low fraction of the bulk phase ($2\theta = 6.1°$ and 12.2°, respectively) is observed.

For comparison, substrates of the hybrid polymer ORMOCER III were also investigated and used as gate di-

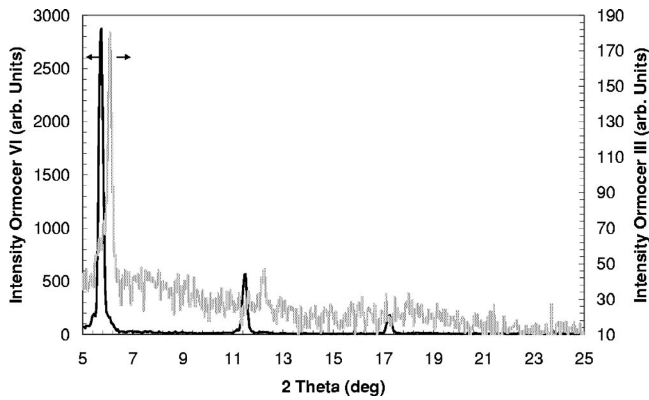

FIG. 3. XRD spectrum of a 50-nm-thick pentacene layer on ORMOCER VI (black curve) and on ORMOCER III (gray curve).

electrics in OTFTs. The processing of the ORMOCER III resin is analogous to that of ORMOCER VI, again resulting in a layer thickness of about 450 nm. The intrinsic rms roughness of ORMOCER III is about 6.2 Å, and therefore comparable to that of ORMOCER VI. Indeed, the pentacene film grown on ORMOCER III reveals a very large nucleation density and consists of tiny, cornered grains [Fig. 2(c)], although it has been applied using the same growth conditions (growth rate, substrate temperature, layer thickness) as for the ORMOCER VI substrate. Since there is no significant difference in the surface roughness between the two systems, it must be the specific surface chemistry and the surface structure of the ORMOCER VI network that are crucial for the formation of large-grained films. The XRD measurement for the pentacene/ORMOCER III system (Fig. 3, gray curve) reveals a dominant fraction of the bulk phase ($2\Theta=6.1°$). Due to the poorer ordering of the crystallites, only the (001) and, to some extent, the (002) reflex of this phase are detected; their full width at half maximum is increased according to the decreased size of the crystallites. For the bulk phase, the overlap of the π-electron system is lower than for the thin-film phase according to the larger tilt angle of the molecular axis with respect to the surface normal. This might have a detrimental effect on the charge-carrier transport.

In Fig. 4(a), the output characteristics of a top-contact transistor with ORMOCER VI as gate dielectric and a channel length of 55 μm reveal a good control of the drain current with the gate voltage and nearly perfect saturation. The gate leakage is negligible as well as the hysteresis between forward and reverse drain voltage sweeps.

In Fig. 4(b) the subthreshold characteristics in the linear regime (at $V_{DS}=-1$ V) of pentacene TFTs with ORMOCER VI and ORMOCER III as gate dielectrics and $L=200$ μm are compared. For both devices hysteresis in the drain current between forward and reverse gate voltage sweeps is smaller than the voltage sweep steps of 1 V. The pentacene TFT with ORMOCER III as gate dielectric has an on-current level I_{on} that is two orders of magnitude smaller than that of the ORMOCER VI device. Consequently the ORMOCER III device has an on-off ratio that is more than two orders of magnitude smaller than that of the ORMOCER VI device, which is $I_{on\text{-}off}=5\times10^5$. The subthreshold swing S of the OTFT with ORMOCER VI is about $S=1$ V/decade, compared to $S=6$ V/decade for the other dielectric material, indicating a very slow turn-on behavior for the latter. As the subthreshold swing is directly correlated with the number of interface traps, its strong increase in the ORMOCER III device is a direct indication that the increased number of grain boundaries, directly reflected by the larger nucleation density of pentacene grown on the ORMOCER III interface, can be associated with an increased number of interface traps.

From the subthreshold curve it is also possible to extract the turn-on voltage V_{on}, which is defined as the gate voltage to achieve a drain current level of ten times the lowest I_{off}. For the ORMOCER VI device we find $V_{on}=15$ V corresponding to a normally on device, whereas $V_{on}=6$ V for the ORMOCER III TFT. This clearly demonstrates that for the latter device a substantially higher gate voltage is needed to form an accumulation channel at the interface than for the ORMOCER VI device.

The threshold voltage was determined from the transfer characteristics in saturation by extrapolating the linear slope of the square root of the drain current to zero. For the ORMOCER VI TFT we found $V_T=15.5$ V which is very close to the V_{on} value that was determined from the linear regime, thus indicating that the turn-on behavior is independent of the lateral electric field. In addition to the signifi-

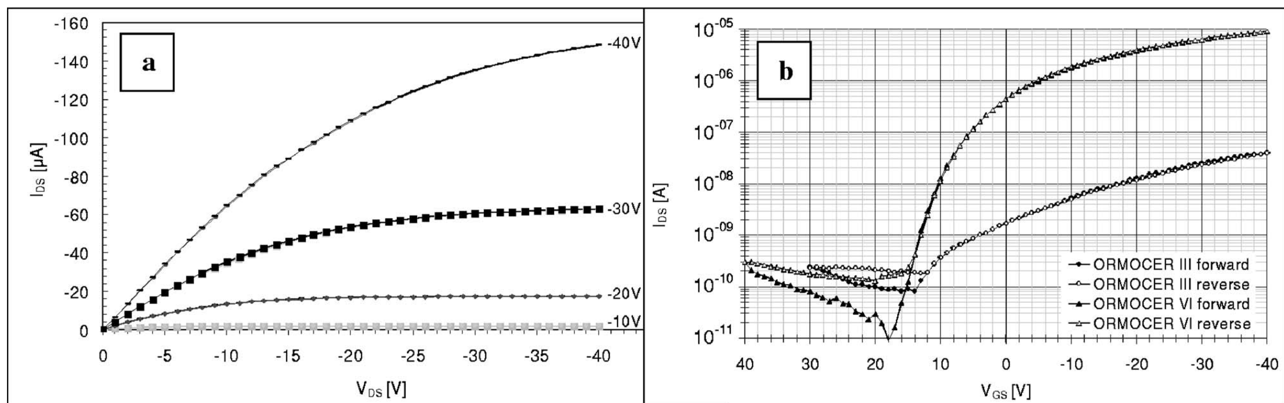

FIG. 4. (a) Output characteristics of an OTFT based on ORMOCER VI as gate dielectric. In (b) the subthreshold characteristics of an ORMOCER VI device at $V_{DS}=-1$ V is compared to the corresponding one of an ORMOCER III device. The onset voltage is determined as the gate voltage needed to achieve a drain current level that is one order of magnitude higher than the lowest off current.

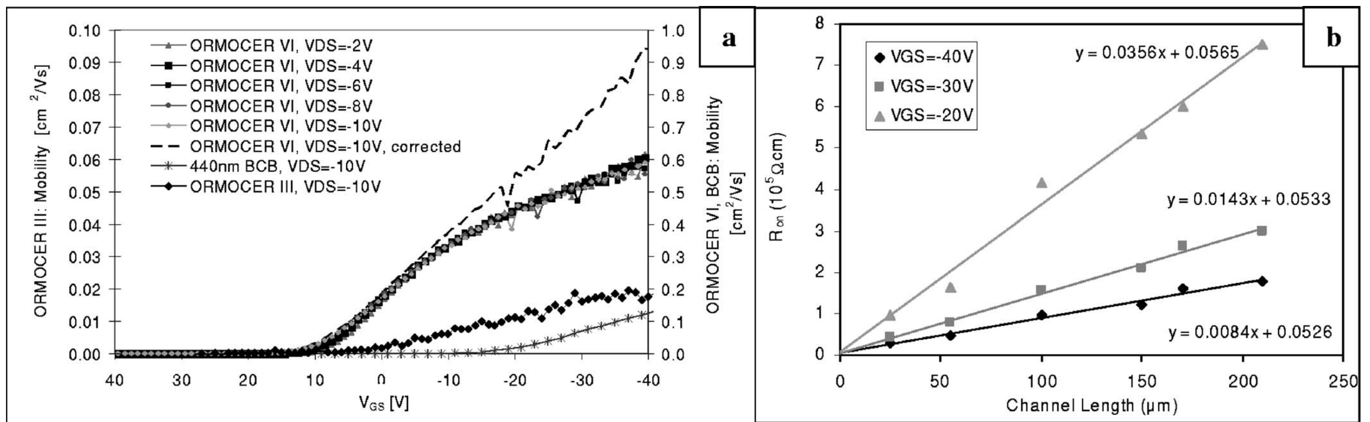

FIG. 5. (a) Gate voltage variation of the effective charge-carrier mobility $\mu_{\text{eff}}(V_{\text{GS}})$ for the OTFT based on ORMOCER VI as gate dielectric compared to that of the OTFT with ORMOCER III and of an OTFT with benzocyclobutene as gate dielectric. Also depicted is the gate voltage variation of the intrinsic mobility at $V_{\text{DS}}=-10$ V (dashed line). (b) Overall resistance as a function of the channel length. The total contact resistance is determined by extrapolating the linear fit to $L=0$.

cantly reduced drain currents, the threshold voltage is shifted to more negative values for the ORMOCER III device to about $V_T=6.5$ V as compared to the ORMOCER VI TFT. It is important to mention that all quoted device parameters for the ORMOCER VI system are typical values as has been figured out by characterizing a large body of transistors (see below).

In Fig. 5(a), the gate voltage variation of the charge-carrier mobility μ that can be deduced from the transconductance is illustrated. For the ORMOCER VI device, μ first increases with the gate voltage and then starts to saturate at $V_{\text{GS}}>-10$ V, which is attributed to the drain current limitation by the contacts. The maximum effective mobility is $\mu_{\text{eff}}=0.6\ \text{cm}^2/\text{V s}$. This value is a typical value that is quite near the mean value of effective mobiliy data $\mu_{\text{eff}}^{\text{stat}}$ that we extracted from 37 TFTs out of three different batches of ORMOCER VI devices to be $\mu_{\text{eff}}^{\text{stat}}=0.52\pm0.18\ \text{cm}^2/\text{V s}$. It is important to emphasize that a significant number of devices show μ_{eff} in the region $0.8\leqslant\mu_{\text{eff}}\leqslant1\ \text{cm}^2/\text{V s}$.

It is well known that for a gate-bias-dependent mobility, as is observed in this study, the saturation of the mobility at high gate voltages is due to a current reduction by the source and drain contact resistance.[28] According to Eq. (1),

$$\mu_i = \frac{\mu_{\text{eff}}}{\left(1-\mu_{\text{eff}}\dfrac{C'}{L}(V_{\text{GS}}-V_T)R_C\right)} \qquad (1)$$

with C' being the area-related capacitance of the hybrid dielectric and L the channel length, the correction for the experimentally determined series contact resistance $2R_C=54\ \text{k}\Omega$ mm yields a linearly increasing intrinsic carrier mobility μ_i with $\mu_i=0.95\ \text{cm}^2/\text{V s}$ at $V_{\text{GS}}=-40$ V [see the dashed line in Fig. 5(a)]. The contact resistance was determined with a standard method based on the transmission line model (see, for example, Ref. 12). According to this, the linear channel length dependence of the overall device resistance that was extracted from the linear part of the output characteristics was extrapolated to $L=0$ and the intercept taken as the total parasitic resistance $2R_C$ [see Fig. 5(b)]. For the ORMOCER VI TFTs the total contact resistance typically varies in the range $10<2R_C<100\ \text{k}\Omega$ mm and is only slightly gate voltage dependent for the range investigated.

A linear gate voltage dependence of μ_i is typical for the interface of organic semiconductors with organic dielectrics.[28] Some people argue that the charge-carrier mobility itself is gate voltage dependent due to a dependence on the induced carrier density which, in the linear regime, increases linearly with increasing gate voltage.[30] In this case for high-**k** dielectrics and constant film thickness (meaning constant electric field) an increased mobility is expected due to the fact that the induced charge-carrier density depends on the dielectric permittivity as well as on the film thickness. For polycrystalline semiconductors, the gate voltage dependence of μ_i is mainly attributed to the morphology of the active layers.[3,7,28,30] The linear gate voltage dependence of the mobility is more pronounced for organic dielectrics; here, gate-voltage-dependent mobility values can be observed for high-[30] and even for low-**k** materials.[7]

In contrast to the vertical electric field, the mobility is independent of the lateral electric field apart from a small influence of the series resistance which decreases with increasing V_{DS}. In Fig. 5, the dependence of the effective mobility on the gate voltage is also shown for the ORMOCER III OTFT. Again, the typical rise of the mobility and the contact-resistance-induced limitation at $V_{\text{GS}}>-20$ V are observed. But the maximum effective mobility is more than one order of magnitude ($\mu_{\text{eff}}=0.02\ \text{cm}^2/\text{V s}$) smaller than for the OTFT produced with ORMOCER VI as gate dielectric. The reduction in mobility is reflected directly in a corresponding reduction of the drain current level and a negative shift of V_T.

As can be concluded from the comparison of the electrical performances of the OTFTs based on gate dielectrics from the two different organosilane systems, there is a direct correlation between grain size, polycrystalline ordering, and charge-carrier mobility. The higher the ordering of the pentacene and the larger the crystallites, the higher is the intrinsic mobility. In ORMOCER III–based transistors, the increased fraction of the bulk phase that is believed to have a

reduced intrinsic mobility might also contribute to the mobility decrease.

This microstructure-property relationship is further supported by comparing the gate voltage variation of the mobility for ORMOCER devices with the one obtained for an equally constructed OTFT with a similarly thick ($d = 440$ nm) gate dielectric layer of benzocyclobutene (BCB). This material is also directly patternable and yields sufficiently dense dielectric layers; the overall mobility values, however, are smaller than those found for the ORMOCER VI devices, but larger than those of the other, the ORMOCER III system [Fig. 5(a)]. This is mainly due to the fact that the average pentacene grain size on the BCB layer is approximately 1.2 μm, compared to 3.8 μm on the ORMOCER VI and 0.4 μm on the ORMOCER III, thus suggesting that the order of magnitude of the charge-carrier mobility directly correlates with the average grain size of the polycrystalline semiconductor.

We produced and characterized high-quality organic field-effect transistors based on hybrid organic-inorganic ORMOCER dielectric materials and the organic semiconductor pentacene, demonstrating the use of low-temperature hybrid polymers as active directly patterned gate dielectrics in OTFTs. A comparison between two ORMOCER systems showed that the tuning of the chemical composition for the gate dielectric strongly affects the pentacene growth and therefore the whole functionality and performance of the polymer electronic device. With ORMOCER VI, intrinsic field-effect mobility values up to 1 $cm^2/V\,s$ and transistor characteristics showing high on-off ratios, good saturation, and nearly no hysteresis effects were achieved. OTFT devices based on the ORMOCER III system have poorer electric performance due to an increased density of trap states at the interface, which is induced by the higher granularity of the pentacene film. The ORMOCER material properties can be tuned over a wide range and therefore they are interesting candidates for replacing inorganic gate dielectrics in various electronic applications. In contrast to BCB, which needs temperatures up to 300 °C for cross linking, the ORMOCER-based OTFTs are easily compatible with commercial polymer foils established in a reel-to-reel fabrication process due to the sufficiently low processing temperatures. Furthermore, the surface structure of ORMOCER VI favors the growth of large-sized pentacene grains, whereas we found only medium-sized grains on the untreated BCB surface, resulting in lower charge-carrier mobility values on this material. Pyo *et al.* have also demonstrated low-temperature processing of photosensitive and thus directly patternable polyimide gate dielectric layers but they resulted in OTFTs with much lower mobility values than have been achieved with the ORMOCER VI.[31] The possibility of producing high-performance OTFTs on flexible substrates with gate dielectrics which provide direct patternability and, additionally, yield passivation against humidity will further support the progress of organic electronics.

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