Two-trap model for carrier lifetime and resistivity behavior in partially annealed GaAs grown at low temperature

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We have developed a semiquantitative model based on Ostwald ripening to explain observed trends in both the carrier trapping lifetime and bulk resistivity when low-temperature-grown gallium arsenide is partially annealed. The effects of both point defects and precipitates are described independently, representing two distinct types of recombination center. The model predicts previously observed and hitherto unexplained anomalous features in the carrier lifetime and resistivity trends as the anneal temperature is increased. The predictions are supported by experimental measurements of the point defect concentration and precipitate parameters, using x-ray diffraction and transmission electron microscopy imaging, respectively.

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I. INTRODUCTION

Low-temperature-grown gallium arsenide[1–3] (LT-GaAs) is a common choice of material for many photoconductive applications, owing to its unique combination of physical properties. The characteristic short carrier lifetime (<200 fs), high resistivity, high electron mobility, and high electric breakdown field make it suitable for use in devices including ultrafast optical switches,[4] transistors,[5] and solid-state terahertz transceivers,[6–8] among others.

The optical and electronic properties of LT-GaAs, and in particular, the short carrier trapping lifetime, result from the high concentrations of native point defects, which may be introduced using nonstoichiometric molecular beam epitaxy (MBE) growth. Growth at temperatures significantly below the usual 580–600 °C suppresses the out-diffusion of arsenic, allowing an excess to be incorporated. This excess arsenic may be manifested as three distinct types of point defects: arsenic antisite (As_{Ga}), interstitial (As_i), and gallium vacancy[9] (V_{Ga}). Single crystal growth is possible down to substrate temperatures of approximately 190 °C, beyond which the strain produces grain boundaries, dislocations, and polycrystallinity. Low-temperature-GaAs is a term used to refer to material grown in the temperature range of around 190–350 °C.

In as-grown (i.e., unannealed) LT-GaAs, the electron-trapping lifetime may be as short as 90 fs,[10] owing to the rapid trapping of electrons from the conduction band into mid-gap states. These states have been shown to be associated with the ionized antisite defects, As_{Ga}^{+},[11] which act as deep donors, approximately 0.7 eV below the conduction band edge.[12]

However, the need for a high unilluminated bulk resistivity is equally important for terahertz and other photoconductive applications. Such material tends to have a low resistivity (<10 Ω cm) caused by hopping conduction between these states.[13] An additional problem is the possible saturation of the defect states, since each electron captured from the conduction band neutralizes a trap. This occurs because the electron-hole recombination time may be several orders of magnitude longer than the trapping time.[14]

These problems are conventionally overcome by annealing at high temperatures, promoting the migration of point defects to precipitates of metallic arsenic. These act as buried Schottky barriers, thereby increasing the resistivity through the creation of overlapping depletion regions.[15] In the context of a short carrier lifetime, the degradation resulting from the removal of point defects is assumed to be at least partially compensated by the high cross section of arsenic precipitates for electron capture.[16] Furthermore, saturation effects may also be overcome by the relatively large density of states in the precipitates. Typically, annealing at 600 °C is performed following growth, and this is known to increase the resistivity by up to five orders of magnitude.[13] The point defects are entirely removed in favor of large precipitates (~10 nm), but the carrier lifetime is severely compromised, often to several picoseconds.

Consequently, the annealing process represents a trade-off between a high bulk resistivity and a short carrier lifetime—properties which are simultaneously required by many appli-

cations. In this paper, we demonstrate that these simultaneous properties can be achieved by partially annealing the material, and we present a novel model to interpret the observed unusual trends in the measurable parameters, as a function of the anneal temperature. This "two-trap" model successfully connects the changing physical properties of the defects and precipitates in the material to the observed trends in the carrier lifetime and bulk resistivity.

The paper is organized into several sections as follows. In Sec. II, the annealing process is described, and the terms annealed and partially annealed LT-GaAs are defined in terms of the observable parameters. Section III describes the derivation of the two-trap model itself; whereas, Sec. IV contains a summary of the experiments performed to validate the model. The results are discussed in Sec. V and summarized with conclusions in Sec. VI.

II. ANNEALED AND PARTIALLY ANNEALED LT-GaAs

For both annealed and unannealed LT-GaAs wafers, the concentration of antisite defects, As_{Ga}, may be deduced from the lattice strain via x-ray diffraction (XRD) measurements.[9] Using the calibration found by Liu *et al.* gives

$$N = -5.9 \times 10^{17} \Delta\theta \ \mathrm{cm}^{-3}, \tag{1}$$

where $\Delta\theta$ is the splitting parameter in units of arcseconds. In the case of unannealed material, the antisite defects are assumed to be the sole trapping centers, and their number density may be related to the carrier lifetime τ via the Shockley-Read-Hall (SRH) model[2]

$$\tau = \frac{1}{v_{th}\sigma N}, \tag{2}$$

where v_{th} is the thermal velocity of the electrons, σ is the capture cross section of each point defect, and N is their number density. A scatter plot of the number density [inferred from the XRD curves using Eq. (1)] versus the carrier lifetime (measured using time-resolved photoreflectance[10]) is shown in Fig. 1 for 14 LT-GaAs wafers grown under a variety of conditions at the Cavendish Laboratory and representing both annealed (600 °C *in situ*) and unannealed wafers.

The SRH model describes only the unannealed material, with the annealed wafers exhibiting a carrier lifetime considerably shorter than that predicted if the residual antisite defects were the only traps. Thus the mechanism for trapping must differ in the case of annealed LT-GaAs. The evolution of the material properties from the unannealed state to the annealed state during the anneal process is of great interest, both for the understanding of the underlying physical processes, and to allow the optimization of the material. Many previous studies of LT-GaAs annealing dynamics have concentrated on flash anneals at high temperature. In such materials, it is assumed that all of the highly mobile point defects are depleted; yet the precipitate states do not reach equilibrium. For such systems, the unified cluster model is appropriate,[17] in which point defects are considered to be precipitates in the small diameter limit. Thus the trapping can be described by a modified SRH expression with only a single parameter: the cluster density.

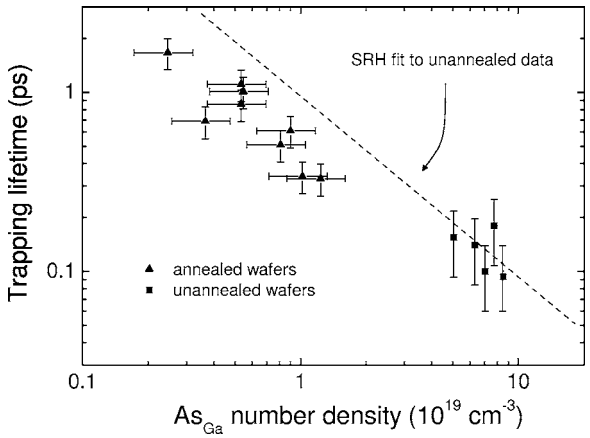

FIG. 1. Plots of the measured trapping lifetime as a function of the antisite defect density, as inferred from XRD spectra. The SRH model is fitted to the data from the unannealed wafers, and it is clear that the annealed material does not fall on the same curve, and therefore cannot be interpreted using the SRH model.

In contrast, our previous studies of the annealing process have shown that appreciable changes in the lifetime and resistivity occur for annealed temperatures far below those commonly reported.[6] Specifically, we soak-anneal *ex situ* for relatively long periods of time (up to 1 h) at temperatures in the range 250–600 °C, resulting in "partially annealed" LT-GaAs that is defined by two principal physical properties. First, the elimination of point defects from the lattice is incomplete, allowing a simultaneous existence of both point defects and precipitates. This has several beneficial effects, as will be discussed later. Second, the precipitates are allowed to achieve equilibrium with the surrounding lattice at the annealed temperature, meaning that the evolution of the precipitates with temperature is governed by energetic—rather than kinetic—considerations. Using this technique, we are able to produce LT-GaAs with a high resistivity ($>10^4\ \Omega$ cm), and essentially no compromise in the carrier lifetimes.[6]

The dynamics of the anneal processes may be investigated by monitoring the state of the material as a function of both anneal temperature and time. We have previously found that the trends displayed by the carrier lifetime and resistivity are very different from those which may be inferred from interpolating the extremes of unannealed and *in situ* annealed LT-GaAs. Rather than a monotonic rise, the carrier lifetime decreases to a minimum value as the anneal temperature is initially increased. The resistivity increases to a plateau, exhibiting saturation with increasing temperature, before rising again as the temperature is increased further.

For partially annealed LT-GaAs, large concentrations of both point defects and precipitates are present in equilibrium, and it is the interaction between these defect types that is responsible for the anomalous trends observed when annealing. The role of precipitates in trapping has been long disputed[18,19]: indeed our studies, and those of others, have shown that under some circumstances, the carrier lifetime actually decreases when the material is annealed. This effect has been frequently reported in previous work, without consistent explanation.[20,21]

III. THE TWO-TRAP MODEL

In this study, we show that the annealing behavior in the partially annealed regime is most naturally explained using a novel model that considers point defects and precipitates as distinct but coexisting entities. This distinction is important because small precipitates and complexes are thought to be present in the as-grown state, and energetically behave very differently to single point defects. The "one-trap" SRH model must be extended to account for multiple trap types, and the dynamics of the precipitate formation cannot be explained by simple diffusion. This section describes a semiquantitative model that is able to account for the observed trends in the electronic parameters, and the dynamic transition between these states.

At any given annealing temperature, the point defect level rapidly achieves a nonzero state of equilibrium. This is stable because the migration of vacancies to voids in the lattice reduces the diffusion coefficient for the antisite defects, effectively locking the concentration. This is entirely consistent with the vacancy-assisted diffusion model proposed by Bliss *et al.*[22] In this case, the solution to the spherical diffusion equation simplifies to Eq. (3) when the annealing time is sufficiently long for an equilibrium state to be achieved. N is the number density of point defects, N_0 is the initial number density following growth, and τ_V and τ_{As} are the characteristic diffusion times of the vacancy and antisite defects, respectively, which are both functions of the annealed temperature, T_A.

$$N(T_A) = N_0 \exp\left[- \frac{\tau_V(T_A)}{\tau_{As}(T_A)} \right]. \tag{3}$$

The diffusion time functions may be estimated by finding the enthalpy of migration from an Arrhenious plot fitted to measured data.

Similarly, at any given annealed temperature, the precipitate diameter d_{ppt} may be independently described by the following phenomenological exponential growth function:

$$d_{ppt}(T_A) = d^0_{ppt} + d^1_{ppt} \exp\left(\frac{3T_A}{T^0_A} \right). \tag{4}$$

The exponential relationship is consistent with a precipitate diameter fixed by thermodynamic considerations: a temperature-dependent equilibrium is reached when the surface free energy of the interface is equal to the strain energy associated with the precipitate volume. The mechanism for the change in diameter is Ostwald ripening, in which the larger precipitates grow at the expense of the smaller ones as the temperature increases, with material transferred along stress-induced concentration gradients. This is quite different from the precipitate accretion process that would result from a simple diffusion mechanism.

The total arsenic atomic excess, N_0, is known from the XRD parameter for the unannealed material, in which little or no precipitation has occurred. Equations (3) and (4), together with an extra parameter to describe the net loss of arsenic from the crystal during the annealing, may then be used to calculate, as a function of anneal temperature, the observable parameters required to describe completely the point defect and precipitate content of the LT-GaAs. N and d_{ppt} can be deduced by conservation of the total arsenic atomic content. The precipitate number density N_{ppt} and interprecipitate spacing can then subsequently be deduced, by conserving the total volume of metallic arsenic, using a value of 4.6×10^{22} cm^{-3} for the atomic number density of metallic arsenic.

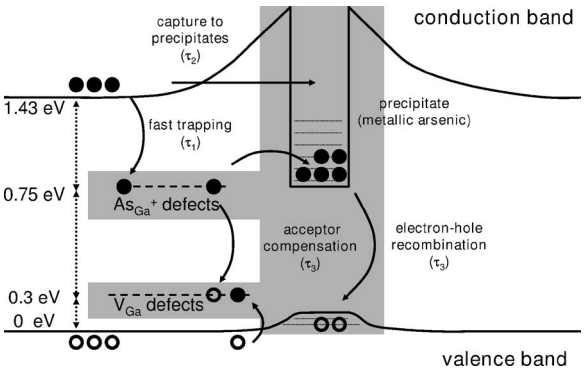

FIG. 2. Schematic diagram of the band structure of LT-GaAs in the vicinity of a metallic precipitate. The energy levels associated with the point defects are also illustrated.

The model's derivation of the carrier lifetime from these parameters is based on the assumption that both point defects and precipitates are able to independently capture electrons, and in the latter case, with an effective cross section that is a simple function of the precipitate diameter. The conduction band optically injected carrier density n is, in general, given by a rate equation

$$\frac{dn}{dt} = \frac{\eta P}{h\nu V} - \sum_i \frac{n}{\tau_i}, \tag{5}$$

where η is the external quantum efficiency, P the total incident optical power, $h\nu$ the average optical photon energy, and V is the excitation volume. τ_i is the carrier lifetime with respect to the ith trapping mechanism. The model considered here uses three such mechanisms for decay: rapid capture by antisite defects, τ_1; capture by precipitates, τ_2; and recombination across the band gap, τ_3. The latter corresponds to the lifetime of semi-insulating GaAs and is a constant of order 50 ps-1 ns depending upon purity. Figure 2 diagrammatically summarizes the various processes considered here, in terms of the band structure of LT-GaAs.

The occupation of the point defect states n_1 may be described by a simple rate equation

$$\frac{dn_1}{dt} = \frac{n}{\tau_1} - \frac{n_1}{\tau_2} - \frac{n_1}{\tau_3}. \tag{6}$$

For a point defect trap density of N, each trapped electron will neutralize one ionized antisite defect. The trapping time is thus given by the modified SRH expression as

$$\tau_1 = \frac{1}{\sigma v_{th}(N - n_1)}. \tag{7}$$

The equivalent cross section for the precipitates must be modified from that of their physical size, since it is the sur-

rounding depletion region that dictates the capture probability. Thus we use

$$\tau_2 = \frac{1}{\sigma_{ppt} v_{th} N_{ppt}}, \tag{8}$$

$$\sigma_{ppt} = \pi \left(\frac{d_{ppt} + d_{dep}}{2} \right)^2, \tag{9}$$

where σ_{ppt} is the precipitate cross section. d_{dep} represents the extent of the depletion region and is here left as a fitting parameter. The thermal velocity takes its room temperature value of 3.8×10^5 ms^{-1}, and σ is estimated (from Fig. 1) to be 3×10^{-15} cm^2. Thus given the number density of the point defects and the precipitate mean diameter and number density, the net carrier lifetime can be found by solving Eqs. (5)–(9) numerically for the steady state.

In a similar manner, the bulk resistivity of the LT-GaAs may be calculated using the same parameters that describe the defect state of the material. In as-grown LT-GaAs, past studies of the temperature dependence of the resistivity have indicated that its value is governed by hopping conduction between defect sites, explaining why unannealed LT-GaAs is unusually conductive. The hopping resistivity associated with the antisite defects is given by[13]

$$\rho_{hop} = \left(\frac{32\pi\alpha}{N} \right)^{1/2} \frac{kT}{e^2 \delta} \exp\left(2.1 \frac{\alpha^3}{N} \right)^{1/4} \tag{10}$$

with α^{-1} as the wave function decay distance and δ as the hopping attempt frequency. Thus the hopping component for the resistivity increases dramatically and without limit as the point defects are eliminated during the annealing.

There is also a component of resistivity that arises from conventional scattering of residual carriers in the conduction band. These are present owing to the ionization of the antisite defects (deep donors) and thermal excitation. For low defect densities, this is the dominant effect, and is dependent upon the equilibrium carrier density impeded by the effect of depletion regions surrounding the precipitates. The conduction band resistivity is given by the standard expression

$$\rho_{cb} = \frac{1}{ne\mu_e} \tag{11}$$

with the electron mobility μ_e, an activated function of the anneal temperature, seen to rise from 2 cm^2 V^{-1} s^{-1} for as-grown material to 3000 cm^2 V^{-1} s^{-1} for fully annealed LT-GaAs. The net (measured) resistivity is thus found by assuming that the components contribute in parallel.

Given the XRD data to generate N_0, τ_V, and τ_{As} as input parameters, the model was used to predict the trends in the point defect density, net carrier lifetime, resistivity, and the precipitate diameter, spacing and number density, all as a function of the annealed temperature.

IV. EXPERIMENTAL PROCEDURE

To test the two-trap model, we systematically characterized the change in lifetime, resistivity, point defect concentration, and precipitate parameters as the LT-GaAs was annealed. A series of experiments was performed on LT-GaAs wafers that were grown by MBE onto undoped (001) semi-insulating (SI)-GaAs substrates. They incorporated an epitaxial buffer layer of GaAs grown at high temperature, and 1 μm of GaAs grown at a nominal temperature of between 200 and 230 °C at a rate of approximately 1 μm/h, with the temperature estimated using a thermocouple. The samples were subsequently annealed *ex situ* in a rapid thermal annealer under a nitrogen atmosphere and in contact with SI-GaAs wafers to reduce arsenic loss. Ten-minute anneals were used throughout to ensure that quasi-equilibrium states were achieved. The temperature was varied from sample to sample in 25 °C increments, covering the range between 250 °C and 600 °C.

Rather than attempting to infer the defect and precipitate state of the LT-GaAs from the lifetime and resistivity parameters in a phenomenological manner, we have measured the point defect and precipitate concentrations independently, using XRD and transmission electron microscopy (TEM) images, respectively. XRD rocking curves were collected for each sample using a Bede model 200 double-axis x-ray diffractometer, referenced to a GaAs crystal and diffracted from the (004) plane of the LT-GaAs sample. The diffraction peak from the LT-GaAs layer was compared in each case to the corresponding Bragg maximum from the SI-GaAs substrate to generate the splitting parameter $\Delta\theta$.

TEM images were used to characterize the mean size, spacing, and number density of precipitates: these three parameters being sufficient to describe the precipitation process completely. Samples of an LT-GaAs wafer were annealed over a range of temperatures, and prepared for TEM imaging as follows. The cross-sectional TEM specimens, with [110] surface normal orientation, were thinned to electron transparency by conventional mechanical polishing followed by Ar^+ ion milling at 4 kV beam energy and grazing angles. In order to minimize radiation damage and contamination, the samples were transferred to a Technoorg-Linda low-energy ion beam miller operating at 200 V. These specimens were examined using a JEOL 2010F field emission gun TEM operating at an accelerating voltage of 200 kV.

The size of precipitates was measured directly from the TEM images obtained from high-resolution TEM (HRTEM) imaging. The density of precipitates is a measure of the number of precipitates per unit volume V (the product of the sample area and the average thickness). An electron energy-loss spectroscopy (EELS) spectrum is used to measure the sample thickness t, where

$$t = \lambda \ln\left(\frac{I_t}{I_o} \right). \tag{12}$$

λ is the average mean free path, and I_t and I_o are the areas under the whole spectrum and the zero loss peak (ZLP), respectively.

The lifetime was measured using time-resolved photoreflectance using 90 fs pulses from a Ti:Sapphire laser operating at 800 nm.[10] The laser beam was divided using a beam splitter, and an optical time-delay stage allowed a pump-

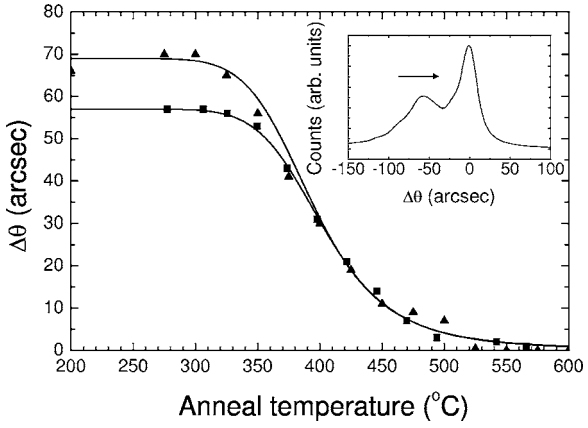

FIG. 3. Plots of the XRD peak separation (proportional to the antisite defect density) as a function of the annealed temperature. Experimental data from two samples are plotted, with curves for the corresponding fits from the model [Eq. (3)]. The initial difference in the as-grown wafers is overcome as the annealed temperature is raised above 375 °C. A typical XRD spectrum is shown in the inset.

probe measurement to be collected, indicating the carrier density as a function of time. The lifetime was then derived in each case by fitting to the exponential decay of the signal. The accuracy of such measurements is dependent upon the wavelength and power of the exciting laser, as well as the correct interpretation of various artifacts that can arise. However, the technique provides valuable and quantitative estimates for the lifetime, which are sufficient for comparative measurements.

The resistivity was characterized through measurements of the two-terminal resistance of test devices, each with a 5 μm $\times$ 5 μm photoconductive gap.[23] The device consists of two planar metal electrodes of 400 nm thickness, lithographically patterned onto the surface of the material under test. A value for the resistance was derived using a source-measure unit in the ohmic (low bias) limit—the contact resistance was negligible.

V. RESULTS AND DISCUSSION

In this section, we sequentially compare the model's predictions with experimental results for each of the six considered observable parameters: the XRD peak separation, the mean diameter, number density, and spacing of the precipitates, as well as the carrier lifetime and the resistivity. In each plot, the points correspond to individual experimental measurements, with the solid curves representing the model's predictions.

The XRD spectra were evaluated for annealed temperatures across the range, for a variety of LT-GaAs wafers. The peak separation $\Delta\theta$ between the SI-GaAs substrate lattice (used to define $\Delta\theta=0$) and the LT-GaAs epilayer is plotted as a function of the annealed temperature for two LT-GaAs examples in Fig. 3. As the temperature increases, the LT-GaAs lattice parameter relaxes to that of the substrate (inset), as the point defects are removed. At temperatures below 300 °C, there is no removal of point defects. Increasing the temperature from 350 °C to 450 °C sees the removal of the majority of the defects, with total extinction achieved at approximately 550 °C.

The curves derived using the diffusion lifetimes from Eq. (3) are overlaid upon the experimental data points in Fig. 3 for the two LT-GaAs wafers. The fit is accurate across the entire range of annealed temperatures. Despite the fact that the original number of incorporated defects varies considerably between the wafers (a result of a small variation in the growth temperature), the curves converge upon annealing, intersecting at approximately 375 °C. This is a direct consequence of the lattice vacancies acting to normalize the diffusivity of the antisite defects (vacancy-assisted diffusion), and thus the curves cannot be transformed between different wafers either by translation or scaling. In the temperature regime where no point defects remain (>550 °C), precipitates have formed to conserve the total arsenic content. Below this temperature, however, the point defects account for much of the excess arsenic in the crystal.

In many MBE chambers, precise measurement and control of the substrate temperature during low-temperature growth is difficult, since the instruments will be operating beyond their designed temperature range. Thus LT-GaAs grown under nominally identical conditions is notoriously inconsistent, explaining the diverse and often contradictory reported behavior. Since the annealing temperature *can* be accurately controlled, the LT-GaAs consistency may be improved by adopting this anneal process.

Figure 4 shows the evolution of the equilibrium mean precipitate diameter, number density, and spacing as functions of the annealed temperature, as deduced from the TEM images (inset). For the images corresponding to annealed temperatures of 250 °C–350 °C, the precipitates are less well defined in comparison to the higher temperature annealed samples. There might be more precipitates, but shielded by point defects, where local regions appear almost amorphous. In Fig. 4(a), the mean diameter increases from 1.54 nm at 250 °C to 9.1 nm at 600 °C. This compares well with the predictions of Eq. (4), where d^0_{ppt}, d^1_{ppt} and T^0_A are fitting parameters obtained from the data. These parameters appear to adopt similar values even for LT-GaAs wafers with very different growth conditions and initial point defect concentrations, and also agree well with values reported elsewhere.[24]

In Fig. 4(b), the number density rises to a maximum value between 350 and 400 °C, before falling to much lower values, which is in good agreement with the model. The number rises rapidly with initial increases in temperature, as point defects condense to form many small precipitates, stabilizing when the point defect concentration is depleted. Further increases in temperature allow a larger precipitate diameter to be energetically preferred, reducing the number density as the smaller precipitates dissolve to provide material for the larger ones to grow. Finally, Fig. 4(c) shows the corresponding minimum in the mean precipitate separation, again, in good agreement with the model.

Unexpectedly, our comparisons of TEM and XRD data indicate that the precipitates contain far more arsenic than can be accounted for by accretion of the antisite defects alone. This case is made more surprising by the likely loss of

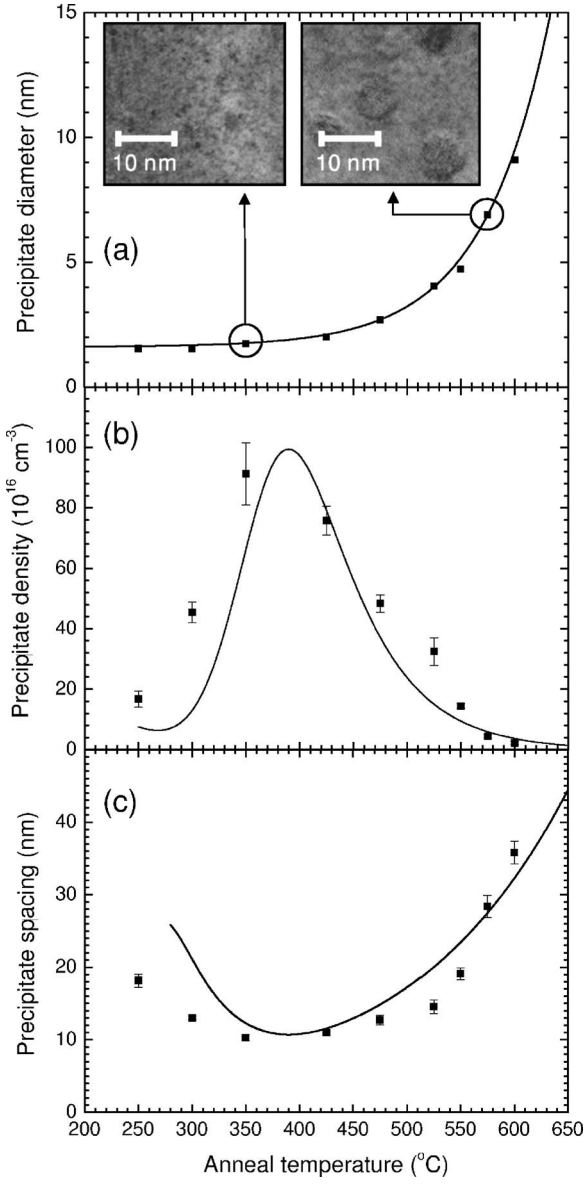

FIG. 4. Plots of the measured (a) mean precipitate diameter, (b) mean precipitate number density, and (c) mean precipitate spacing as functions of the annealed temperature. The points are derived from TEM data, with two images shown inset for the 350 °C and 575 °C samples. An exponential growth curve provides a good fit to the precipitate diameter data, as described by Eq. (4). The curves plotted for the density and spacing are derived using the model, with no further fitting parameters.

arsenic from the crystal surface during annealing. There are two possible explanations: one is that a significant proportion of the excess arsenic is incorporated as interstitial point defects, which are not thought to cause significant strain. Since the As_i defects are very much more mobile than the As_{Ga} defects, it is expected that they would diffuse to form precipitates at a much lower temperature than that required to cause significant migration of the As_{Ga}. However, the presence of this type of defect in LT-GaAs is still under dispute.[25] Another possibility is the presence of small arsenic precipitates, clusters, and complexes even in the as-grown state. This is consistent with extrapolating the exponential

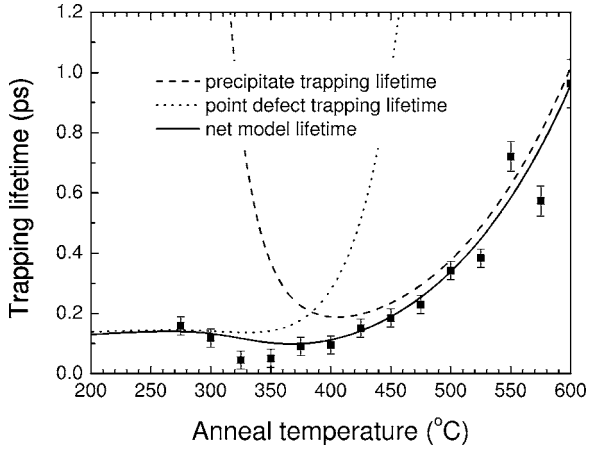

FIG. 5. Plots of both modeled and experimental trapping lifetimes for a LT-GaAs wafer as a function of the annealed temperature. The two components of the lifetime, τ_1 and τ_2, are also shown, representing the trapping lifetimes owing to the point defects and precipitates (dotted and dashed curves, respectively). The net trapping time is shown as a solid curve and is derived from the sum of the individual trapping rates.

curve in Fig. 4(a) back to the growth temperature, which suggests that precipitates up to 1.6 nm are stable at the substrate growth temperature of ~200 °C.

Figure 5 shows the equilibrium $1/e$ trapping lifetime as a function of the annealed temperature. The dotted curve shows the predicted lifetime with respect to the trapping by the antisite point defects alone, τ_1. As might be expected from the XRD measurements, this rapidly increases beyond 350 °C as the point defects are eliminated. The dashed curve indicates the trapping lifetime with respect to the precipitate trapping, τ_2. In this case, the attractive potential is provided not by a point positive charge (as in the case of an antisite defect) but by the depletion region surrounding the metallic precipitate. This lifetime is seen to decrease as both the trapping cross section (precipitate diameter) and the number density of the precipitates increase owing to nucleation from clusters of point defects. The subsequent increase occurs for temperatures at which the total precipitate volume stabilizes, since the Ostwald ripening process causes a net decrease in the precipitate number density. The overall lifetime is given by the solid line in Fig. 5, and reproduces the measured data well over the range shown. The lifetime decreases to a minimum of ~50 fs at an annealed temperature of 325 °C, before rising rapidly as the temperature is increased further.

Figure 6 shows the measured and modeled resistivity as a function of the annealed temperature. In this plot, the experimental points have been normalized to the model curves, since the quantity measured was the resistance of a test device. The resistivity of the material is plotted in terms of its two components. The hopping resistivity (dotted line) associated with the point defects becomes large once significant depletion of the antisite defects occurs. The component of resistivity caused by scattering in the conduction band (dashed line) depends primarily on the equilibrium carrier density. For as-grown samples with a large population of shallow and deep donor levels, the majority of the carriers

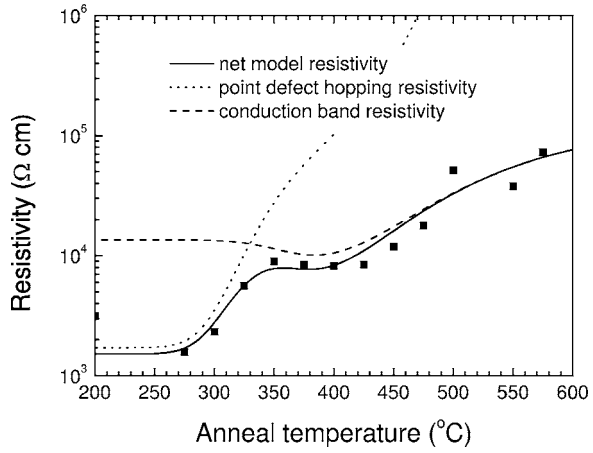

FIG. 6. The bulk resistivity plotted as a function of the anneal temperature showing both experimental data and predictions from the model (solid curve). Again, the model data may be shown in terms of the individual contributions from the conduction band scattering, ρ_{cb} (dashed curve), and hopping in the point defects, ρ_{hop} (dotted curve). Significantly, the resistivity plateau between 325 and 400 °C is predicted by the model.

will not be intrinsic. As the carrier lifetime increases upon annealing, both the mobility and the equilibrium carrier density will increase correspondingly. However, this effect is more than offset by the increase in size of the precipitates, which expands the depletion regions, causing a substantial increase in the conduction-band resistivity beyond that expected in defect-free GaAs.

The net resistivity is seen to increase monotonically with temperature, reaching a plateau in the range 350–425 °C after rising by one order of magnitude. A further rise in temperature leads to an exponential increase without limit, giving another order of magnitude at 600 °C. These trends are reproducible across several independent LT-GaAs wafers, although some variation in the temperature thresholds is observed.

It is interesting that significant changes occur in both the carrier lifetime and the resistivity even for temperatures as low as 275 °C, where no point defect migration is activated. The amount of arsenic available for the creation of precipitates has previously been calculated from conservation of the total excess arsenic in the crystal. During the annealing process, the average precipitate size grows as Ostwald ripening is activated. At low annealing temperatures, this is able to occur even before the migration of antisite defects is activated, qualitatively explaining the changes in the lifetime and resistivity for sub-300 °C annealed temperatures. Furthermore, the continued evolution of both the lifetime and the resistivity at temperatures beyond those at which all of the point defects are eliminated is evidence for the participation of precipitates in trapping.

VI. SUMMARY

In summary, we have introduced a semiquantitative model to explain the hitherto anomalous annealing characteristics of our LT-GaAs. These trends (namely the lifetime minima and the resistivity plateau) may be considered anomalous because they have been repeatedly observed, but cannot be explained by simple diffusion of the point defects, or by the SRH theory.

The two-trap model is able to simultaneously account for the observed minimum in carrier lifetime, together with a plateau in the bulk resistivity. The mechanism depends upon a simultaneous presence of both point defects and precipitates, with excess arsenic redistributed during the annealing to both defect types by vacancy-assisted diffusion and Ostwald ripening, respectively. An understanding of these processes in partially annealed LT-GaAs should allow highly consistent material to be produced.

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