Top-gated field-effect transistor and rectifying diode operation of core-shell structured GaP nanowire devices

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We have fabricated top-gated GaP nanowire field-effect transistors using core-shell structured GaP nanowires grown by a chemical vapor deposition method. As expected, based on results of a thin Ga_2O_3 shell serving as a gate oxide, our top-gated GaP nanowire FETs exhibited more effective gate-channel coupling when compared to the conventional back-gated one. Above the threshold voltage of 1.5 V, diode like *I-V* characteristics were observed between the source and top-gate electrode. This can be explained by the formation of a midgap GaP/wide-gap Ga_2O_3 heterojunction. Measured current from in between the source and top gate shows extreme sensitivity toward ultraviolet illumination, which can be attributed to the electron-hole pair generation in the Ga_2O_3 layer. The first-principle electronic structure calculations on Ga_2O_3 crystal revealed a reduction in the band gap (4.8 eV$\rightarrow$3.8 eV) due to the development of oxygen vacancy states in the forbidden band gap.

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Since the first demonstration of molecular-scale field effect transistors (FET)[1] using a single wall carbon nanotube, there has been a significant amount of research efforts to realize and optimize electronic devices based on one-dimensional nanostructures.[2–7] Among them, semiconducting nanowires could be more advantageous for nanoscale device applications, since they are inherently semiconducting and can be doped relatively easily in a controlled manner. Moreover, recent advances in growth technology make it possible for a single semiconductor nanowire to be constructed as an electronic component, such as a *p-n* junction diode,[8] a coaxially gated transistor,[9] and a semiconductor quantum well by using one-dimensional heterostructures.[10–15] This would be a major breakthrough in bottom-up assembled molecular-scale electronics.

Here, we report the fabrication of top-gated GaP nanowire FETs and investigate the electrical transport properties and photoresponse of these devices. Because our GaP nanowires have a core-shell structure with the outer Ga_2O_3 shell, we fabricated top-gated GaP FETs using an intrinsic Ga_2O_3 shell layer as a gate dielectric, and measured the electrical transport from these devices. Improved channel-gate coupling was observed in our top-gated GaP FET below the threshold gate voltages of 1.5 V. When we applied bias voltages higher than the threshold voltages between the source (drain) and top gate, a rectifying diode behavior was observed from the devices, which could be explained by the formation of heterojunction in the midgap GaP/wide-gap Ga_2O_3. Moreover, we have discovered that current through the heterojunction increases with ultraviolet (UV) illumination, due to carrier generation in the outer Ga_2O_3 shell layer.

For device fabrication, we have used a high quality GaP nanowire grown by chemical vapor deposition. Nanowires were grown using a direct vaporization of mixtured Ga/GaP powder on an alumina substrate, on which NiO or CoO catalyst nanoparticles were evenly distributed.[15] Inset of Fig. 1(a) shows the high-resolution transmission electron microscope (HRTEM) image of a typical GaP nanowire. The HRTEM and selected area electron diffraction (SAED) analysis clearly indicate that our GaP nanowire has a typical core-shell structure with a zinc-blende structured GaP core, and that the outer oxide has a double layer of orthorhombic structured $GaPO_4$ and armorphous Ga_2O_3 layer.[15] The nanowires show very clean surfaces and uniform diameter at optimum process conditions, which make it possible to expect a uniform oxide shell thickness from each nanowire. To make source-drain contacts on an individual GaP nanowire, electrode patterns were generated using an electron beam lithog-

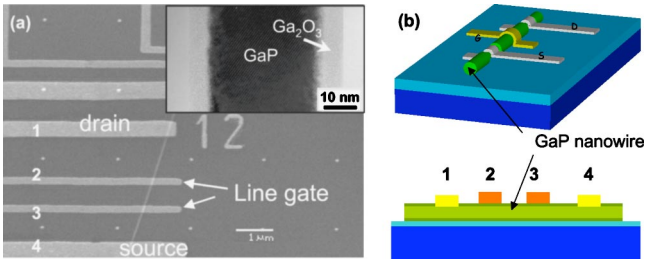

FIG. 1. (a) SEM image of the typical top gate GaP nanowire FET. Inset, HRTEM image of a single crystalline GaP nanowire that showed a GaP core with the Ga_2O_3 shell layer. (b) Schematic diagram of a top-gate GaP nanowire FET. The bottom figure shows the side view of a top-gate FET. While electrodes 1 and 4 can be used as source and drain electrodes, 2 and 3 are used as top gates.

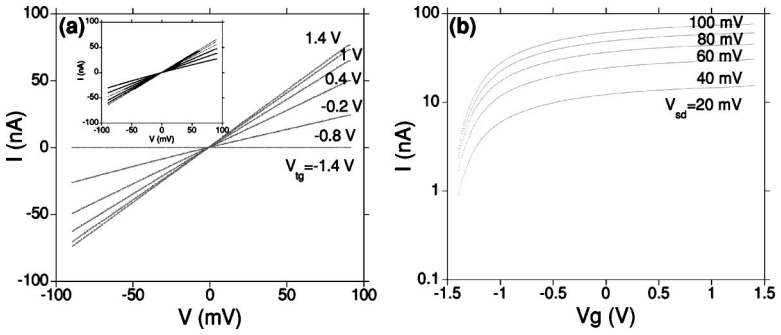

FIG. 2. *I-V* curves of GaP nanowire between the electrodes 1 and 4 as a function of top-gate voltage V_{tg}. Top gate voltages of −1.4–1.4 V was applied. Inset shows *I-V* curves of GaP nanowire as a function of back-gate voltages. We applied −1.4–1.4 V back-gate bias for comparison. All the measurements were conducted at room temperature. (b) I-V_g curves of a GaP nanowire FET at different bias voltages at room temperature.

raphy technique. Then they were etched with 3% HF solution for 6–10 s to remove the outer Ga_2O_3 oxide shell layer. Then, 10 nm Ti and 40 nm Au were evaporated successively without breaking the vacuum, followed by a gentle lift-off process. The top-gate electrodes were fabricated by defining electrode patterns in between the source and the drain electrodes with an extra electron beam lithography step and an Au lift-off without an oxide etching process. Figure 1 shows the SEM image of a typical top gated GaP FET. As is shown in the schematic diagram of Fig. 1(b), the source and drain contact electrodes are defined on top of the GaP core after etching an oxide shell layer, while top-gate electrodes are patterned directly on top of the oxide layer.

Figure 2 shows the electron transfer characteristics measured from the GaP nanowire device in Fig. 1(a). While electrodes 1 and 4 were used as source and drain electrodes, electrode 2 and 3 were used as top-gate electrodes. As shown in Fig. 2, the conduction channel in the GaP nanowire FET closes almost completely around −1.5 V with a top gate, thereby exhibiting a strong *n*-doped behavior. Inset of Fig. 2(a) shows the (*I-V*) characteristics measured at different back-gate bias voltages. Here, the same gate bias voltages as the top gate has been used for comparison. It is clear that the top gate shows better gate coupling when compared with back gate. If we assume that the top gate covers a large portion of the nanowire surfaces, we can approximate the system as a coaxial cylinder. The capacitance of a coaxial cylinder can be calculated as $C=2\pi\varepsilon\varepsilon_o L/\ln(r_a/r_b)$, where L is a length of a cylinder and r_a and r_b represent the outer and inner radius of a coaxial cylinder, respectively. To calculate the coaxial capacitance, we assumed that the dielectric constant of our Ga_2O_3 shell was 10, and geometrical parameters such as $L=3.5$ μm, $r_a=50$ nm, and $r_b=38$ nm were measured from SEM images of the device. The calculated capacitance of a coaxial GaP nanowire is around 7.1×10^{-15} F, which is an order of magnitude larger than the back-gate capacitance ($\sim2.34\times10^{-16}$ F). In the case of back-gate capacitance, the capacitance was calculated with a cylinder on an infinite plane model, $C_{bg}\approx2\pi\varepsilon\varepsilon_0 L/\ln(h/r)$, where r is the radius of a cylinder and h is the thickness of gate dielectric materials. Figure 2(b) shows I-V_{tg} characteristics of the same device measured at different bias voltages. Due to the break down of the Ga_2O_3 insulating layer, we could measure only down to $V_{tg}=-1.4$ V for this sample. The typical depletion onset voltage with a top gate is around −1.4 to −1.8 V. When a Si back gate with 200 nm SiO_2 dielectric layer was used to measure the transistor, complete depletion of the GaP channel occurs only at gate voltages larger than −10 V. Calculated mobility from this device is around 7 cm^2/V s, while most of our GaP FETs have mobility values of 6–22 cm^2/V s. Our GaP FETs have rather low mobility values compared with their bulk form (160 cm^2/V s), which might be due to the diffusive nature of electrical transport in GaP nanowire devices. Such a diffusive transport in GaP nanowires might come from surface scatterings between inner GaP shell and outer Ga_2O_3 layer, or due to the interface scattering at metal/nanowire contact regions.

When we apply high bias voltages in between the contact electrode and top gate, current starts to flow. Figures 3(a) and 3(b) show *I-V* characteristics measured between electrodes 1 and 2 (source and top gate), and 2 and 4 (drain and top gate),

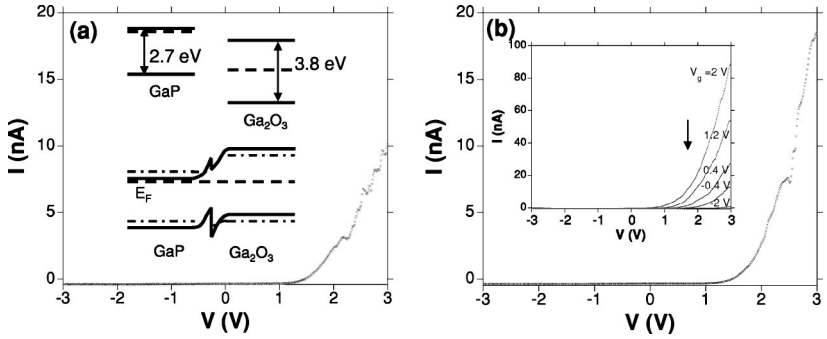

FIG. 3. *I-V* curves between electrode (a) 1 and 2, and (b) 2 and 4, respectively, at 4.2 K. Here, the direction of forward bias is from the source to the top gate. Inset of (a) shows a schematic band diagram for the GaP/Ga_2O_2 junction. Inset of (b) shows back-gate modulated *I-V* curves from electrodes 2 and 4. The top-most curve corresponds to the *I-V* measured at $V_{bg}=2$ V, and current decreases while we decrease V_{bg}, thereby exhibiting *n*-type conduction.

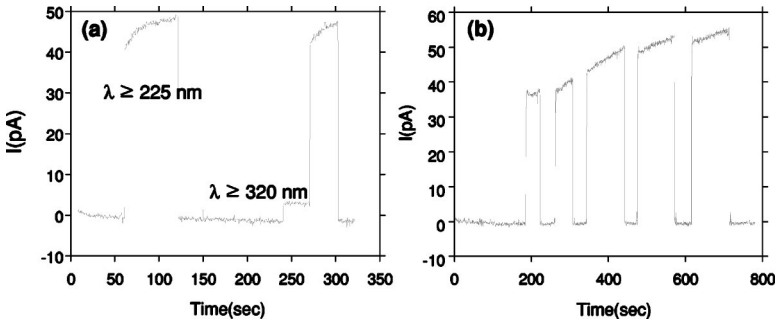

FIG. 4. UV-dependent transport curves from electrodes (a) 2–3, and (b) 1–2. The power intensity for the two wavelength regions are kept the same during measurement.

respectively, at 4.2 K. Highly nonlinear, diodelike *I-V*'s are observed in both cases, which supports the break down of the Ga_2O_3 as an insulating layer. The current increases after the threshold voltage of 1.2 V for the forward bias condition, while break down does not occur over −3 V for the reverse bias condition. Such rectifying behavior persisted up to room temperature. To explain such a rectifying behavior, we modeled the system as a heterojunction of two semiconductors with different gap energy. The inset of Fig. 3(a) shows a schematic diagram of the system. When the *n*-doped smaller gap GaP (~2.7 eV) was brought into contact with the slightly doped wide gap Ga_2O_3 (~3.8 eV), the Fermi level (E_F) is constant across the junction by transferring electrons from the smaller gap GaP to Ga_2O_3. This makes band bending of the conduction band, and valence band, as is denoted in the schematic diagram. The current increases exponentially in the forward bias region, due to the lowering of the barrier for electron transport, while barrier height increases for reverse bias regions.

We also studied the gate dependence of the rectifying junction. Inset of Fig. 3(b) shows *I-V* curves from the GaP-Ga_2O_3 heterojunction with back-gate voltages from −2 to 2 V. Current from the GaP-Ga_2O_3 heterojunction increases with positive back-gate bias, indicating *n*-type gate response. Such an *n*-type response can be expected because our GaP nanowire acts as an *n*-doped semiconducting channel. When we applied negative gate bias to the heterojunction, electron depletion occurred in the GaP layer, thereby suppressing the electron transfer from GaP to Ga_2O_3 layer.

Finally, to investigate the origin of the UV response from our GaP nanowire FETs, we measured the *I-V* characteristics of the source (drain)-top gate, or between two adjacent top gates with illuminating UV lamps. Figures 4(a) and 4(b) show current measured from the two adjacent top gates (electrodes 2 and 3), and source top gates (electrodes 1 and 2), respectively. As shown in the figures, a sharp increase in conductance occurs at UV illumination. When the sample was illuminated with UV with $\lambda \geqslant 320$ nm, a small steplike increase was observed, while a sharp increase in conductance occurred with a $\lambda \geqslant 225$ nm UV exposure. Such an abrupt increase in conductance can be explained by charge carrier generation in the outer Ga_2O_3 shell layer with UV illumination, though there remains a possibility of a heating effect at the contacts. However, the UV source used for this experiment was equipped with infrared filters to avoid a possible heating problem, and we did not see a noticeable change in conductance over extended UV illumination.

We have performed first-principle electronic structure calculations based on VASP[16] to closely examine the relationship between the UV illumination and increased conductance in the Ga_2O_3 shell. Initially, we examined the equilibrium geometry of the monoclinic phase of bulk gallium oxide with monoclinic unit cell (a_0=12.23 Å, a_0=3.04 Å, a_0=5.8 Å, β=103.7° $C2/m$) and defective structures using $1\times2\times1$ supercell, containing 16 Ga and 24 O atoms. The electronic eigenstates are expanded in terms of the plane-wave basis set with a cutoff energy up to 396 eV. The exchange-correlation potential was described within the generalized gradient approximation (GGA),[17] and the Brillouin-zone integrations were replaced with summation over uniform mesh of 64 *k* points. Due to the differences in the nearest neighbor configurations, there were three possible types of oxygen vacancy sites. The left-hand panel of Fig. 5 shows the atomic structure of pristine gallium oxide and the three possible oxygen vacancy sites. All geometries were optimized until the remaining forces were smaller than 0.02 eV/Å. The de-

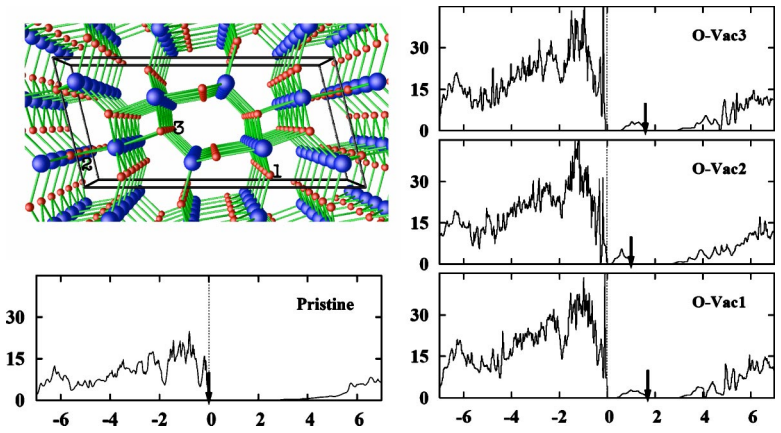

FIG. 5. The top-left figure shows the atomic structure of Ga_2O_3 with three possible oxygen vacancy sites. Other figures show the density of states (DOS) of pristine, and the three different oxygen vacant Ga_2O_3, respectively. The gray lines in atomic structure show the unit cell geometry of β-Ga_2O_3 and numbers are for the three types of oxygen vacancies. The energy level of each DOS plot is adjusted for the origin to be the valence band edge of pristine Ga_2O_3 structure. The Fermi level (the energy for the highest occupied states) is represented with the arrow for each case.

tailed electronic structure of each geometry is shown in the plot of density of states in Fig. 5. In all oxygen vacant structures, the vacancy induced states are developed in the previously forbidden gap of the pristine structure. The vacancy-induced states are occupied by two electrons, thus the oxygen vacancy acts as a donor. The calculated band gap energy and the donor level with respect to the conduction band edge of each structure are summarized in Table I. Decreased band gap energy of oxygen vacant Ga_2O_3 structures (band gap of 3.47–3.85 eV, while experimentally found band gap of Ga_2O_3 bulk is around 4.2–4.8 eV) matches well with the UV energy ($\lambda \geqslant 320$ nm, 3.87 eV) that we used to excite the current flow in the Ga_2O_3 layer.

In summary, we have fabricated top gate FETs that can be used as rectifying diode at the same time with core-shell structured GaP naowires. Improved gate to channel coupling was observed from our top-gated GaP FET and *n*-type conduction with a large on/off ratio was observed. After the threshold voltage, top-gate contact serves as a rectifying diode. When the devices were illuminated by UV lights with $\lambda \geqslant 320$ nm, a sharp increase in conductance was observed from the Ga_2O_3 shell layer, which supports the idea of carrier generation and conduction in the Ga_2O_3 layer. *Ab initio* quantum mechanical molecular dynamic calculations based on VASP showed a decreased band gap energy, due to oxygen vacancies, which explain the observed UV enhanced conduction in the Ga_2O_3 shell layer.

TABLE I. The calculated band gap energy and the donor level of pristine Ga_2O_3, and three distinguishable oxygen vacancy configurations. The values in parentheses are estimated band gap scaled with the same ratio of an experimentally measured value, and a calculated one in pristine Ga_2O_3 crystal. The donor level exists with respect to the conduction band edge.

	Coordinate number	E_{don} (eV)	Gap energy (direct)
Pristine			2.66 (4.2–4.8 eV)
O-Vac-1	3	−1.33	2.23 (~3.5 eV)
O-Vac-2	3	−1.70	2.44 (~3.9 eV)
O-Vac-3	4	−1.30	2.20 (~3.5 eV)

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[1] S. J. Tans, A. R. M. Verschueren, and C. Dekker, Nature (London) **393**, 49 (1998).
[2] A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker, Science **294**, 1317 (2001).
[3] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, Nature (London) **424**, 654 (2003).
[4] Y. Cui, X. Duan, J. Hu, and C. M. Lieber, J. Phys. Chem. B **104**, 5213 (2000).
[5] Y. Huang, X. Duan, Y. Cui, L. J. Lauhon, K.-H. Kim, and C. M. Lieber, Science **294**, 1313 (2001).
[6] J.-R. Kim, H. Oh, H. M. So, J.-J. Kim, J. Kim, C. J. Lee, and S. C. Lyu, Nanotechnology **13**, 701 (2002).
[7] J.-R. Kim, H. M. So, J. W. Park, J.-J. Kim, J. Kim, C. J. Lee, and S. C. Lyu, Appl. Phys. Lett. **80**, 3548 (2002).
[8] X. Duan, Y. Huang, Y. Cui, J. Wang, and C. M. Lieber, Nature (London) **409**, 66 (2001).
[9] L. J. Lauhon, M. S. Gudiksen, D. Wang, and C. M. Lieber, Nature (London) **420**, 57 (2002).
[10] H.-M. Lin, Y.-L. Chen, J. Yang, Y.-C. Liu, K.-M. Yin, J.-J. Kai, F.-R. Chen, L.-C. Chen, Y.-F. Chen, and C.-C. Chen, Nano Lett. **3**, 537 (2003).
[11] M. T. Björk, B. J. Ohlssoon, A. I. Persson, C. Thelander, M. H. Magnusson, K. Deppert, L. R. Wallenberg, and L. Samuelson, Nano Lett. **2**, 87 (2002).
[12] Q. Li and C. Wang, J. Am. Chem. Soc. **125**, 9852 (2003).
[13] Y. Wu, R. Fan, and P. Yang, Nano Lett. **2**, 83 (2002).
[14] J.-O. Lee, H. Oh, J.-R. Kim, K. Kang, J.-J. Kim, J. Kim, and K.-H. Yoo, Appl. Phys. Lett. **79**, 1351 (2001).
[15] S. C. Lyu, Y. Zhang, H. Ruh, H. J. Lee, and C. J. Lee, Chem. Phys. Lett. **367**, 717 (2003).
[16] G. Kresse and J. Hafner, Phys. Rev. B **47**, 558 (1993); **49**, 14 251 (1994); G. Kresse and J. Furthmueller, *ibid.* **54**, 11 169 (1996).
[17] J. P. Perdew and Y. Wang, Phys. Rev. B **45**, 13 244 (1992); J. P. Perdew, J. A. Chevary, S. H. Vosko, K. A. Jackson, M. R. Pederson, D. J. Singh, and C. Fiolhais, *ibid.* **46**, 6671 (1992).