Colossal electroresistance of a Pr_{0.7}Ca_{0.3}MnO₃ thin film at room temperature

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The electronic conduction through a $Pr_{0.7}Ca_{0.3}MnO_3$ thin film is investigated by measurements using dc and pulsed biases. Semiconducting $Pr_{0.7}Ca_{0.3}MnO_3$ films sandwiched by electrodes show both hysteretic and asymmetric behaviors in current-voltage characteristics. The observed conduction characteristics exhibit the space-charge-limited-current effect, and the hysteretic behavior can be ascribed to a carrier trapping and detrapping of the trap sites in the manganite. The hysteresis induces a colossal electroresistance (CER) of more than 5000% at room temperature. The CER ratio is independent of the duration time of pulses from an infinite (dc) down to 150 ns, indicating that the carrier filling of all the traps can be completed within a short time.

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Dramatic control of electronic states enabled by a small external stimulus is expected to break an impasse in developing electronic devices with a fresh concept free from a conventional silicone technology. Correlated electron materials such as doped manganites with a perovskite structure show a variety of electronic phases, which are competing but energetically close to each other,¹ and thus they are considered as a candidate for the devices. Recently, a quite large resistance change by an external electric field-i.e., colossal electroresistance (CER)-was observed at room temperature in Pr_{1-r}Ca_rMnO₃ (PCMO) and triggered a surge of research on its potential for practical applications such as nonvolatile memory elements.²⁻⁴ Such a simple resistive device as is comprised of only PCMO sandwiched by metallic electrodes is quite desirable since its size can be made arbitrarily small.

PCMO exhibits a nonmetallic behavior over the whole doping composition (*x*) range. The ground state of PCMO with x=0.3-0.5 is a charge-ordered antiferromagnetic insulator, which can be switched to a ferromagnetic metal by applying large magnetic or electric fields.^{5–7} Near degeneracy and competition of these phases lead to electronic phase separation^{8,9} and cause the switching-like and relaxor-like phenomena.^{5,6} However, at room temperature, PCMO is not too close to any phase boundary between competing phases and is in an insulating paramagnetic state regardless of x.⁵ Therefore, the origin of CER at room temperature is yet to be elucidated.

In order to clarify the CER phenomena in this compound, we have fabricated polycrystalline film samples, which is similar to the ones reported previously.³ We have performed current-voltage (*I-V*) measurements for devices complying PCMO thin films with $x \approx 0.3$. The *I-V* curves exhibit a large hysteresis and a strong asymmetry, which could be characterized by space-charge-limited current controlled by trapped charge density.

In this study, a PCMO thin film was deposited by an rfmagnetron sputtering technique on a Pt conducting layer (bottom electrode) formed on an insulating MgO singlecrystal substrate. The Pt film on the MgO substrate was deposited at room temperature by an rf-magnetron sputtering in the atmosphere of Ar-gas pressure of 7 Pa, resulting in (111)oriented texture. During the deposition of PCMO, the substrate temperature was 700 °C and the total sputtering gas pressure was 3 Pa with an O₂ partial pressure of 0.6 Pa. The typical thickness of Pt and PCMO film was 380 nm and 150 nm, respectively. The deposited PCMO films were polycrystalline as revealed by x-ray diffraction measurement, as shown in Fig. 1(a). Figure 1(b) shows a cross-sectional image of the transmission electron microscopy of the fabricated layered film. Energy-dispersive x-ray spectroscopy revealed



FIG. 1. X-ray diffraction pattern (a) and cross-sectional image of the transmission electron microscopy (b) of the $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO) film fabricated on the Pt/MgO substrate. The Pt film on the MgO (100) substrate oriented with the (111) direction. (c) shows a schematic view of measurement.



FIG. 2. (a) Typical *I-V* characteristic at 300 K. Arrows indicate sweeping directions. The inset magnifies the behavior around the zero-biased point. (b) The voltage bias dependence of the colossal electroresistance ratio deduced from the characteristic in (a). (c) Temperature dependences of both high- and low-resistance states. The plotted resistances were measured at the biased current 10 μ A: (open circle) high-resistance state, (solid circle) low-resistance state.

the doping level (x) of 0.3 and almost no diffusion of Pt into the PCMO layer. Figure 1(c) shows a schematic view of our devices. An evaporated Ag film with the thickness of 400 nm and circle area of 250 μ m ϕ was used as the top contact pad. A nominal separation between the pads was 1 mm. The positive direction of the bias voltage is defined as the current flows from the top to the bottom electrodes.

Figure 2(a) shows typical *I-V* characteristics at room temperature. The I-V curves exhibit pronounced hysteretic and asymmetric behaviors. The hysteresis is associated with the change from the high- to low-resistance states in the positive-voltage region and the change from the low- to high-resistance states in the negative-voltage region. The *I-V* curves with the hysteresis sequence are obtained repeatedly by sweeping the applied bias. The I-V curves that indicate two resistance states intersect with each other at the origin of the coordinate axes, as shown in the inset of Fig. 2(a). This indicates that the two stable resistance states can realize the nonvolatility. Such an electric-field-induced nonvolatile change of the resistance, termed here electroresistance (ER), is defined as a ratio of $\Delta R/R = (R_{high} - R_{low})/R_{low}$. The ER ratio of our device is over 5000% at maximum as shown in Fig. 2(b) and thus are called colossal electroresistance. The CER effect tends to be suppressed with increasing biased voltage, yet the ratio remains over 100% in most of voltage region showing hysteresis. The temperature dependence of the resistance for both states shown in Fig. 2(c) was semiconducting, being consistent with the result of the bulk



FIG. 3. *I-V* characteristics at 300 K in a double-logarithmic plot: (a) positive-bias and (b) negative-bias regions. Note that the absolute values of current and voltage are taken for the both ordinates. Arrows indicate sweeping directions. The dashed lines correspond to $I \propto V$, while the solid lines to $I \propto V^2$.

crystal.⁵ These results can rule out the Joule heating effect as the origin of the CER effect.

Figures 3(a) and 3(b) show the logarithmic plots of the I-V curve for the positive- and negative-voltage regions, respectively. The arrows indicate the bias sweeping direction. In the low-voltage region of Fig. 3(a), the current shows a behavior with $I \propto V$ (Ohmic), followed by $I \propto V^2$. Then, a sharp current rise is seen at a threshold voltage $V_T \approx 1.0$ V. In the higher-voltage region $(I > V_T)$, $I \propto V^2$ is observed again. Thus, the I-V characteristics of this system are well described by the trap-controlled space-charge-limited-current (SCLC) mechanism¹⁰ across the entire range of current extending five orders of magnitude.¹¹ According to the SCLC mechanism, the threshold voltage V_T corresponds to the transition voltage from the trap-unfilled SCLC to the trap-filled SCLC. In the voltage-decreasing scan, the current is decreased as $I \propto V^2$, but a current drop at V_T does not appear. This indicates that the trap-filled SCLC state can be kept even below V_T , resulting in the clear hysteresis in the positive-bias region.

In the negative-bias region, as shown in Fig. 3(b), similar SCLC behavior is observed. In the low-voltage region, the *I*-*V* curve shows the behavior with $I \propto V$, followed by $I \propto V^2$ as well. In the high-voltage region, the absolute value of the current, however, decreases significantly between -1.6 V and -2.0 V and then increases again. This may indicate that at the threshold voltage $V_T^* \approx -2.0$ V, there occurs transition from the trap-filled SCLC to the trap-unfilled SCLC in the negative-bias region.

From this point of view, the CER effect on this system is caused by the change of the filling ratio with the trap sites in the PCMO layer. The observed difference between the absolute value of the V_T (≈ 1.0 V) and the V_T^* (≈ -2.0 V) suggests the asymmetry of the trap potential with or without trapped carriers. The asymmetry might be caused by the different electronic properties between Ag/PCMO and PCMO/Pt interfaces. It is probable that, at either or both of the interfaces, Schottky-like barriers with the depletion layer are formed. Nevertheless, the nonvolatility of the resistive memory is difficult to explain in terms of the asymmetry of the barrier layers alone.

The trap-filled SCLC state, which first emerges upon sweeping the applied voltage below V_T , should remain filled for a long period of time or until a negative voltage of V_T^* is applied. In order to explain such a persistent trap-filled SCLC, we have to postulate some environmental changes of the trap sites caused by the electronic transitions. The mean time τ spent by a carrier in a trap at temperature T corresponds to the inverse of the escape frequency of a carrier in a trap ν^{-1} . The escape frequency ν can be described by $\nu = \nu_0 \exp\{-(E_t - T\Delta S)/kT\}$, where ν_0 is the attempt-to-escape frequency, ΔS the change of the entropy in the Gibbs energy function, and k Boltzmann's constant, which is required to effect an escape from a trap of depth E_t .^{12,13} The negative value of ΔS increases the residence time of a carrier in the trap and suggests an environmental change of the trap sites which corresponds to the ascent of the symmetry in the material system. For a CER effect in a metal-insulator-metal system, a basic theoretical model has recently been proposed.^{14,15} The proposed model assumes several domains between the electrodes, and the current is given by the hopping of carriers from one domain to another. A large domain in the bulk behaves as a charge reservoir, and the domains at the metal/bulk interface regulate the current as barriers. Provided that the electrons in the domains near the interface are strongly correlated and exhibit the Mott transition as a function of the carrier concentration, the *I-V* curve in the model calculation reproduces essential features of experimental results.¹⁵ The model predicts that the charging of the domains in the bulk is crucial for the nonvolatility of the CER behavior. The persistency of the trap-filled SCLC state is also supported by the model calculation with large electronic change in the material system.

In order to investigate the dynamical response of the carrier trapping, the CER characteristic was measured by applying pulsed biases. Figure 4(a) shows the resistance as a function of time while applying pulses with an amplitude of 15 V and a duration time of 250 ns. By applying a negative pulse to the device in a low-resistance state, the resistance changes to a higher value. The value is kept for any successive negative pulses. When a positive pulse is applied, the value of the resistance suddenly reverts back to the original low value. This nonvolatile and reversible switching behavior can be repeated by applying numbers of pulses. The polarity and ratio of the resistance switch are in good agreement with those expected from the hysteresis of the *I*-V curve of the dc measurement.¹⁶ Figure 4(b) shows the duration time τ_{w} dependence of the CER ratio. A ratio of more than one order of magnitude is observed in the range of $\tau_{\rm w}$ from 120 s



FIG. 4. (a) Resistance as a function of time measured while applying voltage pulses with the amplitude of 15 V and the duration time of 250 ns. (b) CER ratio versus pulse duration time with an amplitude of 15 V. The data of dc measurement are put at the duration time of 2 min ($\approx 10^{11}$ ns).

(dc) down to 150 ns, and the CER can be detected for $\tau_w \ge 50$ ns. The short-pulse limit may be due to extrinsic factors because the limit was comparable with the time constant estimated from the resistance and capacitance of the device. The duration-time-independent CER down to 150 ns ($=\tau_{wth}$) indicates that the filling of all the traps is completed within a very short period τ_{wth} . This behavior is independent of the atmosphere of the measurement such as air, helium, or vacuum below 10^{-4} Pa. Therefore, these facts preclude any possibilities of the chemically or thermally assisted forming process.¹⁷

A similar investigation has been done so far for CER of the Cr-doped perovskite Ti or Zr oxides in details by Bednorz and co-workers.^{18,19} They reported that the CER ratio was dependent on the amplitude or the number of the applied pulses, which may suggest that the CER depends on the amount of the charges in trap sites. However, they also reported that the CER depended on the duration time of the pulse and was unsaturated even for pulses with a very long duration time such as between 1 ms and 1 s.²⁰ The switching time of CER in Cr-doped Ti or Zr oxides seems to reflect a relatively slow charging of the trap sites. This is in contrast to the present result for correlated electron materials such as manganites. Since the strongly correlated electron systems may intrinsically contain spatial inhomogeneity (in the nanoscale or larger) of electronic phases,⁸ only an infinitesimal carrier injection is expected to cause a drastically fast change of carrier distribution which may give rise to such a fast resistance switch. The duration-time-independent CER with very small au_{wth} in our device may underpin the scenario of the instantaneous charging and redistribution of the charged domains as the trap sites.

In summary, we have characterized the hysteretic and asymmetric I-V characteristics in a $Pr_{0.7}Ca_{0.3}MnO_3$ film sandwiched by metal electrodes and proposed that the colossal electroresistance phenomenon may be based on the trapcontrolled space-charge-limited current; namely, the hysteresis originates in the transition between the trap-filled SCLC and the trap-unfilled SCLC. The CER ratio is over 5000% even at room temperature and kept constant from dc to voltage pulses as short as 150 ns, showing a great potential as an emerging nonvolatile memory technology. The nonvolatility and fast response seen in CER may not be explained by the conventional carrier trapping mechanisms. The collective nature in trap-filling and -defilling processes due to strong electron correlation may play a key role.

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