Space-charge and trap-filling effects in organic thin film field-effect transistors

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We use a surface-charge formalism to analyze recent measurements of the electrical properties of organic thin films in a planar field-effect transistor (FET) geometry, including the contribution of both injected charge carriers and charge carriers introduced because of doping. In the presence of trapping centers we find that the electrical conduction in the channel can follow a trap-filling transition with increasing gate voltage. This effect, which produces a significant variation in the effective mobility with gate voltage and induces a strong dependence of the apparent threshold voltage on the temperature, has been observed in measurements on organic FETs but its origin had remained unclear up to now. In addition, we find that space-charge effects can explain several features of recent experiments with organic FETs (OFETs) that cannot be described by the conventional FET model, such as the absence of a saturation behavior for higher source-drain voltages, which we assign to space-charge limited conduction near the drain electrode and which becomes the dominant contribution when the source-drain distance is decreased. The formalism that we used for this analysis can be applied to any FET system based on charge-carrier injection in insulators, and it has an intrinsic flexibility that allows easy extension to take into account additional effects.

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I. INTRODUCTION

Injection of free charge carriers into an insulator from Ohmic metallic contacts results in an inhomogeneous space-charge density which can lead to a space-charge limited (SCL) current proportional to the square of the applied voltage.[1] Although this effect is well-known for one-dimensional conduction between two electrodes,[1,2] it has commonly been neglected in the case of injection-based surface field-effect transistor (IFET) structures using an insulating material between "source" and "drain" metal electrodes. The operation of such a device involves the tuning of the injected charge density with the voltage applied to a "gate" electrode, and it was first described by Wright.[2,3] Later, the problem was treated again, often relying on established knowledge about FETs based on differently doped semiconductors, and several models were proposed to understand the charge transport mechanism in this class of devices.[4–12] However, no coherent analytical treatment describing the physics of charge transport in the insulating thin film of an IFET, which can be easily modified to include the effects of SCL and trap filling, has been published to date. Equations imported by analogy from standard FET models have been used in the past, but they had only limited success in the interpretation of experimental results, and it is not possible to relate the assumptions on which they were based to the reality of the IFET geometry and the materials it uses.

This situation needs to be rectified also because of the great technological and fundamental interest in organic IFETs,[5,13,14] where charge transport takes place in an organic wide-band gap insulator. These devices have attracted great attention recently because of their potential application in low-cost integrated circuits. Moreover, the IFET geometry has also been successfully applied to the fundamental investigation of various insulating organic materials.[5]

It should also be noted that the direct application of formulas originally developed for conventional metal-oxide-semiconductor FETs (MOSFETs) to describe the electrical properties of organic IFETs has generated some confusion in defining important parameters of these devices. One example is the meaning of the threshold voltage in a system where most of the charge carriers are injected from the contacts and not created by the formation of an inversion layer in the channel.[9,10] Another example is an analytical treatment that was proposed to model the current-voltage characteristics of short-channel organic IFETs.[7] The model was derived assuming the existence of a parasitic resistance in series with an ON-channel resistance representing the accumulation layer in the channel.[7] This approach is not entirely satisfactory since the final drain current expression does not tend to the Mott-Gurney law in the limit of high source-drain voltages. Further, the model also considers an additional dependence of the parasitic resistance on the gate voltage which obscures the interpretation of the physical origin behind that resistance.

In this paper we analyze charge transport in the IFET channel using an analytical approach that can take into account the effects of space-charge screening and charge-carrier trapping. The assumptions used to develop the theory and their physical consequences can be readily identified, and the relationship between experimental results and microscopic material parameters is clearly established. This avoids the sometimes nontrivial adaptation of concepts derived from semiconductor device physics to IFETs.

We will show that SCL effects induce a nonsaturation of the current at high source-drain voltages in short-channel devices, an effect that can be minimized by decreasing the channel thickness. This prediction is confirmed by recently

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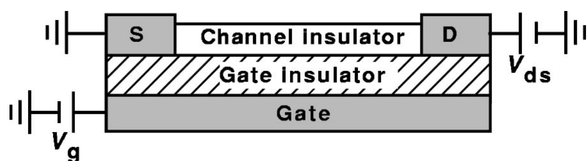

FIG. 1. Schematic structure of the injection-based field-effect transistor (IFET) configuration considered here. S is the source electrode and D is the drain electrode.

published experimental data, where a nonsaturation of the current-voltage characteristics has been observed in short-channel OFETs without a reasonable explanation.[15–17] From this analysis it is clear that SCL conduction can strongly influence operational parameters and design considerations for thin-film IFET geometries based on organic semiconductors and insulators, and also the interpretation of experimental results obtained using such devices.

Finally, we analyze the effects of charge-carrier trapping in the channel. We demonstrate that the effective field-effect mobility becomes dependent on the gate voltage once traps are present in the active layer. Such a gate voltage dependence of the field-effect mobility has been observed in organic IFETs[8,18–20] and sometimes ascribed to an intrinsic charge-transport process typical of disordered materials. However, by simply assuming the presence of a single-energy trap level in the organic insulator, we demonstrate the existence of a trap-filling transition that occurs with increasing gate voltage and that is able to explain quite well the mobility data recently measured in OFETs.

We start by presenting, in Sec. II, the fundamental effects on which the operation of the IFET rests, and the theoretical approach that we will use. This will establish the basic assumptions of the theoretical model and its dependence on material parameters typical of IFETs. Next, in Sec. III, we will analyze the expected behavior of the IFET, highlighting the influence of space-charge effects and trap filling, discuss the on/off ratio, and compare our predictions with experimental data.

II. THEORETICAL MODEL

In this section we analyze, using the surface-charge formalism, the basic transport mechanisms involved in the IFET operation. We show that the IFET problem can be treated by separating the charge density injected in the channel by the gate voltage from the charge density injected in the channel by the source-drain voltage. These quantities are expressed in terms of a surface density in the fundamental equations, and the predominance of one of these charge densities determines different regimes of the device operation.

The schematic IFET structure we are interested in is shown in Fig. 1: a thin film "channel insulator" (the active organic film in OFETs) connects the source and drain contacts, and a high resistivity "gate insulator" separates the channel insulator from the gate electrode. Since we first want to describe the fundamental properties of a model device, we consider charge carriers with a constant, electric-field-independent mobility, and a channel insulator free of any electronic levels that can trap the charge carriers. Additionally, we assume that one type of charge carrier can be injected through Ohmic contacts at the source and drain electrodes, and we neglect the effects of diffusion. These approximations enable the development of a simple, yet powerful model that allows us to quantitatively evaluate the essential features of charge transport in the channel insulator. Without loss of generality, we assume in the following that the injected charge carriers are electrons.

IFETs using p-type organic insulators can suffer a redox doping of the channel with oxygen when in contact with air.[8] Similar electrochemical mechanisms can also dope n-type organic insulators.[8] Hence, we allow for the possibility of (intentional or unintentional) doping of the channel insulator by considering a constant free-carrier density n_0. This corresponds to a charge per unit surface

$$Q_0 = \pm e n_0 D, \tag{1}$$

where e is the unit charge, D is the thickness of the channel insulator, and the lower sign must be used when the free carriers arising from doping are electrons.

We consider an electron density $n_{ds}(x,y)$ that is injected by the source-drain voltage, and an electron density $n_g(x,y)$ that is injected by the source-gate and the drain-gate voltages (x measures the distance in the channel from the source electrode and y measures the distance in the channel from the gate insulator interface). $Q_g(x)$ and $Q_{ds}(x)$ are the corresponding surface charge densities. For a doped channel insulator, the surface IFET operates in the "accumulation" regime when a positive (negative) gate bias is applied to an n-type (p-type) channel. Under these circumstances $Q_g(x)$ and Q_0 have identical sign.[9] Finally, we assume that the channel insulator is only lightly doped so that the space-charge created by uncompensated donors is small compared to n_g and n_{ds}.

The fundamental equations determining the current I_{ds} flowing between drain and source electrodes are the Gauss equation and the transport equation

$$\frac{dE_x}{dx} + \frac{dE_y}{dy} = -\frac{e}{\epsilon\epsilon_0}[n_g(x,y) + n_{ds}(x,y)], \tag{2}$$

$$I_{ds} = W\mu E_x(x)|Q_g(x) + Q_0 + Q_{ds}(x)|, \tag{3}$$

where E is the electric field in the channel insulator, with x and y components E_x and E_y, ϵ_0 is the vacuum permittivity, ϵ is the dielectric constant of the channel insulator, W is the channel width, and μ is the charge-carrier mobility. Note that (3) is valid without any special requirement on the y dependence of the charge density.

The current I_{ds} depends on the total charge at the position x and on the x component of the electric field at the same position, but its final value must not depend on x. Equation (3) therefore provides a generally valid relation between the electric field and the free-electron density found at a given coordinate along the channel.

When the channel length L is much larger than the gate insulator thickness, it is reasonable to assume that the electric charge density associated with the variation of the elec-

tric field in the y direction is much higher than that related to a variation of the electric field in the x direction, or $|dE_y/dy| \gg |dE_x/dx|$. Using this "gradual channel approximation,"[3–5] we can separate the Gauss equation (2) by associating n_g with the dE_y/dy term, and write

$$\frac{dE_x(x)}{dx} = -\frac{Q_{ds}(x)}{\epsilon\epsilon_0 D}, \tag{4}$$

where D is the thickness of the channel insulator.

Equations (3) and (4) are difficult to solve in general. However, it is possible to find specific regions between the source and drain electrodes where simplifying assumptions can be made and an expression for the gate-induced surface-charge $Q_g(x)$ can be found. Equations (3) and (4) can then be combined into a simple characteristic equation for each region. The characteristic equations are then solved separately and the requirement of continuity of the electric field is used to match the solutions in adjacent regions.

In a functioning IFET, there must be a region where the charge induced by the gate dominates over the other components. The gate-induced surface charge in this so-called "accumulation region" is given by the capacity per unit area C_i of the gate insulator[3,9]

$$Q_g(x) = -C_i[V_g - V(x)], \tag{5}$$

where $V(x)$ is the potential in the channel between source and drain electrodes. $V(x)$ starts from zero at the source electrode and reaches V_{ds} at the drain electrode.

Inserting (5) and (4) into (3), we find the characteristic equation for the accumulation region

$$\frac{I_{ds}}{W\mu} = \left[\epsilon\epsilon_0 D\frac{d^2V}{dx^2} + C_i[(V_g + V_0) - V]\right]\frac{dV}{dx}, \tag{6}$$

where V_0 is a doping related voltage defined by $V_0 \equiv -Q_0/C_i$ (V_0 is positive for electron doping). Integration of (6) gives

$$\frac{I_{ds}}{W\mu}x = \frac{\epsilon\epsilon_0 D}{2}\Delta E_x^2(x) + C_i\left[(V_g + V_0)V - \frac{V^2}{2}\right], \tag{7}$$

where $\Delta E_x^2(x) \equiv E_x^2(x) - E_x^2(0)$. If the source-drain voltage V_{ds} remains lower than V_g, the accumulation layer extends all the way from the source to the drain electrode, and $V(L) = V_{ds}$. Equation (7) then becomes

$$I_{ds} = \frac{W\mu}{L}\left\{\frac{\epsilon\epsilon_0 D}{2}\Delta E_x^2(L) + C_i\left[(V_g + V_0)V_{ds} - \frac{V_{ds}^2}{2}\right]\right\}. \tag{8}$$

This equation gives the current-voltage ($I-V$) characteristics for the IFET in the range $V_{ds} \leqslant V_g$ as a function of the difference $\Delta E_x(L)$ of the electric fields at the drain and the source electrode. The latter can be found numerically from (7) and the condition $V_{ds} = \int_0^L E_x(t)dt$, but it turns out that its contribution in (8) is negligible for $V_{ds} < V_g$. The reason is that in this case the potential drop between the source and drain electrodes tends to be evenly distributed along the channel, and $E_x(0) \approx E_x(L) \approx V_{ds}/L$, so that $\Delta E_x(L) = E_x^2(L) - E_x^2(0) \approx 0$.

When V_{ds} is higher than V_g, there is a range of x values where E_y becomes of the order of E_x and the assumptions used to derive (4) and (6) are not fulfilled anymore. However, we can assume that this range of x values is very small compared to the channel length L. We can therefore define a coordinate x_0 where $V(x_0) = V_g$ and consider it to be the end of the accumulation region, and the start of a "depletion" region.

In the depletion region, $V(x) > V_g$ and E_y tends to push the free charge carriers away from the interface between gate insulator and channel insulator. For $Q_0 < 0$, the doping-induced free charge carriers are depleted near this interface and drift out of the film through the Ohmic drain contact. This situation can be modeled by a depletion layer of thickness t in the channel insulator, so that the total charge per unit surface becomes $Q_0 + Q_g = en_0(D - t)$. We find t by solving the Gauss equation in the y direction[8,9]

$$t = \frac{\epsilon\epsilon_0}{C_i}[(1 + a[V - V_g])^{1/2} - 1], \tag{9}$$

where $a = 2C_i/V_0C_s$ and $C_s = \epsilon\epsilon_0/D$. The thickness t reaches its upper limit $t = D$ when the voltage V reaches a "pinch-off" voltage $V_p = V_g + V_0(1 + C_i/2C_s)$ at a coordinate x_p along the channel.

Using (3) and (4), we can write the characteristic equation for the depletion region where $x_0 < x < x_p$

$$\frac{I_{ds}}{W\mu} = \left[\epsilon\epsilon_0 D\frac{d^2V}{dx^2} + C_iV_0 - en_0(D - t)\right]\frac{dV}{dx}. \tag{10}$$

Substitution of (9) and (10) and integration of the resulting expression from x_0 to a point x inside the depletion region yields

$$\frac{I_{ds}}{W\mu}x = \frac{\epsilon\epsilon_0 D}{2}\Delta E_x^2(x) + C_i\left(V_0V_g + \frac{V_g^2}{2}\right) + (C_i + C_s)V_0(V - V_g) + \frac{(C_sV_0)^2}{3C_i}[1 - (1 + a[V - V_g])^{3/2}]. \tag{11}$$

In writing (11) we considered the x component of the electric field continuous at x_0 and given by (7).

For the case when $V_{ds} < V_p$ and $x_p > L$ the depletion region extends up to the drain contact. The source-drain current in the depletion region is then found by substituting $x = L$ and $V(x) = V_{ds}$ into (11)

$$I_{ds} = \frac{W\mu}{L}\left[\frac{\epsilon\epsilon_0 D}{2}\Delta E_x^2(L) + C_i\left(V_0V_g + \frac{V_g^2}{2}\right) + (C_i + C_s)V_0(V_{ds} - V_g) + \frac{(C_sV_0)^2}{3C_i}[1 - (1 + a[V_{ds} - V_g])^{3/2}]\right]. \tag{12}$$

This equation gives the $I-V$ characteristics for the IFET in the range $V_g < V_{ds} < V_p$. As for the expression for the accumulation region derived above, $\Delta E_x^2(L)$ can be found by numerical integration, but can be shown to be negligible for $V_{ds} < V_p$. When V_{ds} approaches V_p the carrier density decreases towards the drain electrodes, and $E_x(L)$ correspondingly increases. Despite this, we will show below that —especially for long channel lengths L —the range of ap-

plication of (11) and (12) can be extended with minor error until $V_{ds}=V_p$, while at the same time neglecting the term containing $\Delta E_x^2(L)$.

We now finally come to the "insulating" region, where $V(x)>V_p$ and $x>x_p$. The IFET regime of operation associated with the growing of an insulating region inside the channel has been traditionally called the "saturation" regime.

The free charge carriers present in the insulating region are only the charges Q_{ds} injected by the source-drain voltage $(Q_g+Q_0=0)$. The characteristic equation for this region is then very simple

$$\frac{I_{ds}}{W\mu}=\left[\epsilon\epsilon_0 D\frac{d^2V}{dx^2}\right]\frac{dV}{dx}. \tag{13}$$

After integrating (13) from x_p to a point x inside the insulating region, applying (11) and the continuity of the electric field at x_p, and using the expressions for C_s and V_p, we find

$$\frac{I_{ds}}{W\mu}x=\frac{\epsilon\epsilon_0 D}{2}\Delta E_x^2(x)+C_i\frac{\beta}{2}, \tag{14}$$

where $\beta=(V_g+V_0)^2+e^2n_0^2D^3/3\epsilon\epsilon_0$. The source-drain current in the saturation regime is then found by substituting $x=L$ into (14)

$$I_{ds}=\frac{W\mu}{L}\left[\frac{\epsilon\epsilon_0 D}{2}\Delta E_x^2(L)+C_i\frac{\beta}{2}\right]. \tag{15}$$

This equation would predict a constant current if the first term between brackets was negligible, as we found for the accumulation region. A constant saturation current is also the solution that is most often found in the literature of organic IFETs.[5,9] But such an assumption is in general not at all justified. Most of the potential applied between the source and drain electrodes drops in the small insulating region near the drain electrode where the charge-carrier density becomes very small. The magnitude of the electric field $E_x(L)$ can then be much larger than $E_x(0)$, and $\Delta E_x^2(L)\approx E_x^2(L)$ becomes very relevant in (15). An approximate analytical solution for the current can be obtained by finding an approximate relation between the coordinate x_p and the source-drain voltage. The small density of free charge carriers in the insulating region implies $E_x(x)\gg E_x(x_p)$ for $x>x_p$, except near the vicinities of $x=x_p$. It is then a good approximation to assume that the electric field inside the insulating region is given by the space-charge field found between two Ohmic electrodes separated by the distance $L-x_p$; we can then write[1,3]

$$E_x(L)\sim\frac{3}{2}\frac{V_{ds}-V_p}{L-x_p}. \tag{16}$$

The current flowing between the source and drain contacts is the same at every coordinate x of the channel. Using (14) at $x=x_p$ and $x=L$, we find

$$\frac{1}{x_p}-\frac{1}{L}=\frac{\epsilon\epsilon_0 D}{C_i\beta}\left(\frac{\Delta E_x^2(L)}{L}-\frac{\Delta E_x^2(x_p)}{x_p}\right). \tag{17}$$

We already argued above that $E_x(L)\gg E_x(x_p)\approx E_x(0)$. Equation (17) then gives $E_x^2(L)=(C_i\beta/\epsilon\epsilon_0 D)(L-x_p)/x_p$. The comparison of this relation with (16) yields

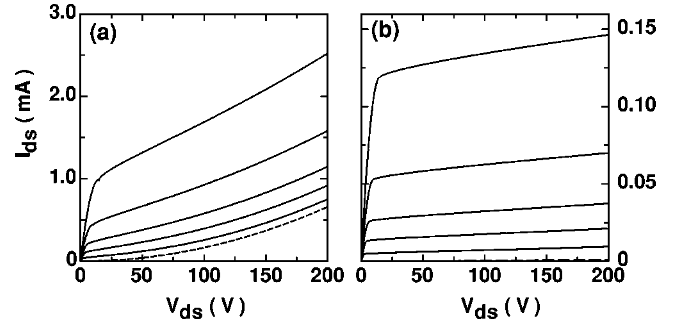

FIG. 2. Current-voltage $(I-V)$ characteristics of two surface IFET. The simulation parameters are $C_i=1.76\times10^{-4}$ Fm^{-2}, $\mu=10^{-4}$ m^{2}V^{-1}s^{-1}, $n_0=10^{20}$ m^{-3}, $W=1.5$ nm, $D=100$ nm, $\epsilon=3$, $L=3$ μm (a), and $L=25$ μm (b). The curves were plotted with increasing gate voltage of 0 V [dashed curve, not visible in (b)], 3, 5, 7, 10, and 15 V (continuous curves).

$$\frac{(V_{ds}-V_p)^2}{\beta}=\frac{4C_i}{9\epsilon\epsilon_0 D}\frac{(L-x_p)^3}{x_p}, \tag{18}$$

which gives x_p as a function of V_{ds}. Inserting $E_x(L)$ from (16) into (15), one then obtains the source-drain current in the saturation regime. In the limit when $L\gg D$, the space-charge effects can be neglected for values of V_{ds} not much higher than V_p, and Eq. (15) gives the conventional formula $I_{\text{sat}}=W\mu C_i(V_g+V_0)^2/(2L)$ for the saturation current. We now have a complete solution for the source-drain current at all gate voltages and all source-drain voltages.

III. RESULTS AND DISCUSSION

A. The current-voltage characteristics

Figure 2 shows the $I-V$ characteristics predicted from (8), (12), (15), (16), and (18) for various gate voltages. The curves were calculated taking parameters that are representative of IFETs using high-quality organic semiconductors. One sees that the current keeps increasing with V_{ds} in the range $V_{ds}>V_p$. The nonsaturation of the current is more pronounced at low gate voltages and is due to the participation of the injected charge Q_{ds} in the electrical conduction of the insulating layer. The potential drop between the points $x=x_p$ and $x=L$ is then high but finite. In the limit of large V_{ds} or small V_g, the carriers injected by the source-drain voltage dominate the conduction and the source-drain current increases quadratically with the applied voltage, a typical signature of a space-charge limited current. At $V_g=0$, and for a low doping level of the channel insulator, I_{ds} is given by the Mott-Gurney law, or $I_{scl}=(9/8)WD\epsilon\epsilon_0\mu V_{ds}^2/L^3$.

Figure 2 also compares the $I-V$ curves for a short-channel device [Fig. 2(a)] with the curves for a long-channel device [Fig. 2(b)]. The long-channel IFET shows a better saturation of the source-drain current in the "saturation" regime; the increase of L decreases the injection of the space-charge Q_{ds}, lowering the electrical conductivity of the insulating layer. Therefore, with decreasing L or increasing D [see Eq. (15)], the contribution of SCL effects on the device operation increases, enhancing the nonlinearities of the satu-

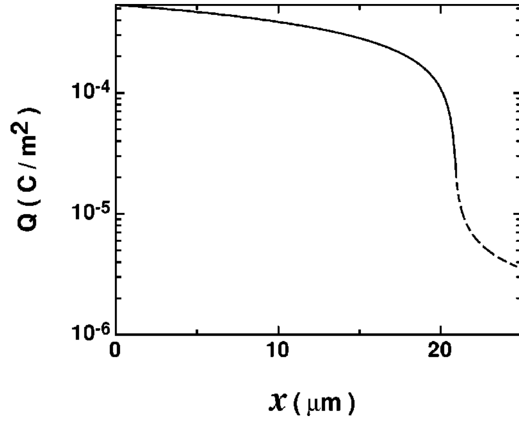

FIG. 3. Spatial distribution of surface space-charge along the IFET channel. The device parameters are the same of Fig. 2(b) with $V_{ds}=33.3$ V and $V_g=3$ V, but considering $V_0=0$ V. The continuous line represents the surface charge in the "accumulation" region and the dashed line represents the surface charge in the "insulating" region.

ration current at small gate voltages. This result can account for the nonsaturation of the current at high source-drain voltages that has been observed in organic IFETs with channel lengths of the order of 4 μm[15,16] and hundreds of nanometers.[17] In accordance with the theory developed in Sec. II, the measurements performed in Ref. 17 show that the nonsaturation of the source-drain current increases with decreasing channel length.

The spatial distribution of surface charge inside the IFET in the saturation regime, for a channel insulator free of doping, is shown in Fig. 3. In this simulation $V_{ds}=33.3$ V, $V_g=3$ V, and $L=25$ μm. The curve was calculated performing a numerical integration of (7) and applying (15). One can see that the length of the "insulating" region is small compared to the length of the "accumulation" region, even when $V_{ds} \gg V_g$. The transition between the two regions is sharp and the charge contained in the accumulation region is high compared with the charge in the insulating region. The numerical result confirms that the approximations used to derive the analytical $I-V$ characteristics are reasonably precise; for example, the value of the coordinate x_p in Fig. 3 is 20.93 μm, whereas the value of x_p calculated applying (18) is 20.84 μm.

Finally, it is important to note from (18) that the doping of the channel insulator, by increasing the "pinch-off" voltage, decreases the length of the insulator layer for a given value of $V_{ds} > V_p$. However, the doping does not change the slope of the drain current once the saturation regime is reached.

A nonsaturation of the drain current has also been observed in a MOSFET (see Fig. 41, Ref. 4, p. 478), where two p-n junctions separate the source and drain electrodes from the channel. However, there the physical mechanism is different.[4] It cannot be used for the IFET where, as an example, the nonsaturation of the drain current mainly depends on the thickness of the channel insulator relative to its length: short-channel IFETs can have a good saturation of the drain current if the insulator channel is sufficiently thin. In conventional MOSFETs the influence of the space-charge Q_{ds} is lower since a p-n junction is a poor injecting contact compared to an Omic metal/insulator interface. In these devices short-channel effects depend on the relative dimension of the depletion-layer widths of the source and drain junctions relative to the channel length. These effects are severe when the device operates in punch-through conditions which cannot be avoided by simply decreasing the channel semiconductor thickness.[4]

B. The on/off ratio

Space-charge effects impose geometrical limits on the performance of an IFET. This becomes clear when we calculate approximate relations for an important device parameter, the on/off ratio. We define the on/off ratio at a given V_{ds} as the ratio between the current in the transistor when $V_g=V_{ds}$ ("on" state) and the current when $V_g=0$ ("off" state).[8] Due to the contribution of the space-charge limited current for the off state, different dependencies of the on/off ratio on the source-drain voltage can be obtained. For example, if $V_{ds} \gg V_p$, the SCL current is negligible and the on/off ratio is

$$\frac{I_{\rm on}}{I_{\rm off}} \approx \frac{V_{ds}^2 + 2V_0V_{ds}}{V_0^2 + (q^2n_0^2D^3/3\epsilon\epsilon_0)} = \left(\frac{C_i^2}{q^2n_0^2D^2}V_{ds}^2 + \frac{2C_i}{qn_0D}V_{ds}\right)\left(1 + \frac{C_i^2D}{3\epsilon\epsilon_0}\right)^{-1}, \qquad (19)$$

where we have used Eq. (8) to calculate the on current and Eq. (15) to calculate the off current. A similar relation to Eq. (19) was derived in Ref. 8 for the on/off ratio of a lightly doped organic FET. At high source-drain voltages so that $V_{ds} \gg V_p$, space-charge effects cannot be neglected and Eq. (19) is not valid any more. In this limit the off current can be approximated by the Mott-Gurney law and the on current by Eq. (15). The on/off ratio is

$$\frac{I_{\rm on}}{I_{\rm off}} \approx \frac{W\mu C_i(V_{ds}^2/2L)}{(9/8)WD\epsilon\epsilon_0\mu(V_{ds}^2/L^3)} = \frac{4C_i}{9D\epsilon\epsilon_0}L^2. \qquad (20)$$

Equation (20) depends only on the geometrical properties of the device and represents the upper theoretical limit for the on/off ratio of an ideal "ultrapure" IFET.

Due to the lower off current, the on/off ratio calculated from Eq. (20) is always higher than the ratio predicted from Eq. (19). Both equations predict an increase of the device switching properties with decreasing thickness of the insulator channel, but Eq. (19) does not predict a dependence of the on/off ratio on the channel length. This dependence is explicit in Eq. (20), where one can see that the device switching performance decreases rapidly with decreasing channel length. This can put important limits on the level of miniaturization that can be achieved with organic-based FETs.

C. The effect of charge-carrier trapping

The model developed in Sec. II uses a formalism based on surface charges for modeling the electronic properties of thin film IFETs. This formalism is very flexible and can be extended to treat more complex physical situations. We illus-

trate this flexibility by analyzing the effect of charge-carrier trapping in the channel insulator during the accumulation regime.

We consider a device that is free of doping impurities but that contains a density N_t of centers that can trap the injected charge carriers. We assume $L \gg D$, so that the charge injected by the source-drain voltage can be neglected compared to the charge injected by the gate voltage. This injected charge is then distributed between the free and the trapped carriers. Applying the detailed balance principle, the density of free carriers n depends on the density of occupied traps, n_{oc} as $\partial n/\partial t = \beta n_{\text{oc}} - \gamma n(N_t - n_{\text{oc}})$, where β and γ are parameters related to the emission and capture rates of the traps, respectively. In steady state this gives an equation in terms of surface charges

$$Q_{\text{free}} = \alpha \frac{Q_g - Q_{\text{free}}}{Q_t - (Q_g - Q_{\text{free}})}, \tag{21}$$

where $\alpha = \beta/\gamma$ is a parameter that depends on the absolute temperature, and $Q_t = -qN_tD$. If we can assume that $Q_t \gg Q_g$ and that the emission rate of the traps is small, then most of the charge carriers induced by the gate voltage are trapped and Eq. (21) can be approximated by a first-order expansion on Q_g/Q_t

$$Q_{\text{free}} \approx \alpha \frac{Q_g}{Q_t}\left(1 + \frac{Q_g}{Q_t}\right). \tag{22}$$

Modifying Eq. (3) and using Eqs. (5) and (22), we can write the characteristic equation for the accumulation regime

$$\frac{I_{ds}}{W\mu} = Q_{\text{free}}E_x = \frac{\alpha}{Q_t}\left[C_i(V_g - V) + \frac{C_i^2(V_g - V)^2}{Q_t}\right]\frac{dV}{dx}. \tag{23}$$

Integration of Eq. (23) from the source to the drain electrodes using $V(0)=0$ and $V(L)=V_{ds}$ results in

$$I_{ds} = \frac{W}{L}\mu\frac{\alpha}{Q_t}C_iV_{ds}\left[V_g - \frac{V_{ds}}{2} + \frac{C_i}{Q_t}\left(V_g^2 - V_gV_{ds} + \frac{V_{ds}^3}{3}\right)\right]. \tag{24}$$

The saturation current is given by taking $V_{ds}=V_g$ in Eq. (24), or

$$I_{\text{sat}} = \frac{W}{2L}C_iV_g^2\mu\frac{\alpha}{Q_t}\left(1 + \frac{2C_i}{3Q_t}V_g\right). \tag{25}$$

Equation (25) shows that the effective field-effect mobility measured by the saturation current method depends on the gate voltage once charge-carrier traps are present in the channel. It should be noted that this effect was derived without any further assumption about the nature of the traps or the physical mechanism behind the charge-carrier transport. The dependence of the field-effect mobility on V_g has been observed in organic IFETs[8,18–20] and sometimes ascribed to an intrinsic charge-transport mechanism present in this kind of material. However, from the discussion above, it is clear that measurements of the intrinsic transport properties of the channel insulator using IFETs should be accepted with care since carrier trapping can mask some features of the intrinsic mobility.

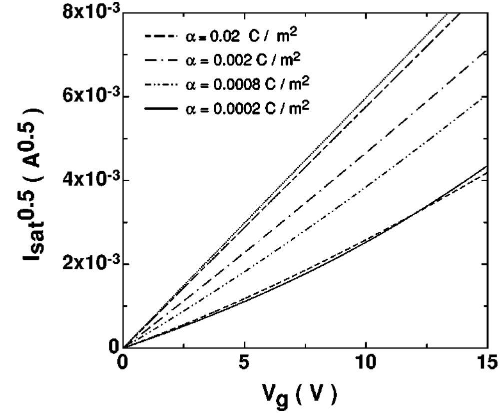

FIG. 4. Square root of the saturation current as a function of the gate voltage. The device parameters are the same of the Fig. 2(b). Q_t was assumed to be 0.0016 C/m^2, which corresponds to a total density of traps $N_t = 10^{23}$ m^{-3}. The curves were calculated from the numerical integration of Eq. (23) using the exact solution of Eq. (21). The dotted curve was calculated from the conventional model, $I_{\text{sat}} = W_\mu C_i V_g^2/(2L)$, and the dashed curve was derived from Eq. (25).

In Fig. 4 we plot the square root of the saturation current as a function of the gate voltage calculated from the numerical integration of the left-hand side of Eq. (23) and using the exact expression for Q_{free} obtained from the solution of Eq. (21). The curves were calculated for various values of the parameter α and for a fixed value of Q_t. The following features can be distinguished.

(i) When $Q_t/\alpha \gg 1$, which simulates measurements at low temperatures or the presence of deep traps in the channel, most of the charges induced by the gate voltage are trapped and Eq. (25) is valid. In this regime the curve $I_{\text{sat}}^{0.5}$ as a function of the gate voltage is nonlinear for a wide range of values of V_g.

(ii) When $Q_t/\alpha \approx 1$, the $I_{\text{sat}}^{0.5}$ curve resembles a straight line in the limit of high gate voltages. At small gate voltages the saturation current is higher than the current obtained extrapolating this straight line to $V_g \to 0$. Further, it is evident in Fig. 3 that the point in which the straight line crosses the V_g axis changes with α. Therefore, the direct application of the conventional FET model to explain these curves would result in a threshold voltage that strongly depends on the temperature, decreasing with increasing T. The above features were observed in recent measurements performed using organic IFETs,[10,19,21–23] but the explanation was controversial until now. Some of these features were ascribed to the hopping transport mechanism of the charge carriers in the disordered organic insulator.[10] However, from the discussion above, it is clear that such features can be produced by charge-carrier trapping, independently of the mechanism behind the charge transport. In principle, comparing measurement performed at different temperatures, it should be possible to determine the variation of α with T. Once this function is known, one can separate the intrinsic transport properties of the material from the ones affected by the car-

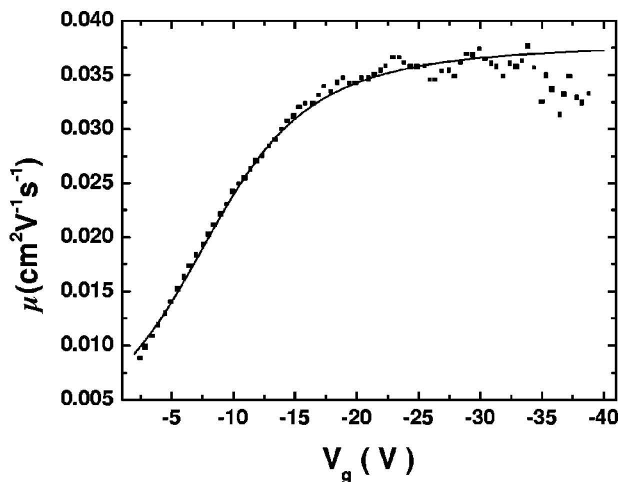

FIG. 5. Variation of the mobility μ with the gate voltage in accumulation regime obtained from the channel's transconductance method. The continuous line is calculated taking $Q_t = 0.000\,45\ \mathrm{C/m^2}$ and $\alpha = 0.000\,12\ \mathrm{C/m^2}$. The experimental data (squares) were taken from Fig. 6 of Ref. 9. The device parameters are $L = 50\ \mu$m, $W = 5$ mm, and $C_i = 5\ \mathrm{nF/cm^2}$.

rier trapping, which can reveal the real physical processes responsible for this transport.

(iii) Finally, when $Q_t/\alpha \ll 1$, which simulates measurements performed at high temperatures or the presence of shallow traps in the channel, the saturation current tends to have the value predicted by the conventional FET model.

The field-effect mobility in the accumulation regime can be estimated measuring the channel transconductance. The transconductance is the partial derivative of the drain current with the gate voltage at constant V_{ds}. For a conventional MOSFET, the relation between the mobility and the channel's transconductance is given by[4]

$$\mu = \frac{L}{WC_i V_{ds}} \left(\frac{\partial I_{ds}}{\partial V_g} \right)_{V_{ds}=\mathrm{const}}. \tag{26}$$

In Fig. 5 we plot the variation of the field-effect mobility as a function of the gate voltage obtained from the transconductance method (continuous line). The curve was calculated from numerical integration of Eq. (23) and using the exact expression for Q_{free} obtained from the solution of Eq. (21). One sees that the field-effect mobility increases strongly with increasing V_g due to trap filling. At high gate voltages, however, the majority of the traps in the channel is filled by the injected charge and μ saturates (trap-filled conduction). In the trap-filled range μ is given by the intrinsic mobility of the carriers in the channel insulator. The behavior shown in Fig. 5 is the analog for the IFET geometry of the trap-filling transition observed in the $I-V$ characteristics of an insulator sandwiched between two Ohmic contacts and with a single energy trap level in the gap.[1]

Figure 5 also compares the theoretical curve with experimental data presented in Fig. 6 of Ref. 9. The data were measured in a typical OFET using dihexylsexithiophene (DH6T) as active layer. The theoretical curve was calculated using Q_t and α as fitting parameters. One sees that the experimental mobility follows quite well the dependence on V_g predicted by Eqs. (21) and (23). The value of the intrinsic mobility assumed in the simulation, $\mu = 0.038\ \mathrm{cm^2V^{-1}s^{-1}}$, is slightly higher than the mobility estimated from the "apparent" saturation of the experimental curve at high gate voltages, $\mu \approx 0.036\ \mathrm{cm^2V^{-1}s^{-1}}$. This small discrepancy is attributed to the fact that the experimental data do not really saturate but start to decrease at high gate voltages. This decrease after -30 V is due to Ohmic losses at the source and drain electrodes.[9]

Since the values of Q_t and α obtained from the fitting in Fig. 5 are of the same order, the plot of $I_{\mathrm{sat}}^{0.5}$ versus V_g for the DH6T device should follow a curve of type (ii) described above. The experimental curve is presented in Fig. 5 of Ref. 9, where its clear that the data tend to bend upward at low gate voltages, reproducing exactly the features shown in Fig. 4.

IV. CONCLUSIONS

In conclusion, we developed a treatment of charge transport in the insulating film of an IFET that allows one to take into account space-charge effects and charge-carrier trapping. We showed that the influence of space-charge effects on the current-voltage curves can be very large. Experimental data where a nonsaturation of the current at higher source-drain voltages were observed should be reinterpreted in light of these theoretical insights, and the development of miniaturized organic field-effect transistors should take into account the intrinsic limitations we discussed. Moreover, we showed that the additional assumption of a single-energy trap level in the organic insulator can explain recent results observed in organic IFETs, including the unusual dependence of the saturation current on V_g and the variation of the effective field-effect mobility with the gate voltage.

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