# Unexpected scaling of the performance of carbon nanotube Schottky-barrier transistors

S. Heinze, M. Radosavljević, J. Tersoff,* and Ph. Avouris‡
*IBM Research Division, T. J. Watson Research Center, Yorktown Heights, New York 10598, USA*
(Received 24 January 2003; revised manuscript received 12 September 2003; published 30 December 2003)

We show that carbon nanotube Schottky-barrier transistors exhibit scaling that is qualitatively different than conventional transistors. The performance depends in an unexpected way on both the thickness and the dielectric constant of the gate oxide. Experimental measurements and theoretical calculations for ambipolar devices provide a consistent understanding of the novel scaling, which reflects the very different device physics of a Schottky-barrier transistor with a quasi-one-dimensional channel contacting a sharp edge. A simple analytic model gives explicit scaling expressions for key device parameters such as subthreshold slope, turn-on voltage, and transconductance.

DOI: 10.1103/PhysRevB.68.235418 PACS number(s): 73.40.Cg, 73.63.Fg

Recent decades have witnessed remarkable and continuing improvements in the performance of field-effect transistors (FET's). These improvements result largely from aggressive scaling of devices to smaller sizes. As further improvement of conventional FET's becomes increasingly difficult, attention has focused on new devices such as carbon nanotube (CN) FET's. CNFET's have already shown very promising performance, despite the use of relatively thick gate oxides.[1–3]

Here we examine the performance improvement of CNFET's upon scaling of the thickness and dielectric constant of the gate oxide. In both experimental measurements and theoretical calculations, we find a very different scaling behavior than for conventional transistors, with important consequences for the design of CNFET's. Specifically, key measures of device performance scale approximately as the *square root* of the gate-oxide thickness $t_{ox}$ or its inverse. These include the turn-on voltage, the transconductance, and the subthreshold slope.

We show that this surprising behavior can be captured in a simple analytic model, which gives a universal form for the saturation current versus gate voltage. Our model incorporates the recent recognition[1,2,4–6] that, in ambipolar CNFET's such as ours, transistor action is caused by modulation of the Schottky barriers (SB's) at the metal-nanotube contacts. The model also highlights the central role of the contact geometry in determining the scaling, with different geometries giving different power laws for the scaling. In contrast, the scaling of conventional FET's with $t_{ox}$ is independent of contact geometry in the long-channel limit. (The same should presumably be true of CNFET's having ohmic rather than Schottky-barrier contacts[7].)

In conventional transistors, there is great interest in oxides with high dielectric constants, because these increase the gate capacitance and thus the performance. Improved performance has also been obtained for CNFET's by using oxides of high dielectric constant.[2,8] However, for ballistic SB-CNFET's, the performance in the turn-on regime is not linked to the capacitance. We show that in this case, the improvement instead comes from changes in the electric field patterns due to the *inhomogeneous* dielectric used. For such geometries, the degree of improvement is tightly coupled to the gate-oxide thickness, with the most dramatic improvement occurring for thicker gate oxides.

Our CNFET's use a standard back-gated geometry,[9] taking advantage of the precise thickness control and high quality of thermally grown $SiO_2$. Very thin gate oxides (2 and 5 nm) are grown in small, pre-patterned areas on a degenerately doped silicon wafer, which serves as the gate. Carbon nanotubes with diameter of about 1.4 nm (Ref. 10) are dispersed on the wafer. Source and drain electrodes, formed using electron-beam lithography and lift-off, contact those CN's lying on ultrathin oxide. In order to suppress the leakage current, the rest of the source and drain contacts are separated from the back gate by a thicker ($\sim$120 nm) field oxide. Details of the fabrication have been presented elsewhere.[11]

Typical transport characteristics of bottom gate devices with thin oxides are shown in Fig. 1. A quantitative comparison can be made by measuring the subthreshold slope[12] $S \equiv (d \log_{10} I/dV_g)^{-1}$ where $V_g$ is the gate voltage. The extracted values are given in Fig. 1. We see a steady improvement of the turn-on for thinner oxides. However, even the thinnest oxides give $S$ significantly higher than the thermal limit of about $kT \ln 10 \sim 60$ mV/dec at room temperature, and a key goal here is to understand the factors that can give further performance improvement.

(Lower $S$ values have been reported in CNFET's using highly doped, effectively ohmic contacts[8] or exotic designs,[13] or ohmically contacted smaller bandgap nanotubes.[7] However, these have their own advantages and disadvantages; and here we consider only straightforward scaling of existing designs and large bandgaps that lend themselves to integration with Si-based devices.)

To understand the scaling properties of carbon nanotube (NT) transistors, we assume ballistic transport (as expected for such short tubes, and in accordance with experiment[14]), and calculate the current using the Landauer-Büttiker formula

$$I = \frac{4e}{h} \int [F(E) - F(E + eV_d)] T(E) dE. \qquad (1)$$

Here $V_d$ is the drain voltage and $F$ is the Fermi function. The energy-dependent transmission $T(E)$ through the SB is

 

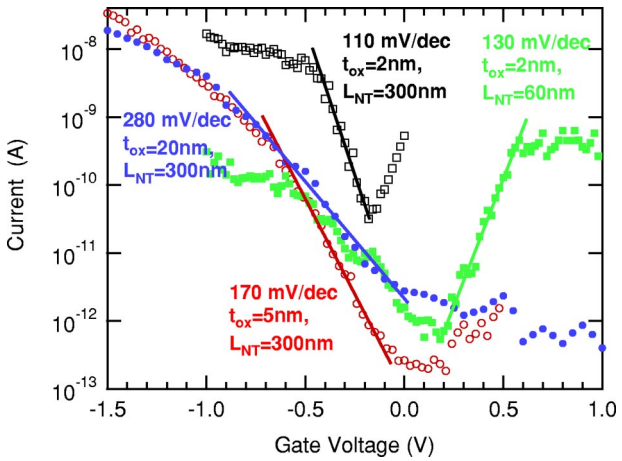


FIG. 1. (Color online) Representative transfer characteristics of CNFET's at different oxide thicknesses $t_{ox}$. The turn-on is characterized by the subthreshold slope $S$ (straight lines). The slope becomes steeper for thinner oxides: from 280 mV/decade for $t_{ox}=20$ nm and $V_d=-0.5$ V, to 170 mV/decade for $t_{ox}=5$ nm and $V_d=-0.5$ V, and 110 mV/decade for $t_{ox}=2$ nm and $V_d=-0.2$ V. Comparable scaling is seen in $n$-type devices as well, e.g., 130 mV/decade for $t_{ox}=2$ nm and $V_d=0.2$ V. [The observed value of $S$ is insensitive to $V_d$, in agreement with previous studies (Ref. 2).]

evaluated within the WKB approximation,[15] using the idealized band structure.[16] This gives

$$\ln T = -\frac{4}{3bV_\pi}\int_{z_i}^{z_f}(\Delta^2-[E+eV(z)]^2)^{1/2}dz, \qquad (2)$$

where $b=0.144$ nm is the bond length, $\Delta$ is half the NT band gap, $V_\pi=2.5$ eV is the tight-binding parameter, and $V(z)$ is the electrostatic potential along the NT. The integration is performed between the classical turning points $z_i$ and $z_f$. [For example, for electrons in the conduction band, $z_f$ is determined from $\Delta-eV(z_f)=E$, $z_i=0$, or, if $E<-\Delta$, is determined from $-\Delta-eV(z_i)=E$.] For simplicity, we present numerical calculations only for the case of ideally ambipolar nanotubes, i.e., having midgap Schottky barriers, though we have examined other cases. In this case, the current is symmetric with respect to the applied gate voltage; and without loss of generality, we limit the discussion to positive gate voltages, i.e., electron tunneling into the conduction band.

To obtain the electrostatic potential along the NT, we numerically solve the electrostatic boundary problem given by our device geometry, which is sketched in the upper inset of Fig. 2. We consider a device similar to the experiment, with a bottom gate at $t_{ox}$ from the NT, source and drain contacts that are 20 nm thick, and a top electrode which is far from the NT relative to $t_{ox}$. (The use of a top electrode in this geometry is for computational convenience; and whether it is grounded or kept at $V_g$ has negligible impact on the results.) We further neglect charge on the NT as in Ref. 5. This remains a good approximation throughout the regime studied here.[17] All numerical calculations here use a NT of 1.4 nm diameter and a band gap of 0.6 eV.

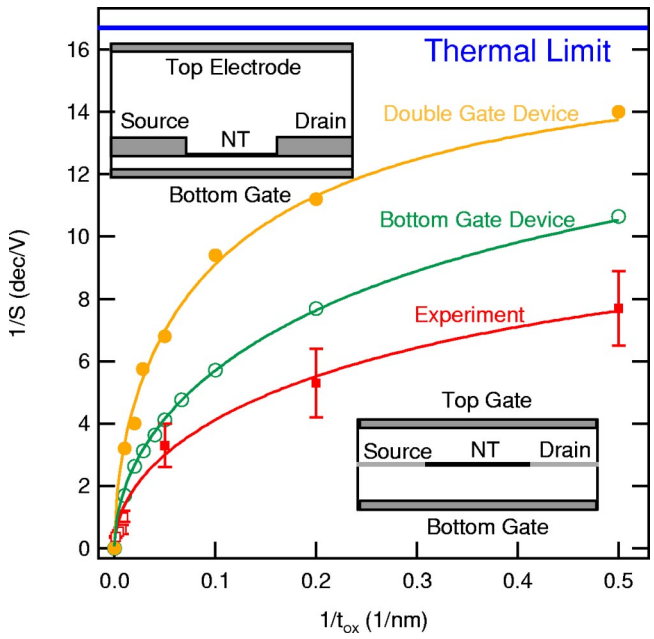


FIG. 2. (Color online) Inverse subthreshold slope $S$ as a function of the inverse oxide thickness $t_{ox}$. Solid curves are fitted as described in text. The bottom red curve is experiment, open red squares are data from previous work, and filled red squares are this work. Data at $t_{ox}=2$ and 5 nm represent averages over several devices. For $t_{ox}=20$ nm our result agrees with previous reports (Ref. 3). Upper two curves are calculated for $V_d=V_g$.[19] The upper left inset shows the bottom gate device geometry (open green circles) while the lower right inset shows the double gate device (filled orange circles).

Our geometry corresponds to the long-channel limit, and we do not consider drain voltages $\gg V_g$, which lead to injection of (minority) carriers from the drain electrode. These interesting issues are discussed elsewhere.[11,18]

Figure 2 shows $S^{-1}$, the inverse of the subthreshold slope, versus the inverse oxide thickness $t_{ox}^{-1}$. For the experimental curve, only ambipolar devices with symmetric (or nearly symmetric) $p$ and $n$ conduction were used, averaging five to seven devices for each point. The $S^{-1}$ values—even for very thin oxides—lie well below the thermal limit. The theoretical curves are evaluated for $V_d=V_g$, corresponding to current saturation.[19] The calculated curve for the bottom gate geometry is in good qualitative agreement with experiment; the difference presumably arises from the specific contact geometry, which is not known precisely on the nm scale in the experiment.[20]

To illustrate the importance of the contact geometry, we also consider an idealized double gate device (lower inset of Fig. 2). Its source and drain contacts are as thin as the NT diameter (1.4 nm), and both top and bottom gate oxides have thickness $t_{ox}$. The general trend with $t_{ox}$ is unchanged, but for any given $t_{ox}$ the subthreshold slope is greatly improved relative to the bottom gate device with thicker contact.

To better understand the scaling of the subthreshold slope with oxide thickness, we consider a simple model. For the double gate device (lower inset of Fig. 2) with vanishing contact thickness, the electrostatic problem can be solved

analytically[21] in the long-channel limit. The potential in the vicinity of the contact varies as $V(z)=2V_g\pi^{-1/2}(z/t_{ox})^{1/2}$, where $V_g$ is the gate voltage and $z$ is the distance from the contact along the NT. Inserting this $V(z)$ into Eq. (2), we calculate the current at saturation [$V_d=V_g$ (Ref. 19)]. In the limit of a thick gate oxide, the position of the conduction band at the drain, $\Delta-eV_d$, can be replaced by $-\infty$. (This is due to the negligible transmission caused by the increasing thickness of the tunneling barrier at energies far below the Fermi energy.) Then

$$I_{sat}=\frac{4e\Delta}{h}H\left(\frac{V_g}{V_{scale}^{dg}},\frac{\Delta}{kT}\right), \tag{3}$$

where $H(x,y)$ is

$$H(x,y)=\int_{-\infty}^{\infty}\frac{\exp[-h(s)/x^2]}{1+\exp(sy)}ds \tag{4}$$

and $h(s)$ is

$$h(s)=\int_{\max(0,-1-s)}^{1-s}t[1-(s+t)^2]^{1/2}dt. \tag{5}$$

The "scaling voltage" for this double-gate device is

$$V_{scale}^{dg}=\left(\frac{2\pi\Delta^3}{3be^2V_\pi}\right)^{1/2}t_{ox}^{1/2}. \tag{6}$$

Within this idealized geometry, changing the oxide thickness is equivalent to simply rescaling the gate voltage by $V_{scale}^{dg}$. The turn-on voltage is proportional to $V_{scale}^{dg}$, and thus scales as $t_{ox}^{1/2}$. We can evaluate $S$ for $V_d$ at saturation[19], where $S=(d\log_{10}I_{sat}/dV_g)^{-1}$. Then $S$, similar to $I_{sat}$, is a function of $V_g/V_{scale}^{dg}$. Thus $S$ scales as $t_{ox}^{1/2}$. Similarly, we find that the transconductance, $dI_{sat}/dV_g$, scales as $t_{ox}^{-1/2}$.

For very thin gate oxides, some of these approximations break down—in particular, the simple form of $V(z)$ near the contact, and the infinite limits of integration in Eq. (4). But in any case, $S$ must eventually saturate at the thermal limit of $kT\ln 10\sim 60$ mV/dec. This suggests the interpolation formula $S=[\alpha t_{ox}+(kT\ln 10)^2]^{1/2}$, with $\alpha$ a fitting parameter. Figure 2 shows that this fitting works well for the experiment and the calculation for both device geometries. For thick oxides, $S$ scales as $t_{ox}^{1/2}$, while for very thin oxides it gradually approaches the thermal limit.

For a more complete description of the device behavior, we examine the saturation current vs gate voltage. Figure 3(a) shows the results of the full numerical calculation for the bottom-gate geometry. These are well described by the analytic model (3), over a large range of $t_{ox}$, if we replace the analytic $V_{scale}^{dg}$ with $V_{scale}^{bg}=2.2V_{scale}^{dg}$, where the single empirical factor of 2.2 is sufficient to account for the difference in geometry. Figure 3(b) shows that all curves are nearly identical to the analytic form (3), with the same $t_{ox}^{1/2}$ scaling as in the idealized model (aside from the one empirical factor of 2.2). As discussed above, the analytic model becomes inaccurate for very thin oxides, and this is observed in Fig. 3(b) for $t_{ox}=2$ nm.

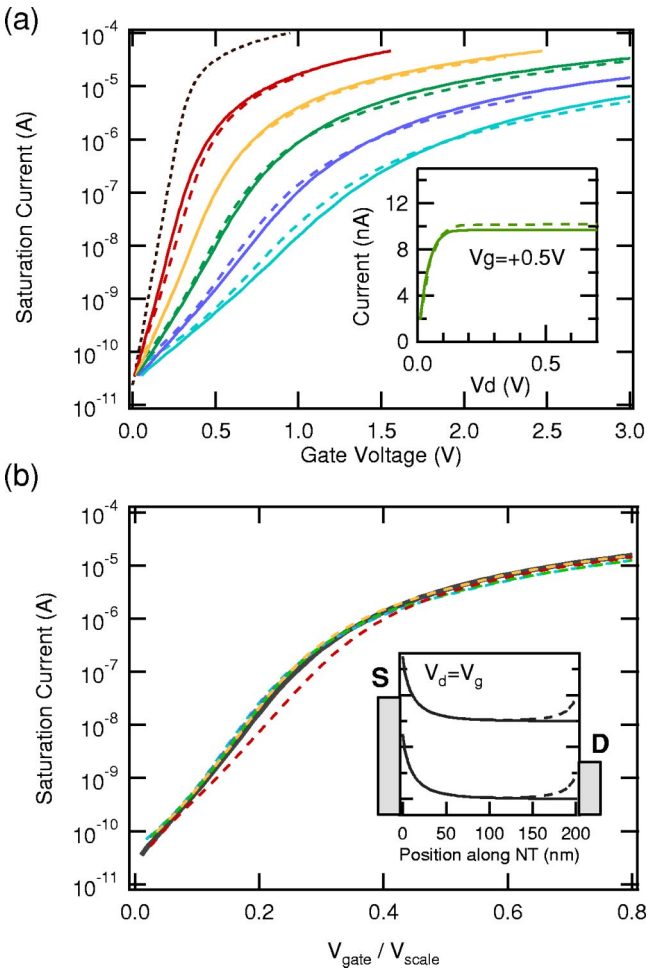


FIG. 3. (Color online) Calculated saturation current versus gate voltage. (a) Results for bottom-gate devices with $t_{ox}=35$, 20, 10, 5, and 2 nm, from right to left, and the thermal limit (dotted line). Solid lines are calculated with Eq. (3) and $V_{scale}^{bg}=2.2V_{scale}^{dg}$ while dashed lines show the full calculation. The inset shows the current saturation with drain voltage for $t_{ox}=10$ nm. (b) Saturation current [same as in (a)] versus $V_g/V_{scale}^{bg}$. All solid lines become one black line, Eq. (3). The inset shows band diagrams at $V_d=V_g$ (solid lines) and at a slightly smaller $V_d$ (dashed lines), illustrating the origin of current saturation in SB-CNFET's (Ref. 19).

In contrast to conventional FET's, the scaling of the performance here with $t_{ox}$ depends on the specific contact geometry. If the contact were infinitely thick, then the electrostatic potential near the right-angle corner would depend on distance as $z^{2/3}$.[21] For such a geometry, the turn-on voltage and $S$ would scale as $t_{ox}^{2/3}$, while the transconductance would scale as $t_{ox}^{-2/3}$. Thus there is not really a universal power law; rather, the behavior depends on the contact geometry. Nevertheless, the two geometries considered in Fig. 2 are rather well described by a single simple equation.

In addition to reducing the oxide thickness, the performance can be improved by using an oxide (or other gate dielectric) having higher dielectric constant.[2,8,13] In conventional transistors, this improves performance by increasing the gate capacitance, and hence the charge in the channel. However, in ballistic SB-CNFET's, the charge in the channel

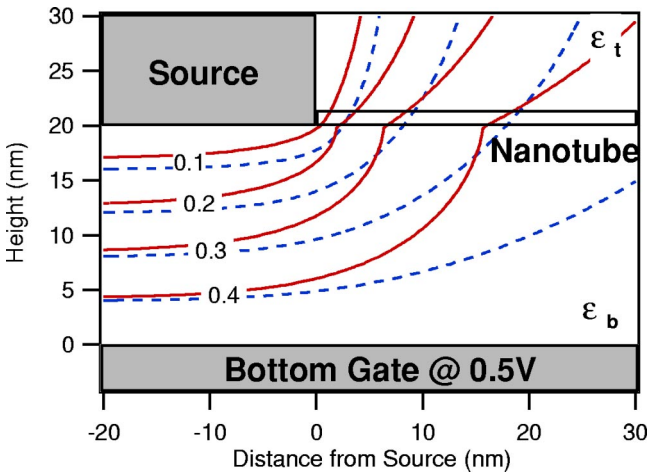


FIG. 4. (Color online) Contour lines of the electrostatic potential at the source contact for an interface between a high dielectric and vacuum (solid red lines, $\epsilon_b/\epsilon_t=11$) and a homogeneous dielectric (dotted blue lines). The value of adjacent contour lines differs by 0.1 V ($V_d=V_g=0.5$ V.)

is unimportant for the turn-on regime,[22] so the improvement observed in such devices[2] must have a different origin.

In fact, within the approximations made here, simply increasing the dielectric constant everywhere would have *no effect* on the turn-on. However, most actual devices studied use a thin gate oxide below the NT, with air above it. Figure 4 shows how the electrostatic potential changes due to the interface between dielectrics. The potential contour lines at the source contact are much closer in the case of an interface with $\epsilon_b>\epsilon_t$, resulting in a thinner SB. Thus the turn-on becomes much sharper.

In this geometry the improvement is large only for relatively thick oxides. This can be understood from the interface boundary condition $\epsilon_b\partial\phi_b/\partial y=\epsilon_t\partial\phi_t/\partial y$, where $\phi_{t,b}$ is the electrostatic potential on top of the interface or below it, and $\epsilon_{t,b}$ are the dielectric constants of the top and bottom oxide. The limit of large dielectric constant for the bottom oxide, $\epsilon_b/\epsilon_t\to\infty$, gives equipotential lines perpendicular to the interface. However, a distance on the order of the oxide thickness is needed for a drop of $V_g$ of the NT potential. Therefore, while the turn-on becomes sharper, it does not approach the limit $T(E)\approx 1$.

Our numerical calculations indicate that with high ratios $\epsilon_b/\epsilon_t$, large improvements can be achieved for thick oxides. However, the changes become rather small for very thin oxides. For example, for $t_{ox}=20$ nm, replacing the homogeneous oxide ($\epsilon_b/\epsilon_t=1$) by $HfO_2$ below and air above the NT ($\epsilon_b/\epsilon_t=11$) changes the slope $S$ from 240 mV/dec to 120 mV/dec. This improvement agrees well with experimental data.[2] For $t_{ox}=2$ nm, though, $S$ changes only from 95 mV/dec to 75 mV/dec.

We have focused here on the case of a midgap Schottky barrier. However, we have also examined the behavior for other values of the Schottky barrier. As long as the current is limited by tunneling through a SB, as for barrier heights of 0.2 eV or more, the scaling behavior derived here continues to hold.

We thank Bruce Ek for expert technical assistance, Shalom Wind for valuable experimental advice and discussion, and Jörg Appenzeller for helpful discussion. S. H. thanks the Deutsche Forschungsgemeinschaft for financial support under Grant No. HE3292/2-1.

*Electronic address: tersoff@us.ibm.com
‡Electronic address: avouris@us.ibm.com

[1] R. Martel, V. Derycke, C. Lavoie, J. Appenzeller, K.K. Chan, J. Tersoff, and Ph. Avouris, Phys. Rev. Lett. **87**, 256805 (2001).
[2] J. Appenzeller, J. Knoch, V. Derycke, R. Martel, S. Wind, and Ph. Avouris, Phys. Rev. Lett. **89**, 126801 (2002).
[3] S.J. Wind, J. Appenzeller, R. Martel, V. Derycke, and Ph. Avouris, Appl. Phys. Lett. **80**, 3817 (2002).
[4] A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker, Science **294**, 1317 (2001).
[5] S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and Ph. Avouris, Phys. Rev. Lett. **89**, 106801 (2002).
[6] T. Nakanishi, A. Bachtold, and C. Dekker, Phys. Rev. B **66**, 073307 (2002).
[7] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, Nature (London) **424**, 654 (2003).
[8] A. Javey, H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. McIntyre, P.L. McEuen, M. Lundstrom, and H. Dai, Nat. Mater. **1**, 241 (2002).
[9] R. Martel, T. Schmidt, H.R. Shea, T. Hertel, and Ph. Avouris, Appl. Phys. Lett. **73**, 2447 (1998).
[10] The nanotubes were prepared by laser ablation as described in A. Thess, R. Lee, P. Nikolaev, H. Dai, P. Petit, J. Robert, C. Xu, Y.H. Lee, S.G. Kim, A.G. Rinzler, D.T. Colbert, G.E.S. Scuseria, D. Tomanek, J.E. Fischer, and R.E. Smalley, Science **273**, 483 (1996). They were used without further treatment and dispersed in dichloroethane by a short exposure to ultrasound.
[11] M. Radosavljević, S. Heinze, J. Tersoff, and Ph. Avouris, Appl. Phys. Lett. **83**, 2435 (2003).
[12] S. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981).
[13] S. Rosenblatt, Y. Yaish, J. Park, J. Gore, V. Sazonova, and P.L. McEuen, Nano Lett. **2**, 869 (2002).
[14] P.L. McEuen, M.S. Fuhrer, and H. Park, IEEE Trans. Nanotech. **1**, 78 (2002); S. Wind, J. Appenzeller, and Ph. Avoiris, Phys. Rev. Lett. **91**, 058301 (2003).
[15] More accurate methods are available; see S. Datta, *Electronic Transport in Mesoscopic Systems* (Cambridge University Press, Cambridge, 1995). However, WKB is sufficient for our application. The transmission factor for tunneling is very low in the turn-on regime, so a careful treatment of the non-equilibrium charge is unnecessary. The current varies over orders of magnitude, so high precision is not essential, and absolute accuracy is limited by the absence of detailed structural information regarding the metal-nanotube contact.
[16] J.W. Mintmire and C.T. White, Phys. Rev. Lett. **81**, 2506 (1998).
[17] The main effect of charge on the NT (which we neglect) is to alter the potential within the NT channel. Source and drain SB's are

relatively unaffected in the energy range of significant tunneling current. The current is limited by the channel only when there is negligible charge in the channel. As a result, the approximation gives a good description of the current [except perhaps in the fully ''On'' regime (Ref. 22)], and so does not affect our conclusions.

[18] S. Heinze, J. Tersoff, and Ph. Avouris, Appl. Phys. Lett. **83**, 5038 (2003).

[19] We find numerically that, in the long-channel limit ($L_{NT} \gg t_{ox}$), $I$ and $S$ are nearly independent of $V_d$ for $V_d \gtrsim 0.1$ V, because current in the turn-on regime is then limited by the source and not the drain. Then we can conveniently describe ideal saturation by taking the limit of a vanishing drain barrier ($V_d = V_g$), where all carriers injected at the source can be collected at the drain. However, we note that in some cases our experimental devices exhibit apparent short-channel effects (Ref. 11). We have therefore verified numerically that, while the short-channel $S$ (at fixed $V_d$) is somewhat increased compared to the long-channel limit at any given $t_{ox}$, the observed trend of $S$ vs $t_{ox}$ persists. Thus our experimental findings can be adequately modeled using long-channel devices at ideal saturation and vanishing drain barrier.

[20] This interpretation is supported by transmission electron microscopy images of the device cross section, which show that our source/drain contacts are not nearly as sharp and perpendicular to the substrate as assumed in the simulation.

[21] P. M. Morse and H. Feshbach, *Methods of Theoretical Physics* (McGraw-Hill, New York, 1953).

[22] In the regime of full turn-on, if the Schottky barriers become sufficiently transparent, other factors can come into play in determining the current. Then effects that we neglect can become significant, including the (non-equilibrium) charge in the NT channel. Thus the gate-channel capacitance (and hence the dielectric constant) affects the maximum On-current, see J. Guo, S. Datta, and M. Lundstrom, cond-mat/0306199, IEEE Trans. Electron Devices (to be published).