Quantum interference in a one-dimensional silicon nanowire

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We study electronic transport within a lithographically defined silicon nanowire for zero and finite bias. The 10-nm wide and 500-nm long nanowire is fabricated by advanced electron-beam lithographic techniques. Transport experiments reveal clear quantum size effects in the conduction through the wire. Energy quantization within the wire leads to a shift in conduction threshold. Quantum interference effects cause an oscillatory pattern in the conductance. At low source-drain bias, transport is dominated by shallow tunneling barriers. At higher bias, additional nanowire modes are found to contribute to the conductance.

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I. INTRODUCTION

The quantization of conductance in narrow constrictions within two-dimensional electron systems (2DES's)—so-called quantum point contacts (QPC's)—was discovered fifteen years ago.[1,2] This conductance quantization is due to the contact resistance between the two-dimensional and one-dimensional regions of the system and the quantization of transverse modes in the 1D region. The effect is only established, however, when transport through the 1D region is ballistic, i.e., without (inelastic) scattering of the electrons, and when there is no extensive reflection at the opening of the 1D regions to the 2D reservoirs. Accordingly, for the observation of quantization effects in longer one-dimensional channels—''quantum wires'' or ''electron waveguides''—several requirements have to be met. The 1D channel should be essentially free of impurities and the potential experienced by the electrons should be sufficiently smooth.[3] Of course, for quantization effects to occur, the wire width has to be on the order of the Fermi wavelength. Due to these restrictions, most experiments following the original work were carried out in high mobility GaAs/AlGaAs heterostructures (e.g., Refs. 4–8) which can be grown at very low impurity concentration levels by molecular beam epitaxy. To date, the purest quantum wires were obtained by the cleaved edge overgrowth technique.[6] In these extremely clean wires conductance quantization up to a wire length of 20 μm could be resolved.

Due to the higher impurity concentration and the lower electron mobility in silicon microstructures, original attempts to observe conductance quantization effects in silicon failed. In fact, experiments on 1D transport in Si metal-oxide-semiconductor field-effect transistors (MOSFET's) first led to the discovery of the Coulomb blockade effect in semiconductor microstructures.[9] Quantized conductance was later seen in quantum point contacts on silicon and in silicon/germanium heterostructures[10] or in short silicon wires,[11] but it has not been possible to produce long quantum wires on silicon. As recent experimental progress demonstrates, however, silicon still has the potential to become the material of choice for the further reduction of structure size of nanowire devices. This will ultimately lead to the occurrence of many quantum size effects in silicon-based devices which are already known from compound semiconductors. Using local stress-limited oxidation Kedzierski and Bokor succeeded in fabricating quantum wire transistors with channel diameter of only 5 nm operating at room temperature.[12] Using a shifted resist pattern and orientation-dependent etching of silicon-on-insulator (SOI) films Namatsu *et al.* structured only 2 nm wide wires[13] whereas Cui and Lieber were able to synthesize doped silicon nanowires by laser-assisted catalytic growth.[14] In this paper, we present experimental evidence for the occurrence of quantum size effects in the conduction through a lithographically defined SOI nanowire with width of only about 10 nm embedded in a MOSFET structure.

II. EXPERIMENT

For sample preparation 10-Ω-cm *p*-type separation by implantation of oxygen (SIMOX) wafers with a silicon film thickness of 50 nm and a 400 nm thick buried oxide (BOX) were used. After protection of the active transistor area with a standard photoresist the source and drain regions of the SOI-MOSFET were implanted with As ions at an energy of 10 keV and a dose of 2×10^{15} cm^{-2}. In order to obtain thinner silicon films, a sacrificial thermal oxide was grown on the upper Si layer with a thickness of 44 nm, consuming about 20 nm of silicon. After stripping the oxide in buffered hydrofluoric acid (BHF), a mesa structure was defined in the remaining 30 nm thick silicon film by conventional photolithography and reactive ion etching (RIE). Using high-resolution low-energy electron-beam lithography and the negative electron resist hexaacetate *p*-methylcalix[6]arene (MC6AOAc)[15] we structured the silicon wires with a lateral diameter of about 10 nm by RIE in the nonimplanted active transistor regions. The etched wire was passivated by rapid thermal oxidation (RTO) at 950 °C resulting in a high quality oxide of about 15 nm thickness. After this oxidation an additional 40 nm thick SiO_2 layer was deposited on top of the sample. Next, contact holes were opened in the source and drain regions by wet chemical etching in BHF with a photoresist masking. Finally, a metallic top gate was evaporated simultaneously with the bond pads. In Fig. 1(a) a sketch of the quantum wire is shown. In Fig. 1(b) we present the nanowire defined in MC6AOAc with a width of only about 8 nm. Since etching widens the structure and oxidation leads to a final shrinkage, the final wire width can be assumed to be about 10 nm.

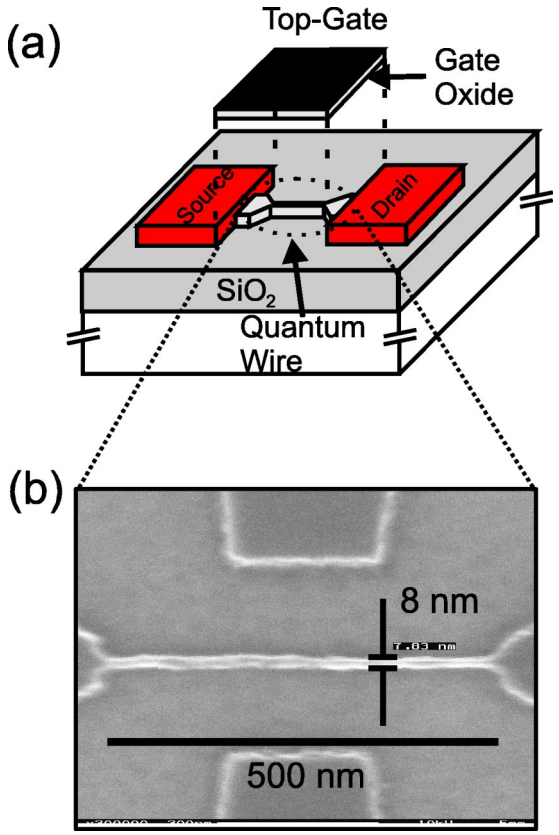

FIG. 1. (a) Sketch of the SOI nanowire: a metallic top gate is separated from the silicon quantum wire by a 55 nm silicon oxide. (b) SEM micrograph of the nanowire defined in Calixarene with a width below 10 nm and a length of 500 nm.

The samples were bonded into a chip carrier and brought into the sample chamber of a variable temperature insert mounted in a helium cryostat with a minimum bath temperature of 1.5 K. The measurement setup consisted of a low-noise current preamplifier and a standard lock-in amplifier operated at a frequency of 130 Hz, applying an ac voltage with amplitude $v_{\mathrm{SD}}=100\ \mu$V across source and drain. Measurements at higher source-drain bias V_{SD} were performed by superimposing a dc offset to the ac sensing signal.

III. RESULTS AND DISCUSSION

A. Zero bias

In Fig. 2 the two-terminal conductance $g=dI_D/dV_{\mathrm{SD}}$ of the 10 nm nanowire is shown as a function of the top gate voltage V_{TG}. Here, I_D denotes the drain current. For comparison, we also plotted the corresponding trace for a similar nanowire with a width of approximately 25 nm. The conductance values of the nanowires shown in Fig. 2 have been corrected for the influence of serial resistances adjacent to the quantum wires. In our structures, a relatively large undoped area of the SOI film below the metallic gate connects the highly doped source and drain regions to the quantum wire. From the resistance of the whole structure at high gate voltages and from measurements on unstructured samples we estimate the serial resistance to be $R_{\mathrm{serial}}\approx 10\ \mathrm{k}\Omega$. This resistance strongly influences the conductance values measured in the two-terminal setup, in particular at high gate voltages, introducing some uncertainty in the absolute value of the conductance.

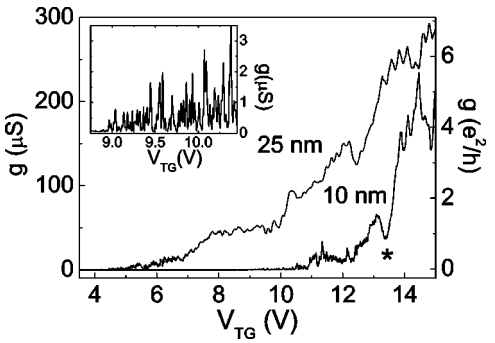

FIG. 2. Top gate voltage dependence of the conductance of a 25 nm wide and a 10 nm wide silicon nanowire. The conductance in the narrow wire starts to rise at much higher gate voltage values than in the wide wire. This offset is due to the lateral energy quantization in the narrow wire. The asterisk marks a gate voltage value above which a strong increase in conductance can be noticed. This threshold behavior is caused by shallow tunnel barriers at the wire openings or within the wire (see text). Inset: Magnified view of the conductance trace for the 10 nm wire between $V_{\mathrm{TG}}=8.5$ and 10.5 V. The first resonances appear at $V_{\mathrm{TG}}=8.9$ V which is taken as the onset gate voltage. The conductance peaks in this region remind of Coulomb blockade resonances. The mean spacing between adjacent conductance peaks corresponds roughly to the charging energy for the whole wire (see text).

The conductance of the 25 nm wire starts to increase at a top gate voltage of $V_{\mathrm{TG}}=4.3$ V. In contrast, the conductance of the 10 nm wire starts to increase at a gate voltage $V_{\mathrm{TG}}=8.9$ V, i.e., at a voltage 4.6 V higher than for the 25 nm wire. This indicates that the onset of conduction through these nanowires is not determined by the inversion threshold voltage of the 2DES in the contacts but by quantum size effects in the wires. We here define the threshold voltage V_{th} as the top gate voltage at which conduction starts in the absence of quantum confinement. For structures with $w \gg \lambda_F$ (where w is the wire width and λ_F is the Fermi wavelength of the electrons in the 2D contacts), we find $V_{\mathrm{th}}=3.4$ V. It is expected that electron transport through the wires can occur only when the wire width exceeds $\lambda_F/2$.[4] The Fermi wavelength can be obtained from the electron sheet density n_s via

$$\lambda_F=\left(\frac{4\pi}{n_s}\right)^{1/2} \tag{1}$$

and the sheet density can be estimated from the capacitance per unit area $\tilde{C}=\epsilon_r\epsilon_0/d=6.3\times10^{-4}$ F/m^2, where $\epsilon_r=3.9$ is the permittivity and $d=55$ nm is the thickness of the gate oxide. Neglecting stray capacitances, the sheet density is obtained from the capacitance via $n_s=\tilde{C}V_{\mathrm{TG}}^*/e$, where $V_{\mathrm{TG}}^*=V_{\mathrm{TG}}-V_{\mathrm{th}}$ is the top gate voltage in excess of the threshold voltage. In Eq. (1) the spin and valley degeneracies for silicon have been accounted for. Inserting the values for our structure, one obtains

$$\lambda_F \approx 56\ \text{nm} \times \sqrt{\frac{1}{V_{\text{TG}}^*[V]}}. \tag{2}$$

From the quantum condition for the onset of conduction when $2w=\lambda_F$, one obtains $w=29$ nm for the 25 nm wire and $w=12$ nm for the 10 nm wire. In the presence of stray capacitances these values will be slightly smaller and lie even closer to the lithographic dimensions of the wires. We therefore continue to use the lithographic dimensions of the wires also as the ''electronic'' dimensions. In order to obtain a scaling factor α which translates between the gate voltage and energy scales, we consider the quantization energies for the transverse modes in the wires: Assuming a hard wall potential in the wires, the transverse energies are simply given by

$$E_n = \frac{\hbar^2 \pi^2}{2m^*} \frac{n^2}{w^2}, \tag{3}$$

where $m^*=0.19m_e$ is the relevant effective mass for silicon. Thus, for the first level in the 25 nm wire one obtains $E_1^{25}=3.2$ meV and for the first transverse level in the 10 nm wire the energy is $E_1^{10}=19.8$ meV. Equating the difference between the onset voltage for the 10 nm wire and the corresponding quantization energy, we obtain

$$\alpha = \frac{E^{10}}{e(V_1^{10}-V_{\text{th}})} = 3.60\times 10^{-3}. \tag{4}$$

For the 25 nm wire, almost the same value is calculated (3.56×10^{-3}). The energy of the second transverse mode for the 10 nm wire is $E_2^{10}=79.2$ meV and the corresponding voltage $V_2^{10}=V_{\text{th}}+E_2^{10}/e\alpha=25.6$ V lies well outside of our measurement range. Thus, in the gate voltage range displayed in Fig. 2, transport through the 10 nm wire is carried solely by the first transverse mode. For the 25 nm wire the second mode is expected to come into play at $V=7.0$ V and the third mode at $V=11.5$ V. The fourth mode is not occupied within the accessible voltage range.

Obviously, both conductance traces displayed in Fig. 2 do not exhibit quantized plateaus. This, however, is not expected for a wire of length $L \gg \lambda_F, w$. In long wires, transmission resonances due to multiple reflections at the wire entrances or at one or several scattering centers within the wire may completely obscure the quantization of conductance.[4] The conductance values themselves are in the correct range expected from transport carried by one or a few transverse modes. However, as mentioned above, due to the uncertainty in the value of the series resistances, the absolute value cannot be determined accurately. In the following we concentrate on the 10 nm nanowire whose zero bias transport properties are completely dominated by the lowest 1D subband in the structure.

Our interpretation of Fig. 2 as a result of quasiballistic one-dimensional transport through the 10 nm wire is further supported by the absence of strong charging effects which would result in Coulomb blockade (CB) oscillations. Such oscillations are found by other groups in experiments on similar SOI nanowires.[16] In Ref. 16, wire width fluctuations due to edge roughness are made responsible for the formation of a serial arrangement of electron islands with large charging energies. The absence of such CB in our structure indicates that the potential within the nanowire is relatively smooth and 1D transport is, in principle, possible. There is, however, some indication that charging of the *whole* wire might play a role in the gate voltage region close to the onset of conduction. In the inset of Fig. 2, the conductance of the 10 nm wire in the gate voltage range between $V_{\text{TG}}=8.5$ and 10.5 V is shown. In this region, a large number of conductance resonances can be seen. Their mean spacing was determined to be $\Delta V_{\text{TG}}=30\pm 10$ mV. This corresponds to an energy spacing of $\Delta E = e\alpha \Delta V_{\text{TG}} \approx 100\ \mu$eV. The expected conductance peak spacing for the wire can be estimated from its gate capacitance $C_{\text{TG}} \approx \tilde{C} \times l \times w \approx 3$ aF which corresponds to $\Delta V_{\text{TG}} = e/C_{\text{TG}} = 50$ mV or $\Delta E = 180\ \mu$eV. This shows that the spacing between conductance resonances is at least on the same scale as the charging energy of the wire or of a somewhat larger structure. At the same time, however, the thermal energy $k_B T = 130\ \mu$eV is also on this scale and charging effects should, in principle, be suppressed. Regardless of the actual origin of the resonances at conduction onset, there is no indication of charging effects due to a subdivision of the nanowire into small islands corresponding to a much larger charging energy.

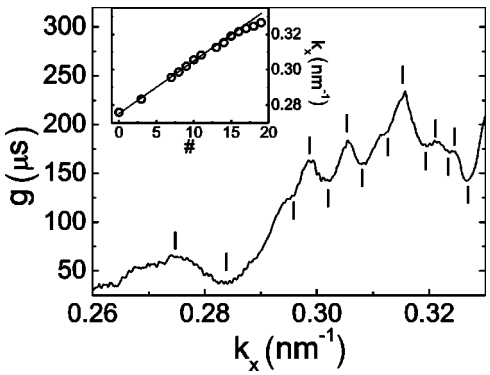

FIG. 3. Resonant structure in the conductance of the narrow wire. Here the conductance is plotted as a function of the longitudinal wave number k_x of the electrons along the transport direction. The maxima and minima are marked with vertical bars. In the inset, the positions of these extrema are plotted against their position number (starting arbitrarily at 0 for the feature with the lowest k_x value). The maxima and minima are well fit by a straight line corresponding to a resonant length which is roughly the wire length.

The wavelike nature of the electrons in the silicon wire results in a resonant structure in the conductance which is shown in Fig. 3. Here the conductance is displayed as a function of the longitudinal moment k_x which is calculated from the gate voltage via

$$k_x = \frac{1}{\hbar}\sqrt{2m^*[e\alpha(V_{\text{TG}}-V_{\text{th}})-E_1^{10}]}. \tag{5}$$

For clarity only the pronounced resonances are shown which occur at higher gate voltages. In a waveguide of

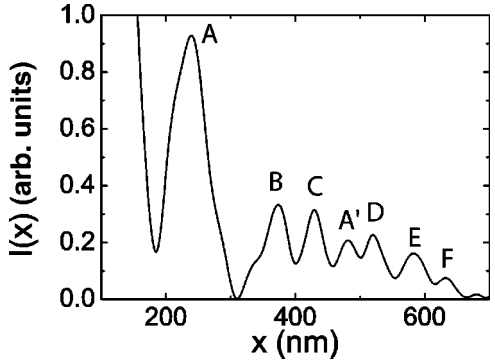

FIG. 4. Power spectrum of the conductance trace in Fig. 3. The peaks correspond to resonances with spatial frequencies 240 nm (A,A′), 375 nm (B), 430 nm (C), 520 nm (D), 580 nm (E), and 630 nm (F).

length L, one expects the distance between adjacent transmission maxima and minima to be

$$\Delta k = \frac{\pi}{2L}. \tag{6}$$

To determine the resonant length within the nanowire which is responsible for the resonances in Fig. 3, we assigned integer numbers to each of the maxima or minima and plotted the corresponding momentum values against their index number (Fig. 3 inset). The data is well fit by a straight line with slope 2.97×10^{-3} nm^{-1}. This corresponds to a resonant length of approximately 530 nm which agrees very well with the lithographic length of our silicon wire. We have to mention that a similar oscillatory conductance pattern is also found for the 25 nm wire at high top gate voltages (see Fig. 2). Due to the presence of several modes in this wire, however, the analysis is less straightforward than in the 10 nm wire.

It is possible that additional fine structure in the conductance trace could appear at lower temperatures. At $T=1.5$ K the thermal length $l_T=\sqrt{\hbar D/k_B T^4}$ for our system is approximately 50 nm (here the diffusion constant is $D=v_F^2\tau/2$ and we assumed as a typical scattering time $\tau=1$ ps). Long-wavelength fluctuations on a scale $\lambda \gg l_T$ are expected to be averaged out. This does not seem to play a significant role in our nanowires at least up to the wire length. However, at lower temperatures, additional features could appear corresponding to small wave numbers k.

Nonetheless, the conductance trace contains fluctuations corresponding to smaller lengths than the wire length and a single spatial frequency cannot account for the complex conductance oscillations visible in Fig. 2. We therefore performed a Fourier transform (FT) of the conductance $g(k_x)$ to reveal the major periodicities hidden in the data. Figure 4 shows the power spectrum $I(x)=|\tilde{g}(x)|^2$ of the conductance trace [where $\tilde{g}(x)$ is the FT of $g(k_x)$].

The major contribution (peak A) comes from resonances corresponding to a spatial period of approximately 240 nm. However, the asymmetric shape of peak A indicates that it is composed of several resonances in close proximity. Other

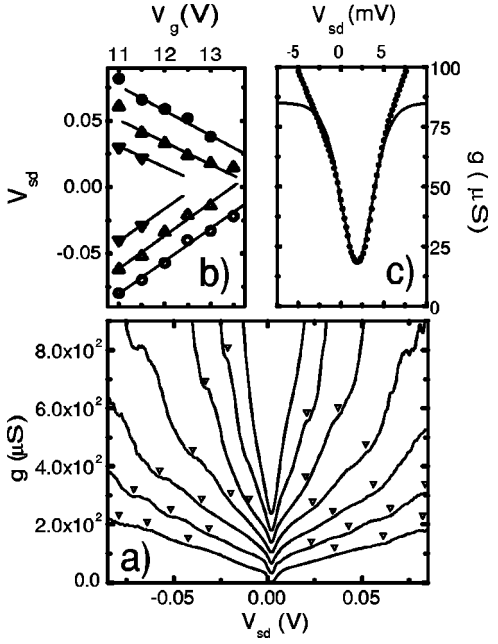

FIG. 5. Conductance $g=dI_{SD}/dV_{SD}$ of the nanowire at finite bias. (a) From bottom to top, conductance traces for $V_{TG}=11$, 11.5, 12.0 , 12.5, 13.0, and 13.5 V are displayed. The traces are offset for clarity. Triangular markers point at distinct features within the conductance traces which are plotted in part (b) of this figure. (b) Bias voltages V_{SD} at which the features marked in (a) appear, as a function of V_{TG}. (c) Expansion of the central part of the g-V_{SD} trace for $V_{TG}=13$ V. A curve fit based on a simple model (see text) is also shown. The experimental data are plotted as dotted line, the fit is drawn as a continuous line.

contributions are found at 375 nm (peak B), 430 nm (C), 520 nm (D), 580 nm (E), and 630 (F). For peaks B and C it cannot be ruled out that these are in fact higher harmonics of resonances with smaller spatial period. Peak A′ (480 nm) most probably is the first harmonic of peak A. Peak D corresponds to the period observed in Fig. 3 and finally peaks E and F most probably are also ''genuine'' contributions and not harmonics. As the higher spatial periods all correspond well with the lithographic wire length, these resonances may be interpreted as transmission resonances due to reflections at the wire entrances. Lower periods correspond to multiple reflections due to edge roughness or impurities within the wire. The presence of these resonances clearly demonstrates that the wavelike nature of the electrons in the nanowire structure is preserved and results in a distinct oscillatory conductance pattern. At the same time the presence of several distinct spatial periods shows that the wire is not completely free of impurities or other sources of disorder. The nanowire thus behaves like a moderately disordered wave guide for electrons.

B. Finite bias

In Fig. 5(a), the conductance $g=dI_D/dV_{SD}$ of the narrow nanowire is shown as a function of the source-drain bias V_{SD} for increasing values of the gate voltage. For clarity, only six representative traces of a total of fifty recorded in the range

from $V_{TG}=11-15$ V are displayed. For the traces with $V_{TG}<13.5$ V, a distinct dip around zero bias can be discerned, whereas all the conductance traces exhibit several conductance plateaus or resonances at higher bias voltages. As can be seen in Fig. 5(b), these features evolve linearly with the applied bias. As some of the conductance features are barely discernible, we verified their exact locations by also considering the derivative of the conductance traces. Conductance plateaus indicate the contribution of additional conductance channels with increasing bias V_{SD}. Additional energy levels within the nanowire can be occupied when the electrochemical potentials within the leads become large enough. In the left and right contacts, the electrochemical potentials are assumed to be of the form $\mu_L=e\alpha V_{TG}^*+e\beta\eta V_{SD}$ and $\mu_R=e\alpha V_{TG}^*-e\beta(1-\eta)V_{SD}$, respectively. Here, the factor η accounts for a possible asymmetry in the voltage drop over the wire and the conversion factor $e\beta$ translates bias voltages into energies. Obviously, $\mu_L-\mu_R=eV_{SD}$. From the above expressions for μ_L and μ_R, the slopes of the ''resonant lines'' in Fig. 5(b) are obtained as $dV_{SD}^{(L)}/dV_{TG}=-\alpha\beta^{-1}\eta^{-1}$ and $dV_{SD}^{(R)}/dV_{TG}=\alpha\beta^{-1}(1-\eta)^{-1}$, respectively. From this, the asymmetry can be determined to be $\eta=0.63$. This is also reflected in the slightly asymmetric conductance traces in Fig. 5(a). With the previously determined value for α, the scaling factor β is obtained as $\beta=0.38$. In principle, the values for α, β, and η could be used to determine the energies corresponding to the conductance plateaus or resonances. However, we were not able to match these energies with any characteristic energy of the nanowire (such as, e.g., the energy of higher transverse modes). Presumably the scaling factors α and β are not independent. At higher source-drain voltages, the electrochemical potentials might be more complicated functions of the applied voltages than stated above. Unfortunately, in this experiment we had no alternative method to establish an energy scale.

The distinct dip around $V_{SD}=0$ is found in all the $g-V_{SD}$ traces recorded for gate voltages below ≈ 13.5 V. It can be explained by the presence of several shallow tunneling barriers at the exits of or within the nanowire. Such shallow barriers might be formed by slight fluctuations in the wire width or, e.g., by band gap reduction due to compressive strain induced by oxidation of the wire.[17] Although we have no direct evidence, we show that our data obtained for low source-drain bias are consistent with the existence of two such tunneling barriers. In fact, in this regime a fairly good fit to the conductance traces could be achieved by assuming that transport be dominated by two shallow parabolic barriers. As one example, in Fig. 5(c) the conductance trace for $V_{TG}=13$ V is shown for low bias voltages together with a curve fit based on the model. The transmission of a single parabolic tunneling barrier is given by[18]

$$T_p(E)=\{1+\exp[-2\pi(E-V_0)/\hbar\omega]\}^{-1}. \quad (7)$$

Here V_0 is the height of the barrier and $\hbar\omega$ determines its width. The total transmission function $T(E)$ of the system was obtained by combining the individual transmission functions of two barriers incoherently and the current was calculated from the formula[19]

$$I=\frac{2e}{h}\int T(E)[f_L(E)-f_R(E)]dE. \quad (8)$$

In this expression $f_{L,R}$ denote the Fermi distributions for the left and right contacts, respectively. The conductance was obtained from the current by numerical differentiation. As the experimental conductance minimum is at a nonuniversal value (i.e., not at an integer multiple of the conductance quantum), the curve had to be shifted vertically to obtain good correspondence with the experimental data. The asymmetry with respect to $V_{SD}=0$, however, is well reproduced by assuming tunneling barriers of slightly different heights. From the fit, we obtained $V_0=33$ meV for one barrier and $V_0=35.6$ meV for the other. For both barriers, $\hbar\omega$ was taken to be 7.2 meV. For other traces similar values for V_0 (between 30 and 35 meV) were found. Of course, in the experiment the conductance does not saturate due to the contribution of higher modes which were not considered in the model.

The height of the barriers obtained from our model is slightly higher than the energy of the first transverse mode. In Fig. 2, this leads to a strong reduction of the zero-bias conductance even when the gate voltages are high enough to occupy this lowest eigenmode (i.e., when $V_{TG}>V_1^{10}$). The gate voltage needed to overcome the higher of the two tunneling barriers is given by $V_{th}+35.6$ meV$/e\alpha=13.3$ V. This value coincides very well with the gate voltage value at which a strong and sudden increase in conductance is visible in Fig. 2 (marked with a star).

IV. SUMMARY AND CONCLUSION

We have fabricated a 10 nm wide and 500 nm long nanowire within a SOI-MOSFET structure using advanced electron beam lithography and etching processes. Due to size quantization within the wire, the threshold gate voltage above which conduction sets in is significantly enhanced. The wavelike nature of the electrons in the structure leads to distinct oscillations in the conductance which are due to multiple reflections and interference of the electron waves. The transverse quantization energies and the oscillation pattern are consistent with the lithographic dimensions of the wire. At finite source-drain bias additional conduction modes are occupied, leading to a strong increase in conductance. A distinct dip in the conductance traces around $V_{SD}=0$ is found for low gate voltages which can be explained by the existence of a few shallow tunneling barriers within the wire. Our studies show that even in an imperfect silicon nanostructure pronounced quantum effects can occur when lithographic techniques are pushed to their limits which is of utmost significance for the future development of silicon-based nanoelectronics.

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