Carrier transport and density of state distributions in pentacene transistors

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We present a density of state model for the transport properties of pentacene field effect transistors. Using a one-dimensional transistor model we study the effect of different localized trap distributions on the current-voltage characteristics of such devices. We find that a distributed trap model with a steep exponential band tail of donors and a shallower exponential tail of acceptors inside the band gap can describe consistently our experimental data obtained from bottom-gate polycrystalline pentacene transistors for different gate dielectrics and under various external conditions.

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I. INTRODUCTION

Organic materials have received increased attention in the last several years as materials for electronics, as they promise a bulk processing of flexible and/or large-area devices at low cost. In particular, the number of available organic semiconductors with a wide range of materials and transport properties is growing fast. In order to utilize these materials best, it is important to understand the physical basis of their transport properties, and how they depend on fabrication conditions and the operating environment.

One class of organic semiconductors is based on acenes, with pentacene as the most prominent member, because of its high band mobility of up to 1.5 $cm^2/V\,s$.[1,2] The transport properties of pentacene are known to depend crucially on the fabrication procedure, and disorder and/or impurities in the current-carrying channel can reduce the carrier mobility by several orders of magnitude. The temperature dependence of the mobility in single-crystalline pentacene ($\mu \propto T^{-2.5}$) suggests a bandlike transport of extended states. For polycrystalline pentacene the situation is more complex, and different models based on grain boundary potential barriers, potential wells, and trapping at localized gap states[3–5] have each been proposed.

During the growth of pentacene on a substrate, grain boundaries and defects are incorporated into the pentacene film. Lin *et al.* (Ref. 3) suggested that poor molecular ordering at the semiconductor-substrate interface causes a severe degradation of the transport properties, as they demonstrated that a surface-treatment with self-organizing molecules such as octadecyltrichlorosilane, which form an ordered growth template for the pentacene molecules, increases the mobility substantially.

Much is known about the role of structural disorder in inorganic semiconductors such as amorphous silicon, which typically form continuous random networks. These materials are characterized by a low free-carrier mobility, shallow band tail localized states, and deep defect states. The organic materials are molecular solids with weak intermolecular interactions, and the detailed correlation between the structural disorder and behavior of thin film transistors is not fully understood. Much of the information about transport in organic materials now comes from transistor data, and a correct interpretation of the device characteristics is necessary to extract the transport information. Transistors are sufficiently complex devices that the material physics of electronic transport cannot easily be extracted from the data. In the inorganic materials, it has proven valuable to use a physics-based numerical model to relate the transistor characteristics to the underlying physical mechanisms.

We have therefore developed this type of numerical model for organic transistors, and have applied this to pentacene to identify the transport mechanisms. The immediate issue is whether a trap model or a potential barrier model is a more appropriate description of transport. The evidence for the potential barrier model in a thin film transistor (TFT) is the fit to Levinson *et al.*'s model[6] which predicts the drain current as function of the gate voltage in the linear regime. However, our recent work has shown that Levinson *et al.*'s model alone is not sufficient to confirm the grain boundary mechanism.[5]

The numerical simulation calculates the impact of localized states on the transport properties of pentacene. Using the gradual channel approach the potential and charge distribution in the TFT channel is calculated as function of an assumed localized density of states in the semiconductor. The modeling results are compared to data measured on high-mobility organic TFT's made from thermally evaporated pentacene.[7,8] The model describes the observed *I-V* characteristics well, assuming a steep exponential band tail of donor states and a shallower exponential distribution of acceptor states. Though the number of states in each distribution varies from device to device, the width of these distributions appears independent of the dielectric material and external stimulations of the device. The ability to extract the density of states distribution and to identify the character of the states, begins the process of identifying their physical origin.

In the Sec. II we describe the model. Section III contains a comparison of model results with data measuered from some of our pentacene TFT devices. A discussion of the results and conclusions follow in Sec. IV.

II. MODEL

In a field effect transistor (FET) (Fig. 1) the source-drain current is carried by mobile charges through a narrow channel at the dielectric interface. By changing the gate voltage one controls the concentration of the mobile carriers in this

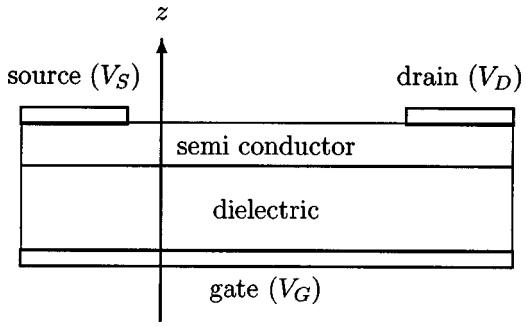

FIG. 1. Schematic plot of a bottom-gate FET. The arrow labeled *z* denotes the cut through the FET along which Eqs. (3) and (4) are solved. The channel length from source to drain contact is *L*, its height (in the *z* direction) is *H*, and its width is *W*.

region by biasing the (local) Fermi energy at the interface. Localized states with energies near the Fermi energy can influence the concentration of mobile charges, thereby changing the current-voltage (*I*-*V*) characteristics of a device.

In order to investigate whether observed *I*-*V* curves for pentacene thin film FET's can be explained by the presence of localized states in the channel area, we have developed a one-dimensional model to calculate the charge and potential distribution along a line through the layers of the FET (z axis in Fig. 1), assuming a density of states distribution of trap states in the semiconductor. In the linear regime (gradual channel approximation), when the source-drain voltage V_{DS} is much smaller than the gate voltage V_G, the potential difference between the gate electrode and the semiconductor hardly changes, and the carrier concentration in planes parallel to the dielectric interface becomes almost independent of the location within this plane. For these cases, our one-dimensional model is sufficient to describe the carrier concentration in the device and, for $V_{DS}\rightarrow 0V$ this region extends over almost all values of V_G.

Using this model we can calculate the source-drain current in the Ohmic linear regime as[9]

$$I_{SD}=\frac{W}{L}\mu_0 q c V_{DS}, \tag{1}$$

where μ_0 is the mobility of the excited carriers inside the bands (localized states have zero mobility and do not contribute to the current) and

$$c=\int dz c(z) \tag{2}$$

denotes the (gate voltage dependent) mobile charge carrier concentration integrated over the channel height *H*. $c(z)$ varies with the applied gate voltage and has a finite value only in a narrow region at the gate dielectric. Depending on the type of semiconductor and the source and drain contacts the carrier distribution $c(z)$ describes holes, electrons, or both. The charge and potential distributions within the channel are completely determined by the Maxwell equations and the continuity equations for the different carriers. In the gradual channel approximation applied here these equations need to be solved only along the *z*-direction (see Fig. 1) and, assuming steady-state conditions, reduce to

$$\partial_z[\epsilon(z)\partial_z\varphi(z)]=-q\{p(z)-n(z)+p_D(z)-n_A(z)\}. \tag{3}$$

and

$$p(z)=\int_{-\infty}^{E_V}\frac{dE\mathcal{D}(E)}{1+\exp\{-[E+\varphi_0-E_F-\varphi(z)]/k_BT\}},$$

$$n(z)=\int_{E_C}^{\infty}\frac{dE\mathcal{D}(E)}{1+\exp\{[E+\varphi_0-E_F-\varphi(z)]/k_BT\}}. \tag{4}$$

Here, $p(z)$ and $n(z)$ denote the hole and electron concentration, respectively, and $\mathcal{D}(E)$ is the density of electron states in the bands, which we approximate using a square root distribution[10]

$$\mathcal{D}(E)\propto\begin{cases}\sqrt{E_V-E}, & E\leqslant E_V\\ \sqrt{E-E_C}, & E\geqslant E_C\end{cases} \tag{5}$$

and an effective carrier mass of $1m_e$ (electron mass), in the absence of specific information about pentacene. $\varphi(z)$ is the external electric potential. $p_D(z)$ and $n_A(z)$ denote the occupied localized states and are given by

$$n_A(z)=\int\frac{dE\,N_A(E)}{1+\exp\{-[E+\varphi_0-E_F-\varphi(z)]/k_BT\}}$$

$$p_D(z)=\int\frac{dE\,P_D(E)}{1+\exp\{[E+\varphi_0-E_F-\varphi(z)]/k_BT\}}, \tag{6}$$

where $N_A(E)$ and $P_D(E)$ describe the distributions of the localized acceptor and donor states, respectively. The potential φ_0 denotes the difference of the ''local'' Fermi energy E_F from a reference energy and comes into play, if the FET consists of multiple layers of semiconductors, either from different materials or of the same material, but with different traps and/or doping states. In this case each layer has its own ''local'' Fermi energy E_F, while the φ_0 is the difference of the work function of this layer with a reference material (we typically use the bottom layer in the FET device). As it turns out, and is described in the Sec. III, we need an interface layer next to the dielectric that has a different distribution of trap states from the bulk material in order to explain the observed experimental results.

The potential and charge distributions in the device are calculated using a finite element approach. To allow for a good spatial resolution of the potential and charge distributions in the channel area, yet reduce the necessary computational load, we use an exponential mesh in the pentacene with a mesh size of less than 1 Å at the dielectric interface and a much larger mesh size at the opposite end. For a given gate voltage V_G we start the calculation with an approximate potential distribution from which we obtain a first guess for the charge distributions Eqs. 4 and 6. We then iterate through Eqs. (3), (4), and (6) until we arrive at a self-consistent solution. To calculate the *I*-*V* characteristics of a device we scan through a range of gate voltages.

In the accumulation regime of the transistor we can use the substitution[9]

$$qc = \frac{\epsilon}{D}\left(V_G - V_t - \frac{V_{DS}}{2}\right) \tag{7}$$

to rewrite Eq. (1) as

$$I_{SD} = \frac{W}{L}\frac{\epsilon}{D}\mu_0 V_{DS}\left(V_G - V_t - \frac{V_{DS}}{2}\right). \tag{8}$$

This expression is commonly used to extract the (band) mobility and the threshold voltage from experimental data. Here, ϵ and D are the dielectric constant and thickness of the gate dielectric, respectively.

III. RESULTS AND COMPARISON WITH EXPERIMENTS

We compare our model to thin film transistors (TFT) made from vacuum evaporated pentacene as channel material. The pentacene was deposited on highly doped silicon wafers coated with thermal oxide or plasma enhanced chemical vapor deposition (PEVCD) silicon nitride as gate dielectric. Gold source and drain contacts were deposited on top of the pentacene layer. The influence of the preparation conditions on the structural and electronic properties of the films was studied and described earlier.[7,8] For the following investigation we use high mobility pentacene TFT's with $\mu = 0.3 \ldots 0.6$ cm^2/V s.

Our measurements find that the pentacene transistors exhibit variability in their I-V characteristics even when deposited under nominally the same conditions. In particular, the gate voltages at which they turn on can differ by more than 10 V, while the measured carrier mobilities remain about the same. Similar variations in the onset current can be induced in a single sample by illumination. Our previous studies suggested that the variability is due to different densities of localized acceptor states, but the physical origin of the states is not determined. One of the purposes of this modeling study is to test this trap-state model.

In our numerical calculations we assume a gate dielectric thickness betwen $D = 100$ and 120 nm, and a pentacene layer height $H = 50$ nm, consistent with actual measurements of the geometry of the devices used for collecting the data shown here. The width to length ratio W/L varies from 6 to 10 in the devices discussed here. Also, because the gold contacts inject holes into the channel region, we consider only hole transport and localized states that influence directly the hole distribution in the simulations.

A. Thermal oxide dielectric

Figures 2 and 3 show experimental current-voltage (I-V) data for a pentacene transistor obtained with a small (2-V) source-drain voltage. It should be noted that the experimental points come from two different measurement methods. Mostly below the threshold voltage the drain-source current I_{DS} is measured using a dc gate voltage. This method leads to some bias-stress effects which cause a reduction in I_{DS} over time, and is more pronounced for higher gate voltages. To avoid these bias-stress effects we use a pulsed gate voltage for current measurements above the threshold voltage. Figure 2 shows that the threshold voltage V_T, as deduced from the slope of the linear regime is about -3 V, while the transistor turns on at about $+10$ V (cf. Fig. 3). It is the subthreshold region between the threshold voltage and turn-on voltage that we attribute to traps and is the focus of the model.

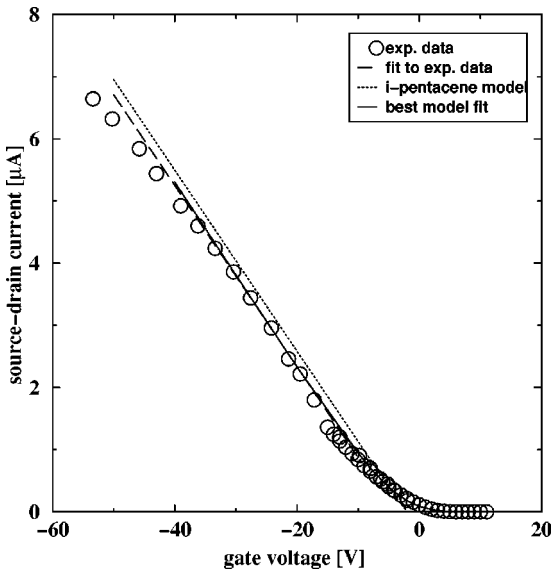

FIG. 2. A typical experimental I-V curve of one of our pentacene TFTs. By fitting the linear regime of the I-V curve to Eq. (8) we obtain a mobility of $\mu = 0.359$ cm^2/V s (broken curve). The dotted line is simulation data assuming intrinsic pentacene as channel material, and the solid curve is a model fit assuming an exponential distribution of low-lying donor states and deeper acceptor states (see the text for more details).

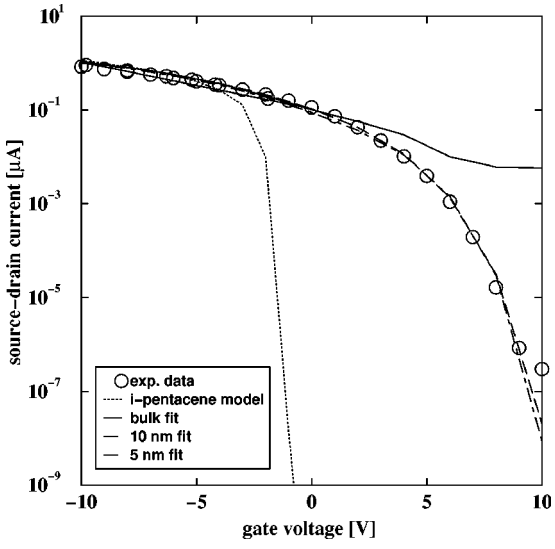

FIG. 3. I-V curve of the same sample as shown in Fig. 2, but as a log-lin plot. The dotted curve shows the expected current-voltage characteristics for a transistor made of intrinsic pentacene. The solid line shows the current if we assume bulk acceptor states in the model.

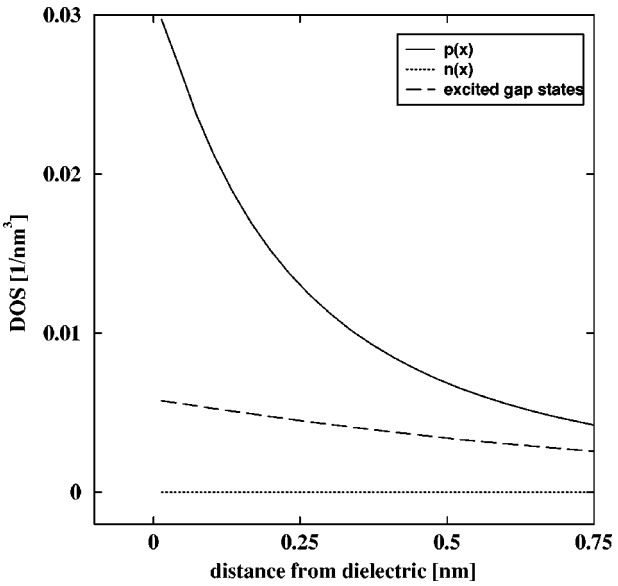

FIG. 4. The distribution of holes $[p(z)]$, electrons $[n(z)]$, and excited gap states at the dielectric interface for $V_G=-10V$.

The dotted curve in Fig. 2 is the calculated *I-V* curve assuming that the channel is made of intrinsic pentacene. As can be seen in Fig. 2 the sample has a higher threshold voltage than expected from a transistor made of ''perfect'' intrinsic pentacene. If we assume that the observed deviations of the *I-V* characteristics from the intrinsic pentacene model is due to localized states only, we need to introduce donor states in order to explain the shift of the threshold voltage to more negative values. The best fit of the experimental data in the linear regime is achieved using a steep exponential distribution ($w_E=40$ meV) of low-lying donor states. These states appear to agree very well with photocurrent and thermal deflection spectroscopy measurements that suggest an exponential band edge slope with a width of $w_E\approx 33$ meV. The best fit to the measured on-current data shown as solid curve in Fig. 2 is obtained using an exponential donor distribution with $E_{min}=0$, $E_{max}=0.2$ eV, $E_0=0$, $w_E=40$ meV, and $N^{tot}=5\times 10^{18}\text{cm}^{-3}$ (cf. the Appendix for the definition of the parameters). The concentration of donor states above $E_{max}=0.2$ eV is very small, and their effect on the *I-V* curve is negligible, justifying the cutoff for the numerical calculations at this energy level.

The holes that carry the current through the channel are concentrated in a thin (few nm thick) layer at the dielectric interface, as shown in Fig. 4. From the model calculations we cannot distinguish whether the donor states are interface or bulk states, as long as they are present within a 3–5-nm-thick layer next to the dielectric interface. However, photocurrent measurements suggest that these states are present within the bulk of the semiconductor.

Figure 3 shows the onset of the current in a log-lin plot. The current starts at a finite positive gate voltage, and, for our trap model, we have to introduce acceptor states to account for this shift. If intrinsic pentacene or pentacene with donor trap states only is assumed, then the current onset is at $V_G=0$ V, as shown by the dotted line in Fig. 3. Furthermore, the acceptor states must be deeper within the band gap than the donor states to have the desired effect on the *I-V* characteristics. The total concentration of acceptor states determines the onset voltage, and the distribution of these states determines the slope of the *I-V* curve at low currents.

TABLE I. Parameters for the acceptor states used to fit the onset current in Fig. 3. See the Appendix for the definition of these parameters.

d (nm)	N^{tot} (10^{21} cm^{-3})	w_E (eV)	$E_0=E_{min}$ (eV)	E_{max} (eV)
5	0.0048	0.2	0.03	0.9
10	0.0023	0.2	0.04	0.9

Our model clearly indicates that the acceptor states are located near the dielectric interface. If we assume them to be homogeneously distributed throughout the whole pentacene layer, then we observe a finite current even at high positive gate voltages (solid line in Fig. 3). This off-current is carried by holes that accumulate on the side of the pentacene layer opposite to the gate dielectric. However, if we assume the acceptor states to be present only in a thin (5–10 nm) layer at the dielectric interface, a good fit to the experimental data is obtained with an exponential trap distribution using the parameters shown in Table I.

The mobility value μ_0 used in the simulation model corresponds to the mobility obtained by fitting the experimental data in the accumulation regime ($V_G<-20$ V), where the source-drain current varies linearily with gate voltage, to Eq. (8). These values for μ_0 compare well with mobilities measured by Lin *et al.* for similar pentacene transistors,[11] and is about a factor 2–5 smaller than mobilities measured in OTS treated penatacene TFT's.[1,2] Due to the localized intraband states we observe a large turn-on regime where the field effect mobility, which is proportional to the slope of the *I-V* curve,

$$\mu_{FE}=\frac{LD}{WV_{DS}\epsilon}\frac{\partial I_{DS}}{\partial V_G}, \tag{9}$$

varies from zero to μ_0. In this turn-on regime, changes in the gate voltage lead to a change in both localized and mobile charge carriers, hence, effectively reducing the current through the transistor for a given charge accumulation. Figure 5 shows the field effect mobility normalized by μ_0. The turn-on voltage range depends on the concentration and distribution of the localized states and extends typically over about 20 V. Because of the increase in population of localized charge states in the turn-on regime we have to use the total charge carrier distribution in the substitution [Eq. (7)], and have to replace the band mobility μ_0 with the effective mobility

$$\mu_{eff}=\frac{c}{c+T}\mu_0, \tag{10}$$

in Eq. (8). Here, T denotes the hole concentration in the localized inter-band states. μ_{eff} is proportional to the ratio of mobile to total charge inside the channel and shows a similar V_G dependence as μ_{FE} (cf. Fig. 5), but remains substantially

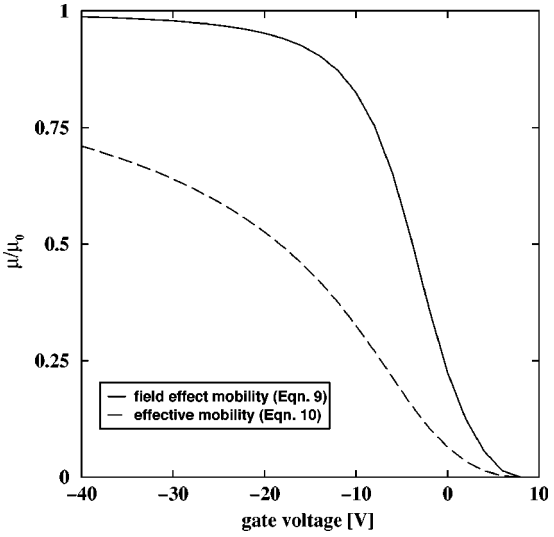

FIG. 5. Normalized field effect and effective mobility as functions of the gate voltage.

smaller than the free carrier mobility μ_0 in the gate voltage regime under investigation. This is a consequence of the large concentration of localized states that contribute to the total charge inside the channel. With decreasing number of localized states μ_{FE} and μ_{eff} both approach a step function with the value of μ_0 above and zero below the threshold voltage.

B. Effects of illumination

External stimulations can change the *I-V* characteristics significantly. For example, our pentacene TFT's show a shift of the onset and threshold voltage with illumination, which recovers slowly in the dark. Figs. 6 and 7 show several *I-V* curves taken during a one week period after the sample has

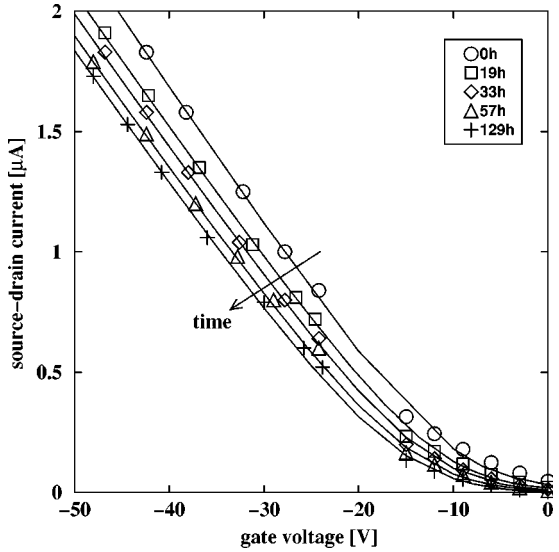

FIG. 6. Experimental *I-V* curves for a sample after about 2 hours of illumination. The data sets are measured at different times after the illumination has turned off. The markers indicate data from measured *I-V* curves, and the solid curves are model fits.

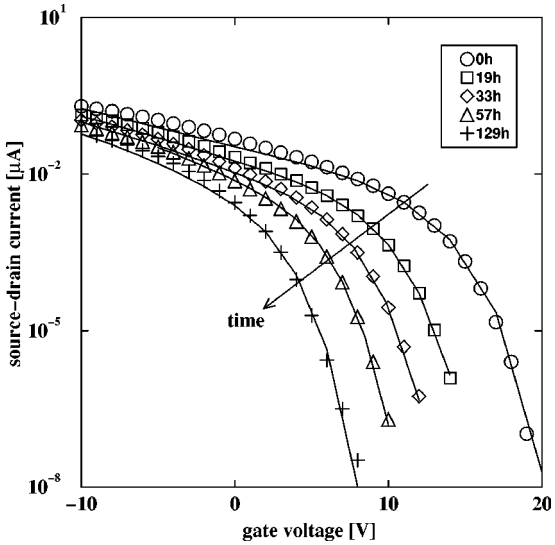

FIG. 7. Same data as shown in Fig. 6, but as a log-lin plot. The onset voltage decreases with increasing time after the turn-off of the illumination.

been exposed to about 2 h of light from a halogene lamp. During the illumination both the onset and threshold voltages shift to higher values, both at different rates. However, after one week the transistor has relaxed back close to its original state (cf. Table II). It should be noted that the illumination did not change the carrier mobility $\mu = 0.14\ \mathrm{cm^2/V\,s}$ of this sample. Using our trap state model as described earlier, we have fitted the data shown in Figs. 6 and 7. We achieve good fits with adjusting only the total concentration of the donor and acceptor states and the minimum energy of the acceptor states (cf. Table III). To account for the shift in the onset and threshold voltages with illumination we have to increase the acceptor and donor concentrations, respectively.

Another effect that can lead to a shift of the *I-V* curves is charge accummulation at the dielectric interface. In this case we would expect the same rate of change in the threshold and onset voltage over time, which is not what we observe experimentally. However, we could expect a combination of these two effects with part of the shift of the *I-V* curves due to bias stress effects, the other part due to change of the concentration of the localized trap states. With the current level of approximation within our model it is hard to extract the contributions from both effects uniquely.

TABLE II. Time evolution of the onset and threshold voltage of the transistor shown in Figs. 6 and 7 after 2 h of illumination. After 129 h the transitor characteristics are back to the values before the illumination.

time (h)	V_t (V)	V_{on} (V)
0	−9.23	19
19	−11.89	14
33	−13.00	12
57	−14.19	10
129	−16.00	8

TABLE III. Fitting parameters for the data sets shown in Figs. 6 and 7. All parameters not listed are the same as for the first sample discussed here.

time (h)	N_D^{tot} (10^{21} cm^{-3})	N_A^{tot} (10^{21} cm^{-3})	$E_{min}=E_0$ (eV)
0	0.018	0.0091	0.040
19	0.025	0.0072	0.050
33	0.029	0.0062	0.065
57	0.034	0.0052	0.070
129	0.038	0.0041	0.110

C. Silicon nitride dielectric

Figure 8 shows data from a transistor with plasma-deposited Si_3N_4 as dielectric. The different curves there correspond to repeated *I-V* curve measurements with a moderate gate voltage ($V_G=-10$ V) applied between the measurements. All three curves can be fitted using the trap state model. However, to account for the shift from positive to negative onset voltages the deep acceptor states have to be converted gradually into donor states (Table IV). On the other hand, since all the three curves have the same shape (i.e., they can be brought on top of each other by shifting them parallel to the *x* axis) we can achieve an equally good fit by assuming the trap state distribution of the right most data set and introducing a positive charge density at the dielectric interface that increases with the length of applied bias voltage. Since the shift of the curves is due to bias stress effects caused by applying a negative gate voltage over a certain period of time, the charging up of the interface seems to be the more physical approach for fitting the data. A similar bias-stress effect was observed in Si transistors with Si_3N_4 as the gate dielectric.[12]

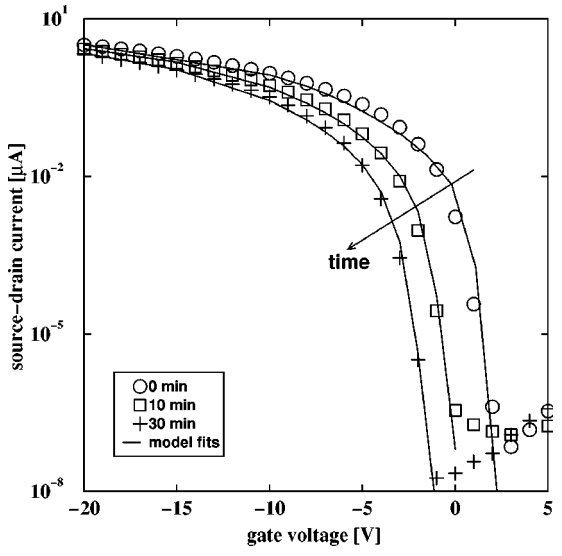

FIG. 8. Current-voltage characteristics for a sample with Si_3N_4 as the dielectric. The shift in the curves is due to bias stress effects. The bias stress effect can be modeled by either a change of the deep donor to acceptor states, or by an accumulation of positive charge in the dielectric.

TABLE IV. Parameters used for fitting the transistor data with Si_3N_4 as the dielectric. The data sets are numbered from highest to lowest onset voltage. $N_{D,tail}^{tot}$ is the total number of band tail donor states, $N_{D,deep}^{tot}$ and $N_{A,deep}^{tot}$ are the total number of deep band donor and acceptor states, respectively, and ρ_{diel} is the charge concentration at the dielectric interface. All concentrations are in units of 10^{21} cm^{-3}. The data sets are fitted using either the different trap state distributions, or the trap state distribution of set 1 and the charge at the dielectric interface.

time (min)	$N_{D,tail}^{tot}$	$N_{A,deep}^{tot}$	$N_{D,deep}^{tot}$	ρ_{diel}
0	0.033	0.0025	0	0
10	0.042	0.001	0.0028	0.002
30	0.053	0	0.005	0.0033

IV. DISCUSSION

We have used a distributed trap state model to investigate the effect of localized band-gap states on the *I-V* characteristics of pentacene TFT's. The first simulation results are quite encouraging, as they show that the experimental *I-V* curves can be consistently fitted assuming a shallow distribution of donor states and a deeper distribution of acceptor states. The donors cause a shift of the threshold voltage, while the acceptor states primarily cause a shift of the onset voltage. Moreover, the saturation of the donor states at low gate voltages results in an extensive linear current-voltage regime consistent with the experimental data.

External stimulations of the device such as illumination or stress biasing of the gate lead to changes in the *I-V* characteristics of our transistors. In the first case the threshold and onset voltages change at different rates during illumination, suggesting a change in the different trap state concentration. Bias stress effects, on the other hand, shift the whole *I-V* curve by a constant amount, and within the model a constant charge density at the dielectric interface fits the experimental data best.

Figure 9 shows the distribution of band and localized (trap) states we obtained from fitting the *I-V* characteristics shown in Figs. 2 and 3. The donor states form a narrow distribution close to the valence band edge, and their width and position agrees well with trap state measurements, as well as photocurrent measurements. The acceptor states are broader and deeper within the band gap. Models of this type generally cannot give a precise density of states distribution, because the calculated *I-V* characteristics largely depend on an integral over energy. Hence the fit is rather insensitive to small changes in the distribution and can be further affected by the depth distribution and/or the presence of states in the dielectric. However, the modeling can give a general shape to the distribution and can demonstrate consistency between different measurements.

The details of the electronic states near the band edge of these polymer systems are not known. However, a possible source for the distribution of localized donors is the presence of highest occupied molecular orbitals (HOMO) states that are shifted outside the valence band due to a slight misalignment of some molecules in the pentacene layer. The HOMO states in pentacene are centered at the C atoms of the center

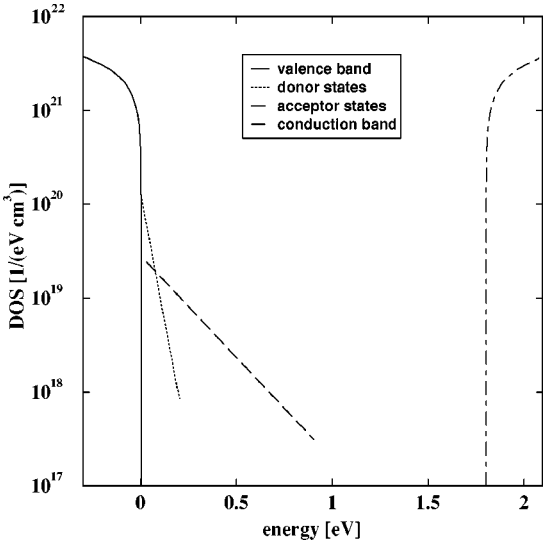

FIG. 9. Distribution of band and localized states for the sample discussed in the text. All energies are relative to the valence band edge which is set to $E_V = 0$ eV.

ring and misalignments of adjacent molecules can prevent sufficient overlap of the HOMO wave functions for the formation of extended (band) states. Misalignments can be introduced into the pentacene layer by the growth conditions and/or the roughness of the substrate. An exponential band tail is a common result of disorder in amorphous or polycrystalline materials, and therefore it is not surprising that it also appears in organic solids such as pentacene. The acceptor states appear to be extrinsic, because their density varies in different samples. Oxygen-related defects seem a plausible origin, and deep-level transient spectroscopy measurements of pentacene films on SiO_2 substrates revealed trap states at energies comparable to pentaceneqinone and anthraqinone defects.[14–16] However, our measurements give no specific information about the nature of the observed trap states.

Our distributed trap state model gives a consistent explanation of the device characteristics of our pentacene transistors, even though it does not distinguish between states inside the grain and at grain boundaries, but assumes a constant trap state density throughout the channel area. This is in agreement with results from laser-annealed poly-Si TFT's. Two-dimensional computer simulations suggested that both intragrain and grain boundary localized states are necessary for a complete understanding of the transport properties of those devices.[13] However, in the regime where the gradual channel approach is valid ($|V_G| > |V_{DS}|$), it is not possible to extract the two different distributions and a single distribution of interband states with a steep band tail part and a broad deep band part describes those devices well. The grain boundary trap states reveal themselves only in the saturation regime of the transistor where the screening of the trap states localized at the boundaries results in a lowering of the grain barrier with increasing gate voltage, reducing saturation effects. A trap state model has also been used successfully to describe the subthreshold characteristics of thin film transistors with poly(3-dodecylthiophene) as the semiconducting material.[17]

In conclusion, we have shown that a trap state model can consistently describe the *I-V* characteristics of pentacene transistors made with different gate dielectrics and under varying external conditions. The distribution consists of a steep band tail of donors, which agree well with photo current and thermal deflection spectroscopy measurements, and a broader deep band tail of acceptors, which agree well with results from transient current decay measurements.[18]

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APPENDIX DISTRIBUTIONS OF LOCALIZED STATES

We describe the interband donor and acceptor states with an exponential distribution of the form

$$P_{exp}(E) = C_{exp} e^{-|E-E_0|/w_E}, \tag{A1}$$

where E_0 denotes the maximum, and w_E the width of the distribution. The total number of states in this distribution is obtained through

$$N_{exp}^{tot} = \int_{E_{min}}^{E_{max}} dE\, P_{exp}(E). \tag{A2}$$

The energies E_{min} and E_{max} limit the range of the distribution. The energies E_{min}, E_{max}, and E_0 are typically specified with respect to the valence band edge.

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