Tuning the room temperature nonlinear I-V characteristics of a single-electron silicon quantum dot transistor by split gates: A simple model

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We propose an experiment that potentially allows a single-electron silicon quantum dot transistor to operate at room temperature. The emitter and collector of the device consist of silicon quantum wires and the base contains a single silicon dot buried in silicon dioxide. We suggest that split gates are added to the usual experimental situation, to provide additional and variable confinement perpendicular to the transport direction in the emitter and collector regions. The current-voltage curve is calculated using the Bardeen transfer Hamiltonian method. The potential defined by the gates is approximated to a harmonic form. We predict the nonlinear structure in the current-voltage curve, will survive to room temperature for systems with an emitter and collector with dimensions of the order 20–40 nm, and where the harmonic potentials have subband level spacing of the order 4–8.5 meV. Furthermore, we predict that the peak positions and peak to valley ratios in the current-voltage curve can be ''tuned'' by changing the split gate voltage.

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I. INTRODUCTION

The development of gas phase growth methods[1] and a variety of other techniques[2–4] have made it possible to produce silicon quantum dots with sizes of the order of 5 nm, that have spacings between the energy levels of the order k_bT at room temperature—a necessary requirement for high-temperature single-electron transistor operation. A range of experimental techniques have been used to probe these zero-dimensional (0D) states, among which transport measurements[5,6] reveal that the current-voltage (I-V) characteristics are highly nonlinear. A typical experimental setup for studying these transistors consists of quantum dot(s) buried in silicon dioxide situated between a polysilicon emitter and collector. The resonant tunneling of electrons through the discrete state(s) in the dot(s) causes a nonlinear structure to appear in the I-V. In addition, a gate is usually situated above the dot region to control the energies of the discrete dot(s) state(s). Using this setup, nonlinear I-V survives up to 150 K.[1] In this paper we demonstrate theoretically, how the temperature range for which nonlinear I-V manifests, can be extended to room temperature.

We propose a variation to the standard experimental setup, where the gate above the dot region is omitted and split gates are grown above the emitter and collector, to define additional confinement lateral to the electron transport direction. The potential of the split gates can be altered to change the lateral confinement, and thus alter the density of states (DOS) in the leads, thereby ''tuning'' the resulting I-V. Previously, a three terminal resonant tunneling diode (RTD) (Ref. 7) with donors in the base, used gates to alter the lateral area of the emitter to less than 0.1 μm^2. The I-V characteristic of the RTD (Ref. 8) was found to be sensitive to the gate voltage. We use the split gates with similar effect, except we produce lateral confinement on a much smaller scale, of the order of nanometers for a single lateral direction. Previous calculations for etched structures[9–11] demonstrate that the quantization of the DOS in the leads (in this case defined by the doping profile and charge on the surface of the device), allows the nonlinear structure in the I-V to survive to higher temperatures (but not as high as room temperature). In addition, these structures have fixed confinement and cannot be tuned.

We present a simple model for calculating the I-V and demonstrate that strong confinement defined by the split gates, results in the nonlinear I-V surviving to room temperature. Room-temperature nonlinear I-V has been measured for a device where the leads consists of narrow wire channels that are 20 nm wide.[12] However, our proposed device is much easier to fabricate, and allows the tuning of the I-V response. The survival of the nonlinear I-V to room temperature is crucial for the construction of industrially viable multistable logic circuits, and other applications such as current mixers and multipliers.[13]

II. THE MODEL AND QUANTITATIVE ASPECTS OF I-V

The proposed device shown in Fig. 1, consists of a double well quantum wire structure consisting of polysilicon and silicon dioxide layers. The silicon layers form the emitter and collector and the base region is the central oxide layer. The silicon layers have sides of length L in the x and z directions, and the confinement in the y direction is defined by the split gates. The base has a width w in the z direction. The emitter and collector are in equilibrium with electron reservoirs [with three-dimensional (3D) DOS] provided by metal contacts or doped regions (not shown). A single silicon quantum dot with typical dimension 4–6 nm is buried in the middle of the silicon dioxide base region. In the z and x directions the emitter and collector form quantum wells. The split gates are grown above the emitter and collector (separated by an insulating oxide layer) to define variable confinement in the y direction. Given that the silicon dioxide provides a large (3.15 eV) barrier and the width of the base is of the order 20 nm, direct tunneling of electrons from emitter to collector is

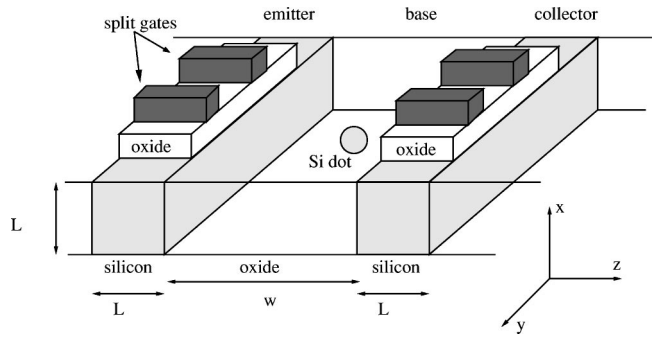

FIG. 1. The schematic diagram of the proposed device (not shown to scale) consists of a double well quantum wire structure made from the materials silicon and silicon dioxide. The central oxide layer with width w in the z direction forms the base region, and has a silicon dot at its center. The silicon layers with square cross section with sides of length L in the x and z directions, form the emitter and collector. There are split gates fabricated on top of oxide layers grown on the emitter and collector, to define variable confinement in the y direction. The split gate voltages, the split gate separations, and thickness of the oxide layer can be changed to tailor the confinement in the y direction. The device rests on a silicon dioxide layer, below which is the silicon substrate.

very unlikely and electrons must ''hop'' through the discrete states in the dot. A linear potential is applied in the z direction—the transport direction. The current from the emitter to the collector can be tuned by altering the DOS in the emitter and collector by changing the voltage of the split gates.

The system is modeled using the Bardeen transfer Hamiltonian technique,[14–17] where the total Hamiltonian is approximated as a sum of separate Hamiltonians for the emitter, the base region, and collector:

$$H = H_{\mathrm{em}} + H_d + H_{\mathrm{co}}, \tag{1}$$

where em and co denotes the emitter and collector regions and d denotes the dot in the base region. The eigenstates of the separate Hamiltonians Ψ_{em}, Ψ_d, and Ψ_{co} and their energies E_{em}, E_d, and E_{co} are defined by their respective Schrödinger equations. Previous calculations show that for the emitter and collector sizes we are considering, with typical gate oxides thicknesses and split gates separation, the potential defined by the split gates will only vary by a small amount along the x direction.[18] We shall therefore ignore this small variation and approximate the potential defined by the split gates to a 1D form. This approximation, together with approximating the oxide barriers in the x direction as hard walls, allows the potentials in the emitter and collector to be separated in the Cartesian directions. The Hamiltonians then have the form

$$H_{\mathrm{em}} = \frac{\hbar^2 \nabla^2}{2m^*} + V_{\mathrm{em}}(x) + V_{\mathrm{em}}(y) + V_{\mathrm{em}}(z), \tag{2}$$

$$H_{\mathrm{co}} = \frac{\hbar^2 \nabla^2}{2m^*} + V_{\mathrm{co}}(x) + V_{\mathrm{co}}(y) + V_{\mathrm{co}}(z) \tag{3}$$

with separable solutions $\Psi_{\mathrm{em}}(\mathbf{r}) = \Psi_{\mathrm{em}}(x)\Psi_{\mathrm{em}}(y)\Psi_{\mathrm{em}}(z)$ and $\Psi_{\mathrm{co}}(\mathbf{r}) = \Psi_{\mathrm{co}}(x)\Psi_{\mathrm{co}}(y)\Psi_{\mathrm{co}}(z)$. The effective mass difference between silicon and silicon dioxide has been ignored by using the spatially average value for silicon, thus setting $m^* = 0.19 m_0$. The potentials in the emitter and collector in the transport direction $V_{\mathrm{em}}(z)$ and $V_{\mathrm{co}}(z)$ have the form of finite potential wells with height 3.15 eV, which is the conduction band offset for the Si/SiO_2 system. For the potential in the emitter and collector in the x direction $V_{\mathrm{em}}(x)$ and $V_{\mathrm{co}}(x)$, hard walls are imposed at the silicon-silicon dioxide interfaces, as stated above, greatly simplifying the calculation by ignoring the relatively small penetration of the wave function into the oxide. The wave functions $\Psi_{\mathrm{em}}(x)$ and $\Psi_{\mathrm{co}}(x)$ therefore, are analytic functions, whereas $\Psi_{\mathrm{em}}(z)$ and $\Psi_{\mathrm{co}}(z)$ must be found numerically.

In the y direction the potential is defined by the split gates. The split gates are kept at equal negative voltage, so that no current can flow between the gates. The accurately calculated potential defined by the splits gates evolves from a square well form to a harmonic form with more negative split gate voltage.[18–20] To model the potential profile defined by the split gates a harmonic form is used (the most suitable choice for a strongly confined system), thus $V_{\mathrm{em}}(y) = V_{\mathrm{co}}(y) = ay^2$. The constant a can be tuned by changing the split gate voltage. The wave functions $\Psi_{\mathrm{em}}(y)$ and $\Psi_{\mathrm{co}}(y)$ have the well known form for the solution of the quantum mechanical harmonic oscillator, with energy levels separated by ΔE_y eV. We estimate that split gate separation should be of the order of 100 nm to achieve a useful value for ΔE_y, though a detailed analysis of the electrostatics is necessary to estimate the split gate voltage and separation required.[18]

In the base region, the shape of the quantum dot is set to a cube and the Hamiltonian has the form

$$H_d = \frac{\hbar^2 \nabla^2}{2m} + V_d(x) + V_d(y) + V_d(z) \tag{4}$$

with separable solutions $\Psi_d(r) = \Psi_d(x)\Psi_d(y)\Psi_d(z)$. The potentials $V_d(x)$, $V_d(y)$, and $V_d(z)$ form into finite quantum wells. However, for simplicity of calculation, we impose hard walls at the interface between the oxide and silicon in the x and y directions. Again, the wave functions $\Psi_d(x)$ and $\Psi_d(y)$ are analytical functions, whereas $\Psi_d(z)$ is found numerically.

A linear potential drop is applied from the left edge of the emitter to the right edge of the collector in the z direction. The electrons hop from the emitter to the dot, and then from the dot to the collector, resulting in a net flow of charge from the emitter to the collector. The direct hopping between the emitter and the collector is neglected, since such tunneling events are relatively unlikely, given the large and wide barrier presented by the base oxide. The matrix elements $M_{\mathrm{em/co}\text{-}d}$ for the transitions from the emitter/collector to the quantum dot within the Bardeen transfer Hamiltonian[14–17] technique has the form

$$M_{\text{em/co-}d}=\left|\left(\frac{\hbar^2}{2m}\right)\int(\Psi_{\text{em/co}}\nabla\Psi_d^*-\Psi_d^*\nabla\Psi_{\text{em/co}})dxdy\right|^2 \times\delta(E_{\text{em/co}}-E_d), \quad (5)$$

where $E_{\text{em/co}}$ and E_d are the energies of the emitter/collector and dot states. Similar expressions exist for hopping of the electron from the dot to the emitter/collector. The integral to generate the matrix elements is performed in the plane with constant z halfway from the center of the dot to the emitter/collector. The discrete states in the emitter and collector are phenomenological broadened, to account for the disordered quasicrystalline nature of polysilicon. This is achieved by selecting an exponential form for the delta function, with the broadening parameter set to k_bT at 50 K. The current into the dot I_{in} from the emitter and collector has the form

$$I_{in}=(1-P_D)\left[\int F(E_{\text{em}})M_{\text{em-}d}dE+\int F(E_{\text{co}})M_{\text{co-}d}dE\right] \quad (6)$$

where P_D is the occupancy of the quantum dot state and $F(E_{\text{em/co}})$ are the Fermi-Dirac occupation factors of the electrons in the emitter/collector. Similarly, the current leaving the dot I_{out} is given by

$$I_{\text{out}}=P_D\left[\int[1-F(E_{\text{em}})]M_{d\text{-em}}dE+\int[1-F(E_{\text{co}})]M_{d\text{-co}}dE\right]. \quad (7)$$

These integrals in energy are evaluated by considering the appropriate discrete energy levels in turn. The integrals over the x-y plane to generate the matrix elements are evaluated numerically, when a parabolic form is used for the confinement potential defined by the split gates. If a square well with hard walls is used instead, the integrals become products of trigonometric functions and can be evaluated analytically. The dot occupancy P_D and current from emitter to collector I are calculated by applying the steady state condition $I_{\text{in}}=I_{\text{out}}$ and solving the simultaneous Eqs. (3) and (4).

The electrostatic fringing edge effect caused by the finite size of the split gates in the transport direction has been neglected in the model. The fringing effect becomes less important with increasing split gate length in the z direction, and for the sizes considered can almost certainly be neglected, as the corrections to the DOS in the leads would be relatively small. We suggest that the split gates could be extended by 2–4 nm out of the emitter and collector, thus moving the fringing potential into the surrounding area, away from the leads where the electron density is highest. The 1D harmonic potential used, should then be an even more reasonable approximation to the true potential profile in the emitter and collector regions.

As the voltage is swept to measure the I-V, for certain voltages the dot state(s) will be aligned with a maximum or with maxima of the 0D DOS of the emitter and collector, whereas for other voltages the dot state(s) will be aligned with a minimum or minima of the 0D DOS in the emitter and collector. This can give rise to nonlinear features in the I-V. Furthermore, as the dot state(s) sample the different subbands in the emitter and collector with different number of nodes in their 3D wave functions, with either odd or even symmetry in the x-y plane, the matrix elements for hopping into and out of the dot can fluctuate rapidly with voltage, causing further nonlinearity in the I-V. Given the complexity of the expression for the current, we cannot predict the position of the peaks in the I-V using a simple picture, and they must be found numerically.

III. RESULTS

The quantum dot is modeled as a cube with sides 4 nm across. The I-V is first calculated for a device with parameters $L=80$ nm and subband spacing in the y direction ΔE_y set to 2.1 meV. The DOS in the emitter and collector shown for various sizes and spacings is shown in Fig. 2. In Fig. 2(a), the DOS is approaching the nonoscillatory form for a 3D system, and we have effectively 3D-0D-3D tunneling, as in the standard experiments.[1] It should be noted that the DOS is proportional to E in this case and not $\sqrt{E}$ as is normally seen for a 3D free electron DOS, due to the parabolic confinement in the y direction. The I-V is then considered for a smaller device with parameters $L=40$ nm and $\Delta E_y=4.21$ meV. The DOS in the emitter and collector shown in Fig. 2(b) exhibits nonlinear fluctuations, and clearly does not have the form for a 3D system. Finally, we consider a strongly confined system with parameters $L=20$ nm and $\Delta E_y=8.42$ meV where the DOS in the emitter and collector, as shown in Fig. 2(c), is highly oscillatory.

The following calculations have emitter and collector Fermi levels μ_L and μ_R, respectively set to 80 meV, this is a parameter in the model. For simplicity, only the ground state is included in the quantum dot. The calculated I-V curve in Fig. 3 for a device with parameters $L=80$ nm and $\Delta E_y=2.1$ meV is compared with the graph when a square well of length 80 nm replaces the harmonic potential. The curves show similar nonlinear features to the features seen experimentally, and a similarly small current. The I-V in Fig. 3 calculated at 300 K shows a little nonlinear structure, this structure vanishes when the emitter and collector size is increased and we effectively have 3D-0D-3D tunneling (not shown). A harmonic potential in the y direction defined by the gates is used for remaining calculations, which is more physical for strong confinement in the emitter and collector.

Figure 4 shows the calculated I-V as a function of temperature for a device with parameters $L=40$ nm and $\Delta E_y=4.21$ meV. The low temperature I-V has, as expected, a threshold voltage which must be applied before sizeable current can flow from emitter to collector. Furthermore at high voltage, a current peak survives to room temperature. As the temperature is raised, states at lower voltage previously fully occupied in the emitter and collector become partially occupied, and a current can flow at lower applied voltage generating additional peaks. Figure 5 shows the calculated I-V as a function of temperature for a device with parameters $L=20$ nm and $\Delta E_y=8.42$ meV. The peaks are very sharp

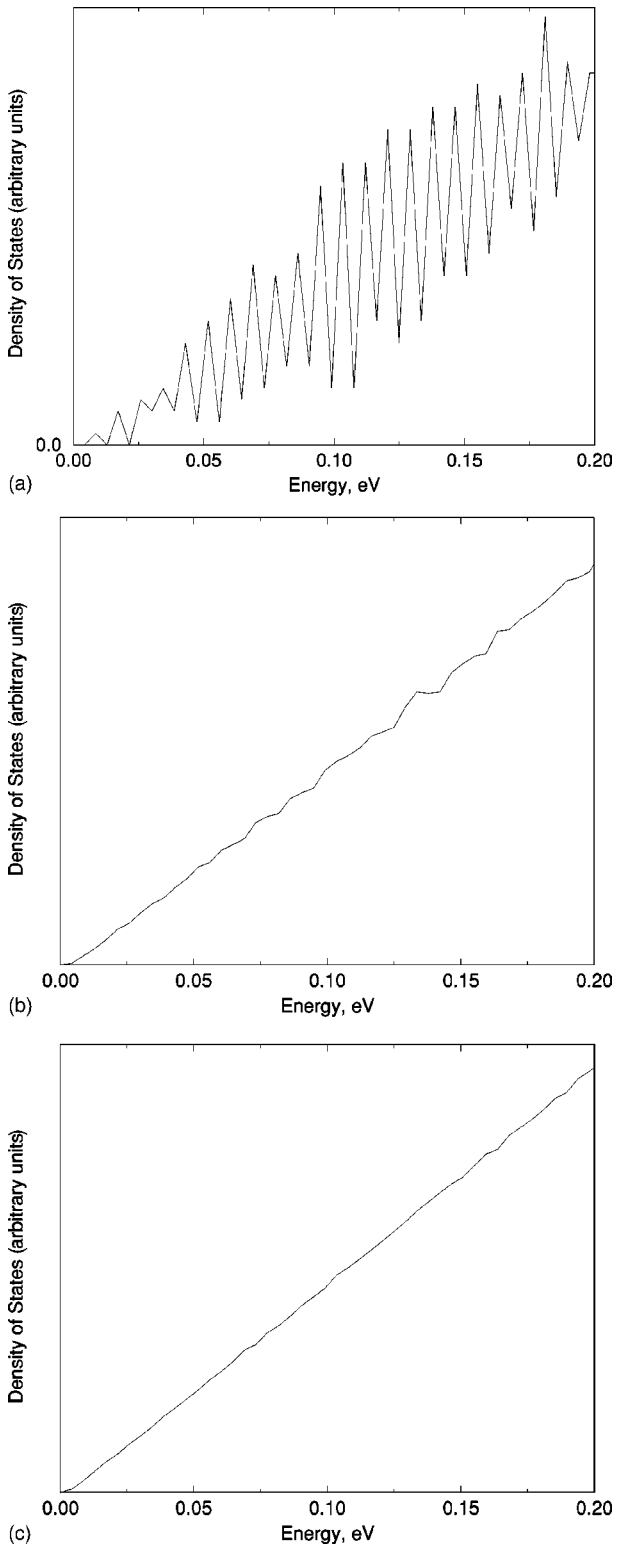

FIG. 2. Variation in the form of the energy dependence of the density of states in the emitter and collector with sides of length and energy level spacing in the y direction given by (a) $L=80$ nm and $\Delta E_y=2.10$ meV, (b) $L=40$ nm and $\Delta E_y=4.21$ meV and (c) $L=20$ nm and $\Delta E_y=8.42$ meV. Note that the wide contacts and narrow energy spacing shown in (a), the 3D similar to the DOS is proportional to E not $\sqrt{E}$ due to the parabolic potential well in the y direction.

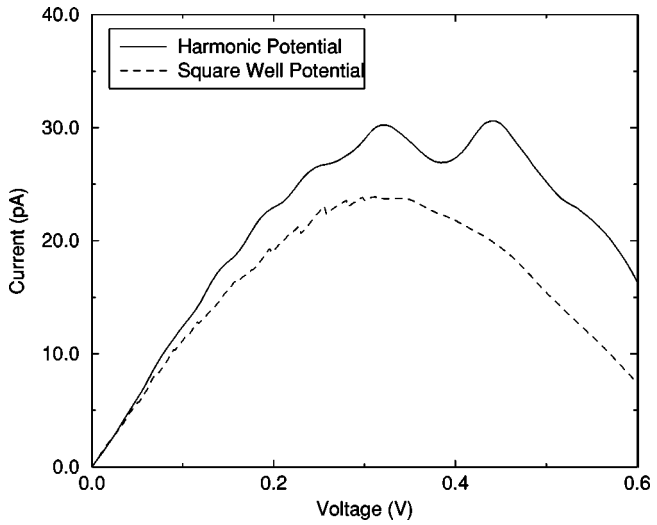

FIG. 3. The calculated I-V at 300 K for a device with lead with sides of length $L=80$ nm and $\Delta E_y=2.10$ meV (solid lines) compared with the I-V for when an infinite square well with width 80 nm replaces the harmonic potential in the emitter and collector defined by the split gates (dotted lines). The two curves are not radically different.

compared to peaks observed in previous graphs, and the corresponding peak to valley ratios also increase with stronger confinement in the emitter and collector. The graphs reveal clear trends: the separation of the peaks in the I-V increases in voltage and becomes sharper and thermally more robust in energy as we reduce the size of the emitter and collector and impose stronger confinement from the gates, reflecting the transition of the DOS in the emitter and collector from an almost 3D to a 0D form.[12]

In Fig. 6, we show the change in the room temperature I-V when small changes are made to the split gate voltage. The I-V curves for parabolic energy level spacings of $\Delta E_y=9.35$, 8.41, and 7.65 meV and $L=20$ nm are shown. The

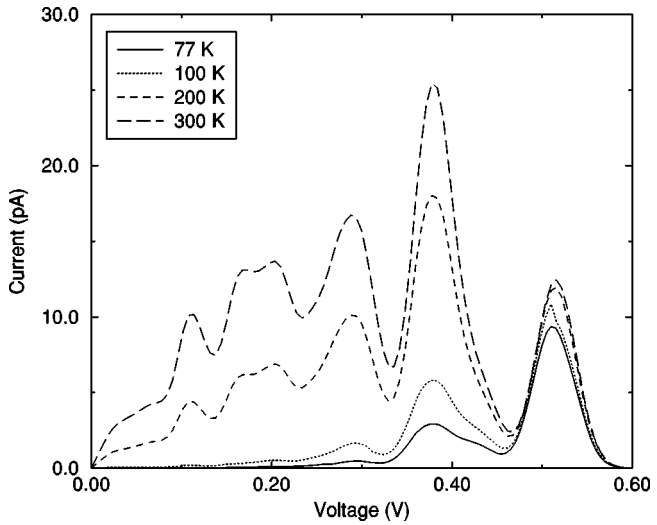

FIG. 4. The calculated temperature dependence of the I-V for a device with leads with sides of length $L=40$ nm and $\Delta E_y=4.21$ meV.

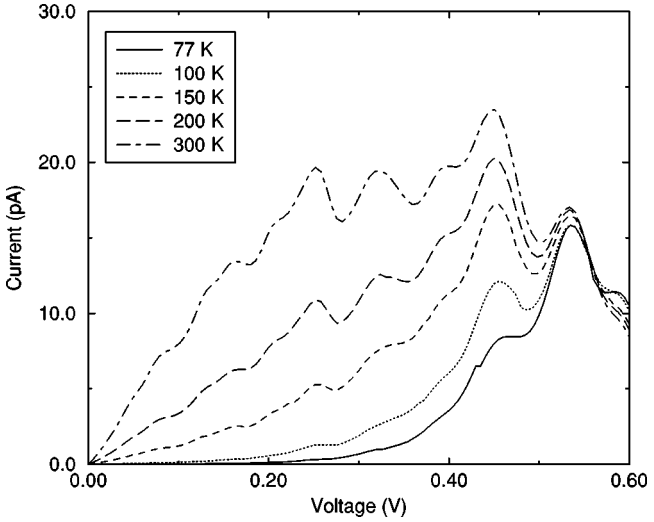

FIG. 5. The calculated temperature dependence of the *I-V* for a device with leads with sides of length $L=20$ nm and $\Delta E_y = 8.42$ eV.

peak to valley ratios and the peak positions are very sensitive to changes in the parabolic potential, thus the *I-V* can be tuned by varying the split gate voltage. The peaks in Fig. 6 move to higher voltage as the parabolic subband spacing increases. As the parabolic subband spacing is decreased by a relatively small amount, the emitter state below the Fermi level decreases in energy. Therefore, a larger voltage must be applied before this state lines up with the dot state, to allow a sizable current to flow. However, if we consider large changes to the parabolic subband spacing, then the state previously above the Fermi level could move below the Fermi level, and this will allow a sizable current to flow at low voltage, altering the *I-V*, this we believe is not observed for the small changes in parabolic subband spacing considered in Fig. 6.

The current in the calculations can be increased either by

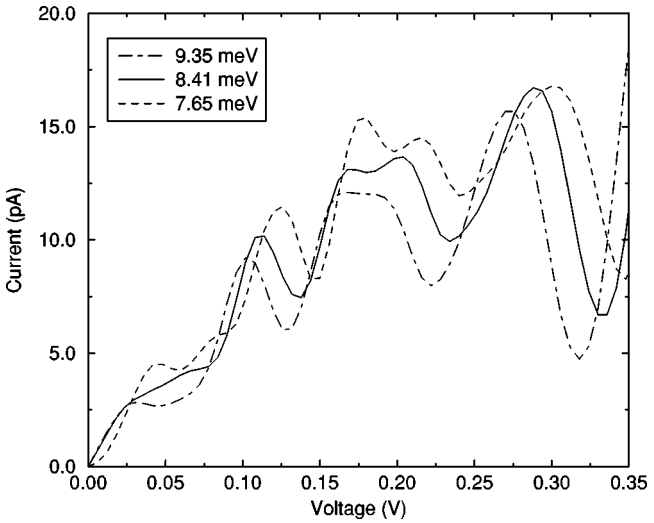

FIG. 6. Tuning of the *I-V* at 300 K by altering the split gate voltages. The calculations are shown for $\Delta E_y = 9.35$, 8.42, and 7.65 meV. The device has leads with sides of length $L=20$ nm.

introducing more dots in the base region as in some experiments, or by reducing the width of the base region. The magnitude of current as suggested by Eq. (3) is partially determined by the product of decaying exponentials of the wave functions in the transport direction, thus reducing the width of the base region, will increase the magnitude of the current exponentially.

In the experimental situation the dot(s) cannot be placed accurately or manufactured with identical shape and dimensions, thus one cannot manufacture identical devices (with identical *I-V*) as demanded by industry. However, given the peak positions and peak to valley ratios may be tuned by the value of the split gate voltage, we have the possibility of ''tuning'' a population of devices to have the same or very similar *I-V* relations for a given interval of voltage. This scheme may nullify the need to make identical devices, thus simplifying the industrial exploitation of the proposed device.

IV. DISCUSSION

We have presented a simple model for calculating the current of a device where the 0D DOS of the emitter and collector can be tuned by split gates. The calculations show that room temperature nonlinear *I-V* can exist for relatively strong confinement in the emitter and collector. We have used approximate forms for the confinement potential defined by the split gates, ignoring their finite size in the transport direction. However, a calculation of the potential profile and energy levels that includes all the boundary conditions would be computationally involved,[21] and is best performed in parallel with future experimental work.[22] We are confident that the inclusion of split gates to define additional confinement in the leads, should facilitate the survival of nonlinear *I-V* to room temperatures, or at the very least push up considerably the maximum temperature at which nonlinear *I-V* occurs. We note, one could use square gates[21] instead of split gates. The square gate will define (at zero voltage from emitter to collector) a tunable harmonic potential in the *z* and *y* directions.

We have only formulated a single particle model, whereas in reality many electrons can occupy the silicon dot. Typically for small dots with radii 1–3 nm, the energy difference between the ground state energy for when two electrons occupy the dot instead of one is between 0.48–0.12 eV.[23] Thus for a given dot size below a threshold voltage, the single particle model will be accurate, since it would be energetically impossible for two electrons to occupy the silicon dot at equilibrium. Beyond this threshold voltage, more than one electron can occupy the silicon dot and the Coulomb interaction will change the energies of the dot states, thereby altering the peak positions in the *I-V*.

The experimental and theoretical investigation of fundamental processes in condensed matter physics that can be carried out, using the proposed device includes (i) the electron-phonon interaction which can reduce the peak to valley ratio in the *I-V*, but should be less important with higher confinement in the leads and (ii) the interaction of the device with electromagnetic radiation and an applied ac volt-

age, which again will depend on the *I-V* and the DOS in the leads and dot(s). The device is compatible with the existing silicon technology, however, similar devices can be fabricated using III/V materials by a combination of molecular beam epitaxy (MBE), self-organized growth of quantum dots[24–26] and split gate techniques.[27] The latter system, given the relatively small band offsets of, e.g., GaAs/AlGaAs, will allow a sizable direct current to flow from emitter to collector, in addition to the current through the quantum dot(s). This material system therefore, will allow a larger current to flow compared to the silicon/silicon dioxide system. The emitter to collector current is likely to be linear at high temperature, and would be expected to overwhelm the nonlinear features caused by the tunneling of electrons though the discrete state in the dot(s), making the system unsuitable for high temperature applications. We hope this paper will stimulate related experiments and further theoretical analysis for both silicon/silicon dioxide and III/V systems.

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