Stimulated-Dielectric-Relaxation Currents in Thin Film Al-CeF_3-Al Samples*

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A new technique, based on stimulated-dielectric-relaxation currents (SDRC), has been successfully used to analyze the defect properties of the Al-CeF_3-Al capacitor system. The SDRC technique consists of cooling the system, with a voltage bias V_d applied to the sample electrodes. The voltage bias is then changed to, say, V_i, while the sample is at the low temperature, and the current-temperature (I-T) characteristics are measured while the sample is being heated at a uniform rate. When $V_d \neq V_i$, the system is in the non-steady-state, and pronounced structure is observed in the I-T characteristics. Depending on the relative magnitudes of V_d and V_i, the I-T characteristic exhibits either a single peak or two peaks, and the current can be either positive or negative, or negative at low temperatures and then positive at higher temperatures. However, when $V_d = V_i$, the system is in the steady state at all times, and no such structure in I-T curves is observed. All the measurements are explained on the basis of the SDRC theory presented in the previous papers; in fact, all the salient features of the SDRC theory have been observed. The SDRC characteristics are related to the properties of the system, such as, the trap depth, trapping density, and barrier heights, all of which have been determined. The interfacial barrier heights at the two interfaces are determined to be about 1 eV at the lower electrode and 0.95 eV at the counter electrode. The trap depth and trap density are found to be about 0.68 eV and 3×10^{20} cm^{-3}, respectively. The energy spread of the occupied trap level is about 1.9×10^{-2} eV. It is also found that an electrode-limited–to–bulk-limited transition in the conduction process occurs in these samples at about 3 V. Previous measurements on thin-film insulators are discussed in light of the present observations and other (unpublished) data obtained by the authors. It is concluded that the analyses of previous data should be viewed with caution.

I. INTRODUCTION

Up until recently[1–10] the possibility of Schottky barriers existing at the metal-insulator interfaces has usually been ignored, yet on theoretical grounds the existence of such barriers is highly probable.[6,7] It has been demonstrated experimentally that Schottky barriers in thin-film metal-insulator-metal (MIM) systems have a profound effect on the ac properties[2,4] of such systems. Also, it can be shown on theoretical grounds that the barriers will have a profound influence on the dc properties on MIM systems.[1,11,12] The two preceding[11,12] papers show that the barriers not only influence the electric field in MIM systems, but also that they are the seat of non-steady-state phenomena in such systems. The object of this paper is to study the non-steady-state phenomena in Al-CeF_3-Al MIM systems, and thus to determine information on the defect properties of the insulator CeF_3.

II. EXPERIMENTAL TECHNIQUES

A. Sample Fabrication

The samples were fabricated on a glass substrate by vacuum deposition of successive layers of aluminum, cerous fluoride (CeF_3), and aluminum. The deposition was made at a pressure less than 10^{-5} Torr. The first electrode (lower electrode; see inset in Fig. 1) was deposited in the form of a strip $1\frac{3}{4}$ in. long and $\frac{1}{8}$ in. wide. The cerous flouride was then deposited at a rate of about 8 Å sec^{-1}. Finally, the counter electrodes were deposited perpendicular to the lower electrode, in the form of strips $\frac{1}{8}$ in. wide and $\frac{1}{2}$ in. long, so as to produce 12 Al-CeF_3-Al capacitors on the substrate. The devices were completed without breaking the vacuum at any time. The thickness of the electrodes were about 1000 Å, and the thickness of the CeF_3 ranged locally, in steps, from 1800 to 4900 Å on the substrate.

B. SDRC Measurements

The experimental procedure consisted of applying a voltage V_d at a high temperature (> 340 °K) for 30 min, thus ensuring that the sample was in the steady state. The sample was then cooled to low temperature, T_0 (≤ 150 °K), in the steady-state condition. At this low temperature the voltage bias was changed to some new value V_i ($V_i \neq V_d$), then the temperature of the sample was raised at a uniform rate, that is,

$$T = T_0 + Bt,$$

where B is the heating rate (°K/sec), and t is the time (sec).

During the heating process the sample current was measured using a Keithley (610 C) electrometer, and the temperature of the sample was monitored with a thermocouple. The current and ther-

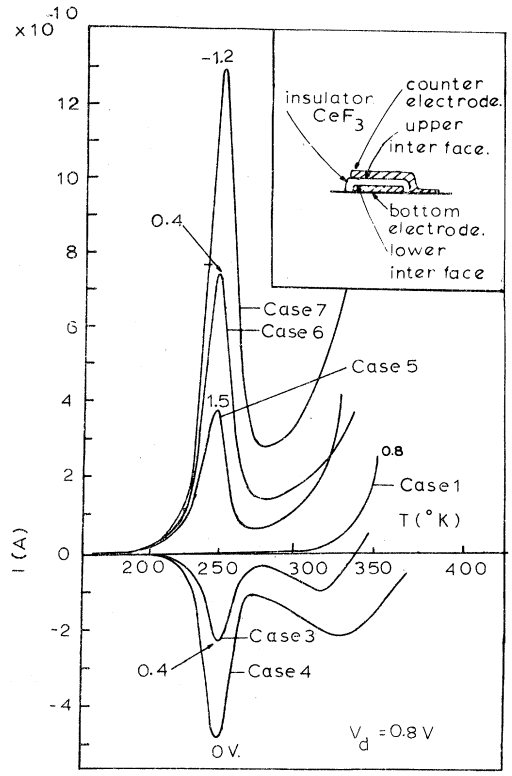

FIG. 1. General family of I-T characteristics for various constant values of V_i and $V_d = 0.8$ V. In this case the counter electrode was positive. The cases marked along side the curve are described individually in the text. Inset shows a schematic diagram of the physical structure of the sample.

mocouple voltage were plotted continuously and automatically by feeding the electrometer output and thermocouple voltage to the Y-axis input and X-axis input, respectively, of a Moseley (7001 AM) X-Y recorder. In order to minimize deleterious ambient effects, the measurements were made under vacuum ($\simeq 10^{-3}$ Torr).

III. PRELIMINARY REMARKS

Throughout the paper we will assume that the current in the insulator is carried by electrons. Also, when the electrons are flowing from the negatively biased electrode to the positively biased electrode, we say that the current is positive; which is, of course, the definition of conventional current flow. When electrons flow from the positively biased electrode to the negatively biased electrode, as indeed it often does, we say the current is negative.

All the I-T curves shown were obtained while the sample was being heated, and the heating rate B was 0.1 °K/sec unless specifically stated otherwise. Also, the counter electrode was positively biased unless otherwise specified.

IV. EXPERIMENTAL RESULTS

It is necessary to study specific voltage ranges of the parameters V_d and V_i in order to make a systematic analysis of the characteristics; that is, the characteristics have to be studied piecemeal, because the conduction process in the various voltage ranges are quite distinctive and therefore quite impossible to discuss generally. However, for the readers reference we begin this section by presenting a complete set of characteristics, solely for illustrating their general features and their relative variation in terms of the magnitudes of V_i and V_d.

A. General Nature of the Characteristics

Figure 1 illustrates a typical family of I-T characteristics for various values of V_i. In all cases during cooling the voltage V_d applied was 0.8 V and the counter electrode was positively biased. Generally speaking for a given ratio of V_i/V_d the effect on the characteristics of varying V_d was simply that their structure was enhanced for increasing V_d and attenuated for decreasing V_d.

The curves in Fig. 2 correspond to those shown

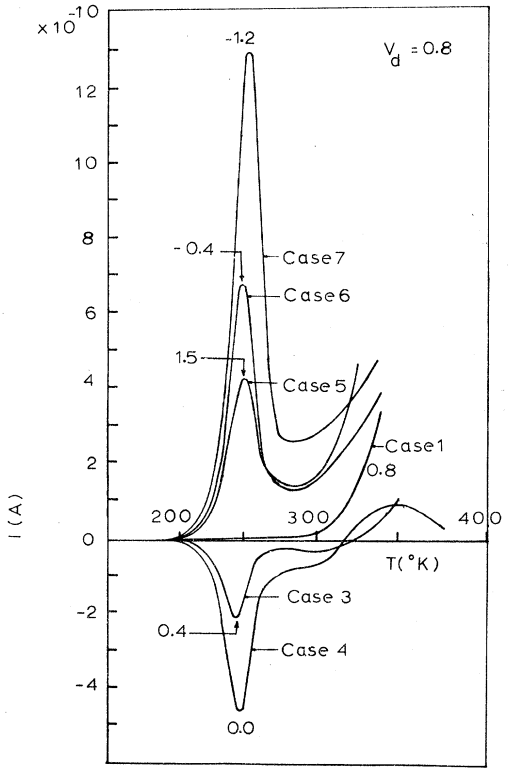

FIG. 2. General family of I-T characteristics for various constant values of V_i and $V_d = 0.8$ V. In this case the counter electrode was negatively biased. See Fig. 1 for remarks concerning case markings.

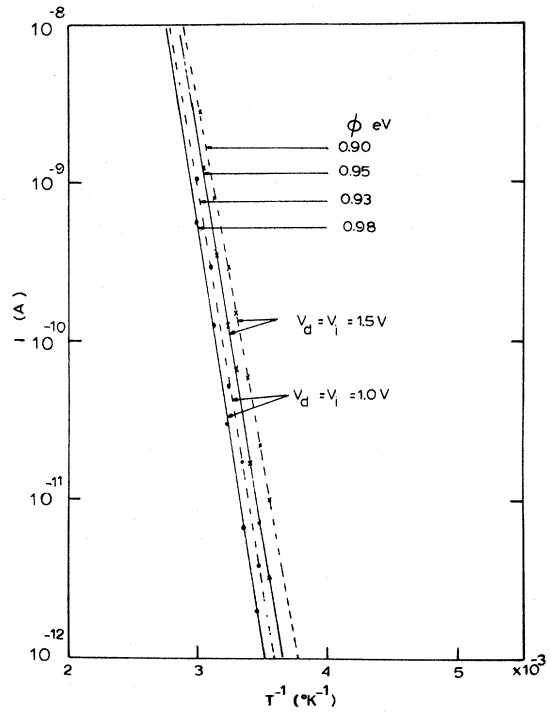

FIG. 3. Steady-state $\log_{10} I$ vs T^{-1} characteristics for two voltage biases.

in Fig. 1 except that the polarities of the voltage biases were reversed.

B. Case 1: Steady-State Characteristics $V_i = V_d$

The curves shown in Fig. 3 were obtained with the same voltage applied during cooling and heating, that is, $V_d = V_i$; thus, these curves are the steady-state characteristics. The solid curves were obtained with the counter electrode positively biased and the dotted curves with the counter electrode negatively biased. The voltage bias used during the measurements is stated along side the curves.

C. Case 2: $V_i > 0$, $V_d = 0$

Figure 4 illustrates the $I = T$ characteristics for various constant values of V_i (0.4 to 1.5 V); in this case the electrodes were short circuited during cooling. These curves exhibit a single maximum at a temperature $T_m \simeq 250$ °K. The magnitude of the maximum current is seen to be greater the greater V_i, and the half-width of *all* the peaks is approximately 30 °K. Above about 290 °K the current increases monotonically with increasing temperature.

The curve corresponding to $V_i = 1.5$ V in Fig. 4 is shown replotted in the form $\log_{10} I$ vs T^{-1} in Fig. 5. At temperature below T_m this curve has a well-defined activation energy of magnitude 0.68 eV.

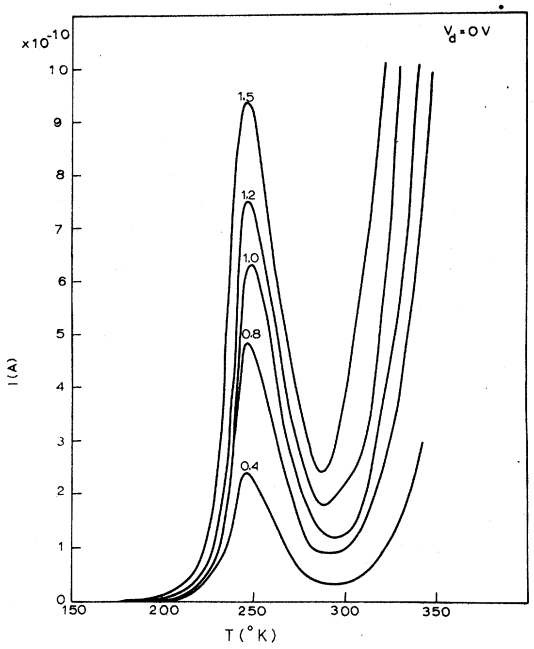

FIG. 4. Family of I-T curves (case 2) for various values of V_i and $V_d = 0$, and a heating rate $B = 0.1$ °K/sec.

Above about 300 °K the curve again manifests a well-defined activation energy, but in this case its magnitude is 0.95 eV. The dot-dashed line

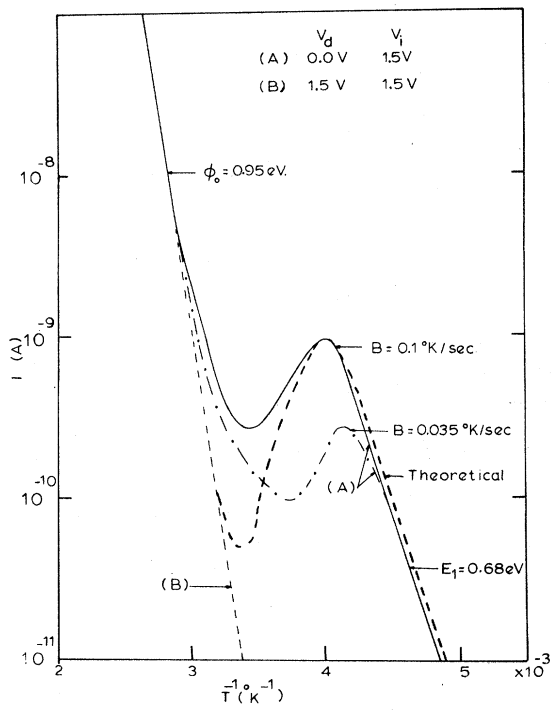

FIG. 5. Plot of $\log_{10} I$ vs T^{-1} (case 2) for $V_i = 1.5$ V and $V_d = 0$ for two different heating rates.

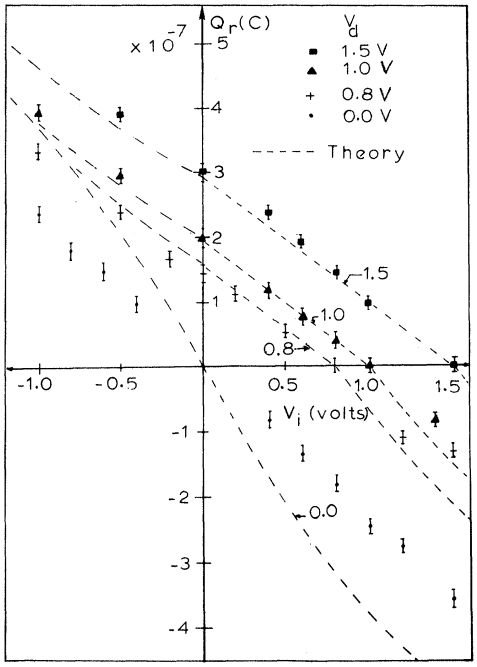

FIG. 6. Family of Q_r-vs-V_i characteristics for various constant values of V_d.

shown in Fig. 5 was obtained under identical experimental conditions as was the solid line except that the heating rate ($B = 0.035$ °K/sec) was lower.

Repeating the above experiments but with the voltage polarity of V_i reversed (i.e., with the counter electrode negatively biased) resulted in essentially identical I-T characteristics as those described above.

The magnitude Q_r of the charge released from the insulator during the relaxation process was obtained by measuring the area[12] under the peak of the curve shown in Fig. 4 and is shown plotted as a function of V_i in the second and fourth quadrant of the graph shown in Fig. 6.

D. Case 3: $V_i > V_d > 0$

The curve illustrated by the solid line in the upper-half of Fig. 7 is the I-T characteristics for the particular case $V_d = 0.5$ V and $V_i = 1.0$ V. This characteristic was found to be typical for all values of V_d and V_i within the specified range.

The dotted curve in the upper-half of Fig. 7 was obtained under the same experimental conditions as was the solid curve except for the polarity of the counterelectrode, which was negative.

E. Case 4: $V_i = 0$, $V_d > 0$

When the system is heated with the electrode short circuited ($V_i = 0$), the current flowing in the system is purely a stimulated-dielectric-relaxation current (SDRC) in origin. Figure 8 illustrates the characteristics[13] for several values of V_d. The significant feature of the characteristics in Fig. 8 compared to those described in the previous sections is the appearance of the second maximum at high temperatures. At about 400 °K the current is essentially zero, apart from a small spurious steady-state background current whose origin is unidentified as yet.

The charge Q_r corresponding to the low-temperature peaks is shown plotted as a function of V_d in Fig. 9.

Repeating the above-mentioned experiments but with the counter electrode negatively biased during cooling resulted in a similar set of curves[13] typical of those shown by the two full lines in Fig. 10; note that these two curves were taken at different heating rates.

It is seen that the effect of decreasing the heating rate B is to reduce the current levels and shift the current maxima to lower temperatures. Although the area of the peaks reduces with decreasing magnitude of heating rates B, it was found that the product of the area and B^{-1} was constant.

F. Case 5: $0 < V_i < V_d$

Figure 11 illustrates a family of I-T characteristics for several different V_i and constant V_d (= 1.5 V). In this case the size of this peak actual-

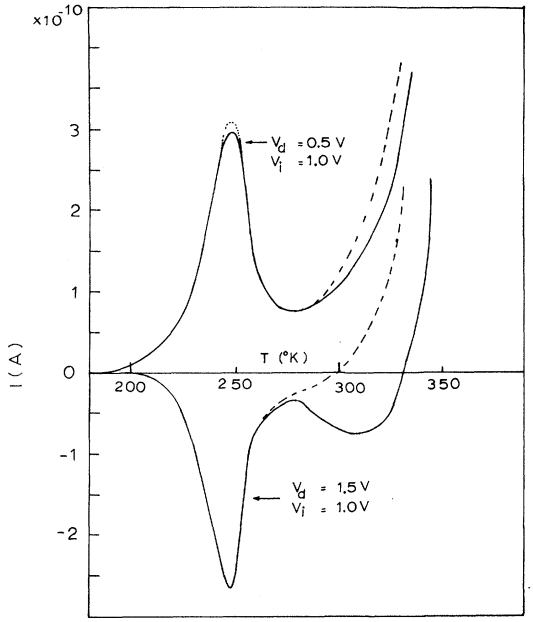

FIG. 7. Upper curves show I-T characteristics for $V_d = 0.5$ V and $V_i = 1.0$ V (case 3). The lower curves show I-T characteristics for $V_d = 1.5$ and $V_i = 1.0$ (case 5). The solid curves are counter electrode positively biased and dashed curves are counter electrode negatively biased.

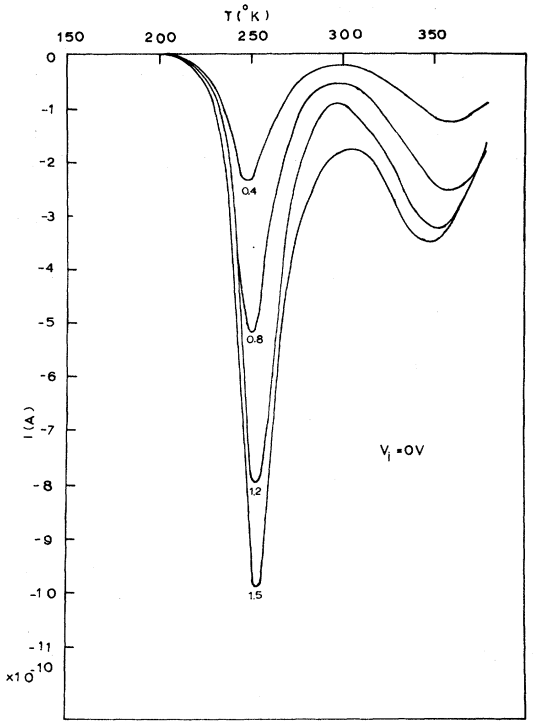

FIG. 8. Current-vs-temperature (case 4) characteristics (Ref. 13) for $V_i = 0$ and different values of V_d.

ly decreases with increasing V_i, whereas in the previous cases the converse was true. At sufficiently high temperatures, the current actually

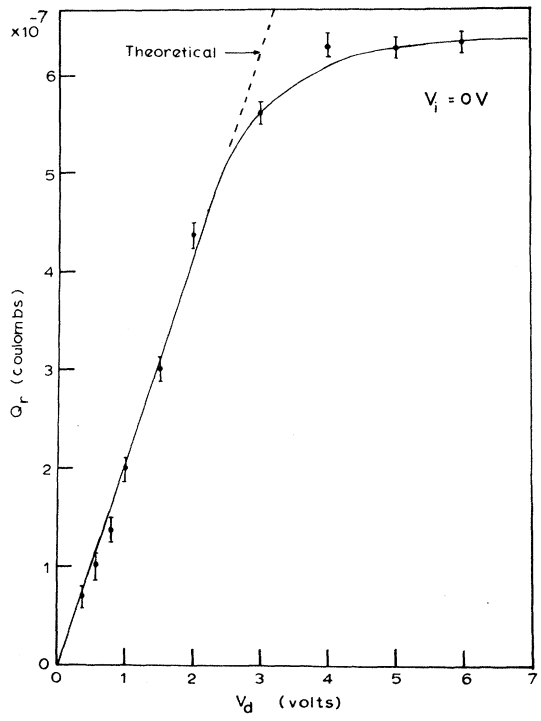

FIG. 9. Q_r vs V_d for $V_i = 0$ (case 4).

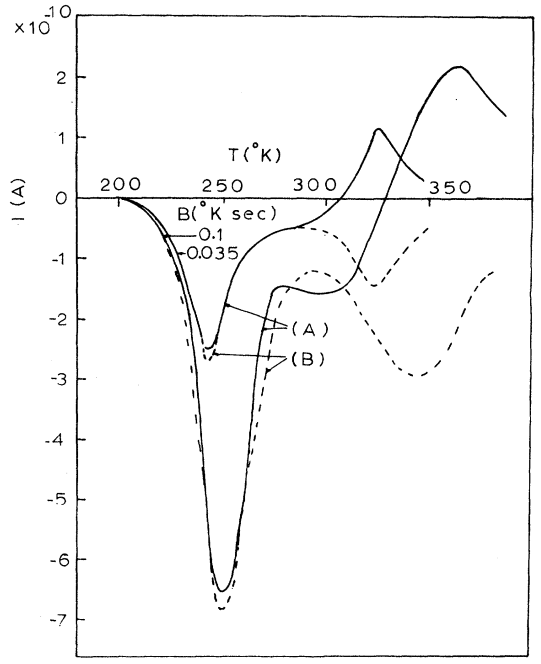

FIG. 10. I-T characteristics (Ref. 13) for $V_i = 0$ and $V_d = 1.0$ V for two different heating rates. Solid curves correspond to counter electrode negatively biased and dashed curves correspond to counter electrode positively biased. (The dashed curve for $B = 0.1$ has been taken directly from Fig. 9).

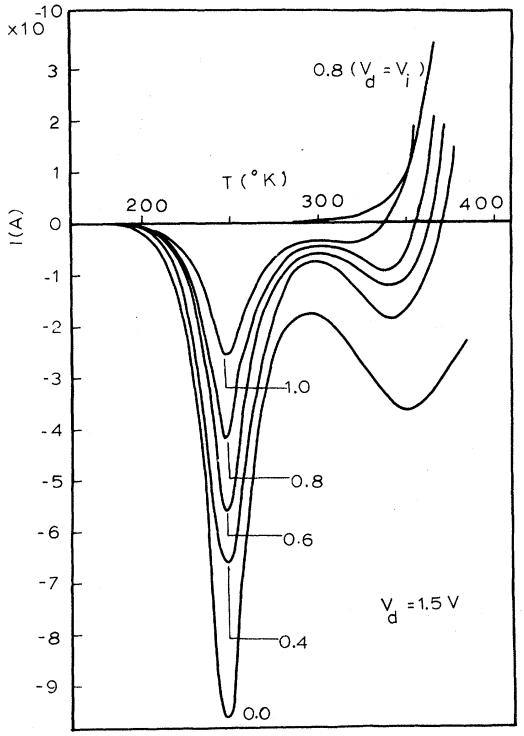

FIG. 11. Family of I-T characteristics (case 5) for $V_d = 1.5$ and various values of V_i.

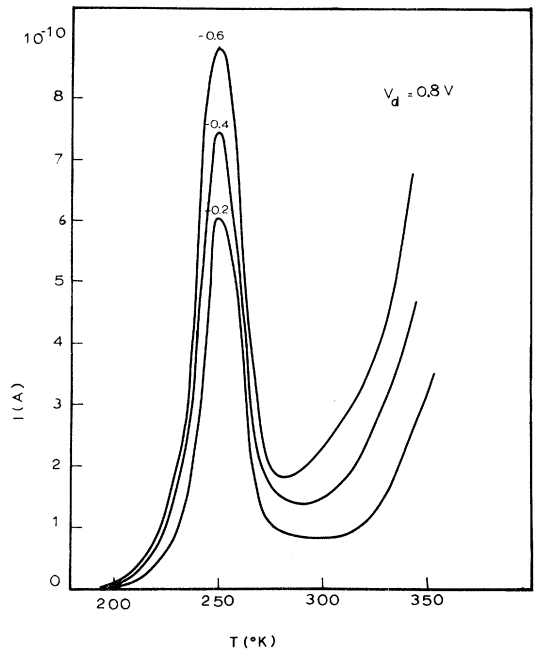

FIG. 12. Family of I-T characteristics for case 6.

changes from negative to positive, and its activation energy in this range is found to be consistent ($\simeq 0.95$ eV) with the steady-state activation energy for the corresponding polarity and magnitude of V_i. Furthermore, the characteristic corresponding to the positive current actually shifts to higher current levels with increasing V_i, which is contrary to that corresponding to negative currents.

Repeating the above experiment with the polarity of bias reversed resulted in a similar set of curves. In the lower-half of Fig. 7 we have shown I-T characteristics for this case for $V_d = 1.5$ V and $V_i = 1.0$ V. The solid curve in this case corresponds to the counter electrode being positively biased, and the dashed curve corresponds to the counter electrode being negatively biased.

The charge Q_r corresponding to the low-temperature peaks shown in Figs. 11 is plotted as a function of V_i in the upper-half of Fig. 6.

G. Case 6: $0 < |V_i| < V_d$, $V_i < 0$

Figure 12 shows a family of curves obtained for various values of V_i using $V_d = 0.8$ V. In this case the current is *always* positive, and the characteristic manifests a single peak, the maximum of which occurs at approximately the same temperature ($\simeq 250$ °K) as observed in the previous cases. Also, the area of the peak increases with increasing V_i.

Repeating the above experiment with the polarity of the voltage bias reversed results in essentially identical characteristics to those shown in Fig. 12.

The charge Q_r associated with the current peak is plotted as a function of V_i, with V_d as a parametric variable, in the upper-half of the graph shown in Fig. 6.

H. Case 7: $0 < V_d < |V_i|$, $V_i < 0$

Figure 13 shows a family of I-T characteristics for various V_i and $V_d = 0.8$ V. The characteristics are essentially the same as those described in case 6, but the current levels are higher. Repeating the above experiment with the polarity of bias reversed yields essentially similar characteristics, The charge Q_r associated with the peaks described above is shown plotted in the second quadrant in Fig. 6.

V. DISCUSSION

Apart from the pronounced structure in the curves reported here, there are four particularly outstanding features that characterize these measurements.

First, *negative* current is observed to flow in the system (case 5), and current flows under *zero-bias* conditions (case 4).

Second, the charge released during the relaxation process is much greater than can be accounted for from geometrical capacitance or injected space-charge capacitance considerations. For example, the charge released corresponding

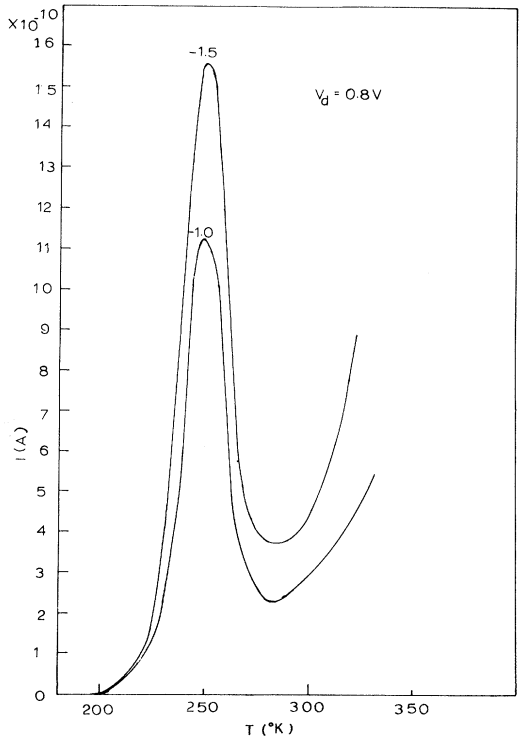

FIG. 13. Family of I-T characteristics for case 7.

to the curve obtained for $V_i = 1$ V, $V_d = 0$ (see case 2 and Fig. 6) is approximately 2.4×10^{-7} C. Now, the geometric capacitance of the sample is 5.1 nF; thus, the displacement charge, $Q_d = V$ C, for $V = 1$ V is 5.1×10^{-9} C, which is about 50 *times* smaller than that observed.

Third, the characteristics are a strong function of previous voltage (V_d) history and voltage polarity during heating (but are quite reproducible under the same experimental conditions). For example, note the striking contrast between the curves shown in Fig 7, in which cases *the voltage applied during heating was identical*. The source of the disparity in these curves lies in the fact that V_d was not the same in all cases; it was 0.5 V in the case of the positive current curves and 1.5 V in the case of negative current curves. (The solid curves correspond to the counterelectrode being positively biased and the dashed curves correspond to the counterelectrode being negatively biased.) The distinctive features of the curves are apparent down to the smallest incremental changes $|V_i - V_d|$, and provided that $V_i \neq V_d$ the characteristics are a strong function of the heating rate (see Fig. 10). In view of these observations an equally important observation is that for $V_i = V_d$ there is no maxima or minima in the characteristics, and the characteristics are independent of the heating rate.

Finally, all the results presented here were essentially independent of the thickness of the samples (the samples investigated range in thickness from 1800 to 4900 Å). *This result is particularly important in that it implies that the phenomena is associated with the contacts.*

All the manifold features can be adequately accounted for by the SDRC theory of Simmons and Taylor assuming that Schottky barriers exist at the Al-CeF_3 interfaces. Thus, our object throughout the rest of this section is twofold. First, we will be concerned with a point by point analyses of the characteristics in terms of the SDRC theory. Second, we will make a quantitative determination of the energy diagram and the defect parameters of the system.

In order to avoid unnecessary repetition of the physical processes responsible for the observed phenomena, we refer the reader to the two preceding theoretical papers.[11,12]

A. Case 1: $V_i = V_d$

In this case, since the sample is in the steady state and since the conduction process is electrode limited, the activation energies associated with the $\log_{10} I$ vs T^{-1} characteristics shown in Fig. 3 must reflect the height of the interfacial barriers. Hence, we conclude from these curves that for $V_i = 1.5$ V the barrier height at the lower electrode is 0.95 eV and that at the counter electrode it is 0.90 eV. Also, the current is given by the Richardson–Schottky equation[14] for a Schottky contact:

$$J_{RS} = A^* T^2 e^{-(\phi_0 - \Delta\phi)/kT} , \quad (1)$$

where A^* is a constant, ϕ_0 is the zero-field barrier height at the contact, and $\Delta\phi$ is the lowering of the cathodic barrier owing to the Schottky effect. From the curves in Fig. 3 we have found A^* to be approximately 36 A(cm °K)$^{-2}$. This value is in reasonable agreement with the theoretical value of 120. More significant, however, is the fact that the observed values of A^* are usually equal to about one-third of the theoretical value,[15] as our value is, and as such is further indication that the conduction process is electrode limited.

B. Case 2: $V_d = 0$, $V_i > 0$

a. Conduction processes. The I-T characteristics shown in Fig. 4 can be explained with the aid of Figs. 14(a)–14(c). (Note that in all energy diagrams the left-hand side electrode represents the lower electrode and right-hand side electrode represents the counter electrode.) According to Figs. 14(b) and 14(c), the nonsteady state current should be positive, as is observed, and reflects the defect properties of the depletion region at the lower electrode.

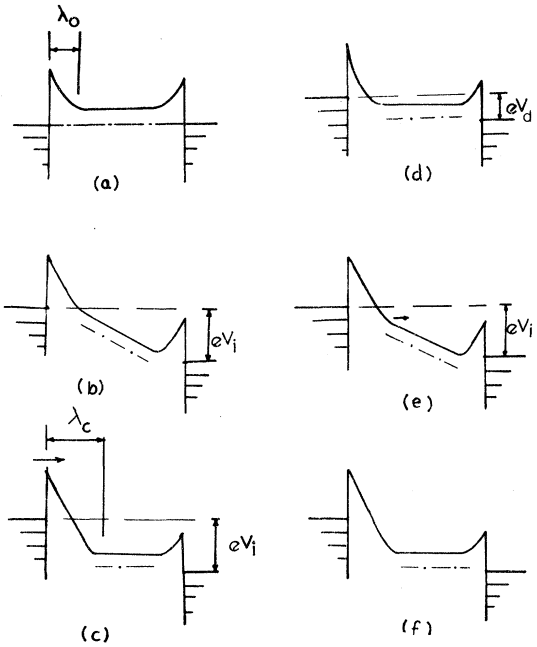

FIG. 14. Energy diagram for the system for $V_d = 0$, $V_i > 0$ (case 2): (a) in equilibrium; (b) just after applying the voltage (V_i) at low temperature at the start of heating process; (c) in the steady state. Energy diagram of the system for $V_i > V_d > 0$ (case 3): (d) during cooling; (e) at the start of the heating process; (f) in the steady state.

Because of the symmetrical nature of the problem, it is evident that when the counter electrode is negatively biased during heating, the I-T characteristics reflect the properties of the depletion region at the interface of the counter-electrode contact. Hence, because of the almost identical nature of the experimental SDRC for both polarities of bias (Sec. IV C) we conclude that the defect properties at both interfaces are essentially identical.

b. Quantitative analyses of the characteristics. The theoretical I-T characteristic for the entire temperature range is given by

$$I(T) = A(J_{\mathrm{SDRC}} + J_{\mathrm{RS}}) \ , \tag{2}$$

where J_{SDRC} is the SDRC which originates in the cathodic depletion region (CDR) and A is the area of the sample.

For a discrete trapping level[12]

$$J_{\mathrm{SDRC}} = q\lambda_c N_t e_n e^{-e_n kT^2/B(E_1+kT)} \ , \tag{3}$$

$$e_n = \nu e^{-(E_1-\beta F_t^{1/2})/kT} \ , \tag{4}$$

where q is the unit of electronic charge, N_t is trap density, E_1 is the trap depth below the bottom of the conduction band, λ_c is the steady-state depletion width, ν is attempt-to-escape frequency, F_t is the field in the interior of the insulator. In (4) β is the Poole–Frenkel coefficient given by

$$\beta = (q^3/\pi\epsilon)^{1/2} \ , \tag{5}$$

where ϵ is permittivity of the insulator. For $T < T_m$, (3) reduces to

$$J_{\mathrm{SDRC}} = q\lambda_c N_t \nu e^{-(E_1-\beta F_t^{1/2})/kT} \ , \tag{6}$$

and F_t is essentially constant [see Fig. 14(b)] and given by

$$F_t \simeq V_t/L \quad (V_d = 0, \ T < T_m) \ , \tag{7}$$

where L is the insulator thickness. Also, J_{SDRC} is normally much greater than J_{RS}.[12] Consequently, it follows that

$$I(t) = q\lambda_c \nu N_t e^{-(E_1-\beta(V_t/L)^{1/2})/kT} \quad (V_d = 0, \ T < T_m) , \tag{8}$$

which shows that $\log_{10} I$ is proportional to T^{-1} when $T < T_m$, as is observed in Fig. 5. Hence, we conclude from (8) and the activation energy associated with the low-temperature portion of the curve in Fig. 5 that

$$E_1 - \beta F_t^{1/2} = 0.61 \text{ eV} \ . \tag{9}$$

Since in this case $F_t \simeq 8.4\times 10^4$ V/cm, then

$$E_1 = 0.68 \text{ eV} \ . \tag{10}$$

At sufficiently high temperatures above T_m it will be apparent from (2) and Fig. 14(c) that the system will be in the steady state, that is, $I(T) = I_{\mathrm{SR}}$.

The value of E_1 expressed by (10) is predicated on the assumption that the trap level being essentially discrete. To test whether or not this is true, we substitute (9) into (3) and generate the complete theoretical I-T characteristic, and then compare the theoretical characteristic with the experimental characteristic. The result of this procedure is illustrated in Fig. 5. In Fig. 5 the dashed curve is the theoretical curve, which has been judiciously translated along the current axis (there was no translational adjustment made along T^{-1} axis) so that its maximum coincides with that of the experimental curve. The close correlation of the two curves implies that the trap level is almost discrete.

Additional information can be obtained from the experimental curve shown in Fig. 5 by recognizing that the SDRC must be equal in magnitude to that of the current flowing in the uniform-field region of the interior of the system. In the interior the I-T relationship may be expressed in the alternative form

$$I_{\mathrm{SDRC}} = q\mu N_c F_t A e^{-(E_1-\beta F_t^{1/2})/kT} \ , \tag{11}$$

which from (7) may be written as

$$I(T) = q\mu N_c (V_t/L) A e^{[-(E_1-\beta(V_t/L)^{1/2})/kT]} \quad (T < T_m, \ V_d = 0) \ , \tag{12}$$

where N_c is the effective density of states in the conduction band of the insulator and μ is the electron mobility. Thus, from the linear portion ($T < T_m$) of the experimental curve shown in Fig. 5, the product $N_c\mu$ is determined to be $N_c\mu \simeq 10^{15}$ (cm V sec)$^{-1}$.

C. Case 3: $V_t > V_d > 0$

The energy diagrams in Figs. 14(d)–14(f) represent this case. According to Figs. 14(e) and 14(f) the SDRC and the steady-state current ($V = V_t$) are positive, which conclusion is in agreement with the experimental observation (Fig. 7). Using similar arguments to those given in Sec. V B it will be apparent that the theoretical SDRC characteristics for this case are similar to those described above. However, for the case in hand the peak height and the area under the curve will be smaller for the same value of V_t. The reason for this is the following: The area under the DRC peak is proportional to the charge removed from the cathodic depletion region (CDR) as the sample relaxes from non-steady-state to the steady state. From a comparison of the energy diagrams in Fig. 14(a)–14(c) and 14(d)–14(f), it will be apparent that for a given V_t the charge removed from the insulator when $V_d > 0$ is always less than when $V_d = 0$.

It will be clear from the symmetrical nature of

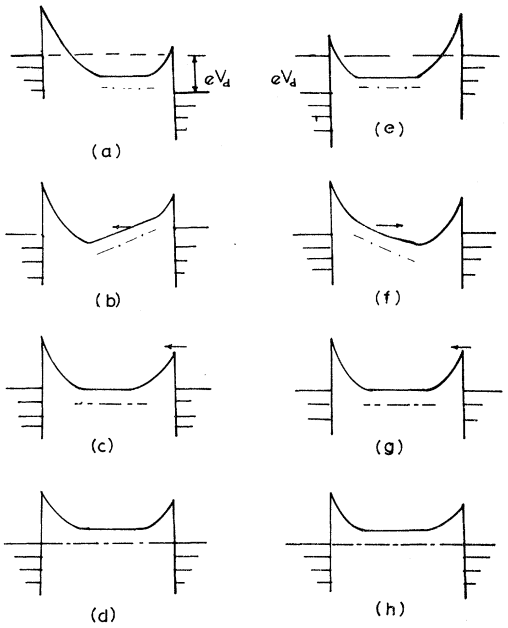

FIG. 15. Energy diagrams of the system for $V_d > 0$, $V_i = 0$ (case 4): (a) in steady state; (b) at low temperature just before heating; (c) in the quasi-steady-state; and (d) in equilibrium. (a)–(d) correspond to the counter electrode positively biased, while (e)–(h) correspond to the counter electrode negatively biased.

the problem that the same arguments are valid for the opposite polarity of bias. All the above conclusions are in agreement with observation.

D. Case 4: $V_i = 0$, $V_d > 0$

a. Counter electrode positively biased. The energy diagrams in Fig. 15 explain the *I-T* characteristics for this case. This case is distinguished from the previous two cases by the fact that the system relaxes to the quasi-steady-state before finally relaxing to steady state. Thus the lower-temperature peak is associated with the relaxation of the system from the non-steady-state to the quasi-steady-state. It is evident from Fig. 15(b) that during this process a current must flow, even though the electrodes are short circuited, and it is negative[13] with respect to the original voltage bias (V_d); this is in agreement with the experimental results (Fig. 8). Furthermore, the SDRC peak is associated with the growth of the depletion region at the counter electrode and, thus, reflects the defect properties of this region. Hence, the shape of the lower-temperature peak should be similar to those described under cases 2 and 3 (Secs. VB and VC) when the counter electrode is *negatively* biased. This conclusion is confirmed experimentally.

In relaxing to the quasi-steady-state, the total excess positive charge in the system remains constant, but is redistributed between both depletion regions. The charge Q_r that circulates the external circuit as a consequence of this redistribution of charge is given by[11,12]

$$\Delta Q = Q_r = \left(\frac{q\epsilon N_i}{2}\right)^{1/2} \frac{A\,|V_d - V_i|}{(V_d + \Delta\psi_1)^{1/2} + \Delta\psi_2^{1/2}} \quad , \qquad (13)$$

where $\Delta\psi_1 = (\psi_{m1} - \psi_i)/e$ and $\Delta\psi_2 = (\psi_{m2} - \psi_i)/e$, and ψ_{m1} and ψ_{m2} are the work functions of the lower electrode and counter electrode, respectively, and and ψ_i is the insulator work function. Thus, in this case, the smaller V_d is, the smaller is Q_r and, hence, the smaller the area under the low-temperature peak, which prediction is observed experimentally (Fig. 8).

The higher-temperature peak in Fig. 8 is associated with the relaxation of the system from the quasi-steady-state to equilibrium [Figs. 15(c) and 15(d)]. In this case electrons are injected from the electrodes into the insulator. If the barrier height at the two interfaces were identical, then the two currents at the contacts associated with this process would be equal and opposite, and there would be zero current flow in the external circuit. However, we deduced from the experimental results in Fig. 3 that the barrier height at the counter electrode is smaller than that at the lower electrode. Hence, in relaxing to the steady state a greater neutralizing current flows across the counter-electrode interface resulting in a net *negative*[13] current in the external circuit. In this case, the resulting *I-T* characteristics reflect the properties of the barrier at the *counter-electrode* interface. Also, it will be apparent from Fig. 15 (b) and 15(c) that the current flows in the same direction[13] as that associated with the low-temperature peak, as is observed experimentally (Fig. 8).

The SDRC continues to flow until the excess charge in the insulator has been neutralized, after which the system is in the steady state. It should be noted, however, that the charge associated with the high-temperature peak is equal to that required to neutralize only the excess positive charge in the lower-electrode depletion region,[16] which amounts to about half the total excess charge in the insulator. What this means is that the area under the high-temperature peak should be approximately equal to the area of the low-temperature peak. Thus, it decreases in size with decreasing V_d; this prediction is in agreement with observation (see Fig. 8).

b. Counter electrode negatively biased. Figures 15(e) – 15 (h) illustrate the energy diagrams when the polarity of the voltage bias is the reverse of that discussed above. Here again it will be apparent that as the sample is heated, it relaxes first to the quasi-steady-state [Fig. 15(g)] and then to

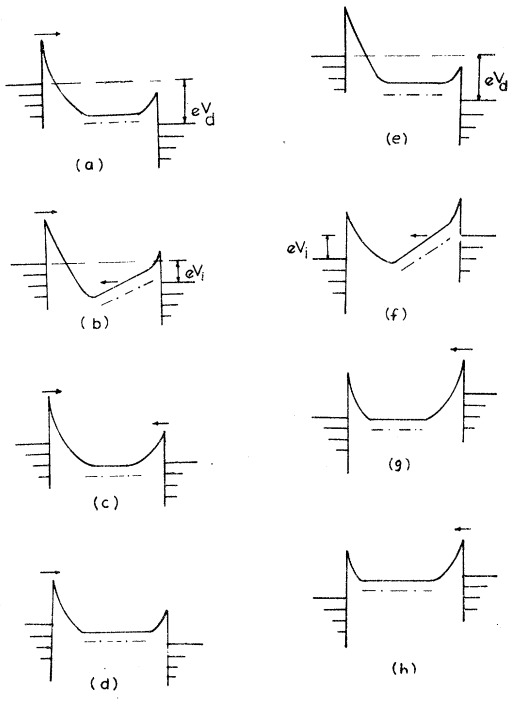

FIG. 16. Energy diagram of the system for $0 < V_i < V_d$ (case 5) when the counter electrode is positively biased: (a) in the steady state; (b) at low temperature just before heating; (c) in the quasi-steady-state; (d) in steady state. Energy diagrams $0 < |V_i| < V_d$, $V_i < 0$ (case 6): (e) in steady state; (f) before the starting of heating and changing the polarity of bias such that $|V_i| < V_d$; (g) when the system is in quasi-steady-state; (h) in steady state.

the equilbrium state [Fig. 15(h)]. It will be clear from the slope of the conduction band in the interior of the insulator [Fig. 15(f)] that as the system relaxes to quasi-steady-state the current is negative[13] with respect to the original voltage bias (V_d), as is observed experimentally (Fig. 10). It will also be apparent from Fig. 15(f) that the quasi-steady-state is associated with the growth of the depletion region at the lower electrode.

Since the process of relaxing from the quasi-steady-state to the equilibrium state consists of the injection of electrons over the lower (counter electrode) barrier into the insulator, the current flows in the *opposite* direction to that for when the system relaxed to the quasi-steady-state. This process is responsible for the reversal of current flow associated with the solid curves (A) at the high temperatures shown in Fig. 10. Thus the marked contrast between the high-temperature characteristics (A) and (B) in Fig. 10, resulting from reversing the polarity of V_d, is simply a consequence of the fact that the barrier height at the counter electrode is slightly lower than that at the lower electrode.

E. Case 5: $0 < V_i < V_d$

a. Counter electrode positively biased. The energy diagrams corresponding to this case are shown in Figs. 16(a)–16(d). These diagrams are very similar in nature to those shown in Figs. 15(a)–15(d), except that $V_i \neq 0$. Thus, the current will be negative, and according to (13) the smaller the difference $(V_d - V_i)$ is, the smaller is Q_r and, hence, the area under the SDRC peak. Clearly, this peak reflects the defect properties of the depletion region at the counter electrode.

Again, from similar arguments given in Sec. V D, it is evident that as the system relaxes from the quasisteady state to the steady state the SDRC peak associated with this process lies on the same side of the current axis as the low-temperature peak. If the lower-electrode contact (cathodic) were perfectly blocking then, as mentioned in Sec. V D, the area of the high-temperature peak would be approximately equal to that under the low-temperature peak. However, the cathode is not perfectly blocking; hence, for $V_i > 0$ a current flows across it that is greater in magnitude the greater V_i. This is, of course, a positive current and, as such, will tend to mitigate the effect of the SDRC. Hence, the area under the high-temperature SDRC peak will always be less than its corresponding low-temperature peak. At a sufficiently high temperature, the current flowing at the cathode will exceed that flowing at the anode; *therefore the current will change from negative to positive*. All these conclusions are in agreement with experimental observation shown in Fig. 11.

b. Counter electrode negatively biased. The energy diagrams for this case are the mirror image of those in Fig. 16(a)–16(d). Using similar arguments to those given above, it is concluded that the SDRC associated with the low-temperature peak is negative; this conclusion is in agreement with observation (Fig. 7) and reflects the defect properties of the depletion region at the lower-electrode interface.

Now, we know that the lower barrier exist at the counter electrode, which, in this case, is also the cathode. Therefore, it will be apparent that the SDRC current associated with the relaxation of the system from the quasi-steady-state to the steady state is positive. Superimposed on the SDRC is the positive background current flowing across the cathode because of the applied voltage; this current increases monotonically with temperature. It can be readily shown that the composite current is such that the I-T characteristic increases *monotonically with temperature*, as observed experimentally. Thus, in this case, a second positive current peak is not observed, which fact is contrary to that when $V_i = 0$.

TABLE I. Q_{r1} and Q_{r2} vs V_d.

V_d (volts)	Q_{r1} ($V_i = 0$) (C)	Q_{r2} ($V_i = -V_d$) (C)	Q_{r2}/Q_{r1}
0.4	0.64×10^{-7}	1.23×10^{-7}	1.92
0.6	1.00×10^{-7}	2.10×10^{-7}	2.10
0.8	1.36×10^{-7}	2.72×10^{-7}	2.00
1.0	2.00×10^{-7}	3.95×10^{-7}	1.96

F. Case 6: $0 < |V_i| < V_d$, $V_i < 0$

Figures 16(e)–16(h) represents energy diagrams for this case. Clearly, SDRC is positive as the system relaxes to the quasi-steady-state; this conclusion is contrary to that for the corresponding process discussed in case 5, but in agreement with experimental observation. It will be obvious that the I-T peak reflects the defect properties of the counter-electrode depletion region. Since the lower barrier is at the counter electrode, it will be clear from Fig. 16(g) that as the system relaxes to the steady state the current will still be positive. Since in the steady state the current must be positive, it follows that the current in this case is always positive.

The effect of changing the polarity of bias from that discussed above results in the energy diagrams that are mirror image of those in Figs. 16(e)–16(h), and the conduction process is essentially the same as described above.

The above conclusions are in general agreement with the experimental results.

G. Case 7: $0 < V_d < |V_i|$, $V_i < 0$

The SDRC is always positive in this case, as observed (Fig. 13), and is associated with the growth of the depletion region at the counter electrode. Since $|V_i| > |V_d|$, the depletion region will be greater in the steady state than when the device was cooled. Thus, during the relaxation process the negative charge released from the depletion region at the cathode is more than sufficient to neutralize the excess positive charge in the lower-electrode depletion region. Hence, the system does not assume the quasi-steady-state as it relaxes to the steady state. Thus, in this case the energy diagrams are essentially the same as those shown in Figs. 16(e), 16(f), and 16(h). According to (13) the area under the SDRC peak will increase with increasing V_i, as is observed (Fig. 13). For the particular case $|V_i| = |V_d|$, the negative charge, say Q_{r2}, released from the depletion region at the counter electrode should be just sufficient to neutralize the excess positive charge in the lower-electrode depletion region. If this conclusion is correct, then Q_{r2} should be just twice Q_{r1}, where Q_{r1} is the charge transfer associated with the condition $V_d(Q_{r1}) = V_d(Q_{r2})$ but with $V_i = 0$ (see Sec. V D and Fig. 9). This is indeed the case, as shown in Table I, in which Q_{r2} and Q_{r1} and their ratio are given for various V_d.

The conduction process for the opposite polarity is essentially the same as that given above.

H. Discreteness of the Trap Level

The temperature T_m at which the peak in the SDRC occurs is related to the maximum in the trap distribution, say E_m as follows[17]:

$$E_m = T_m[1.92\times10^{-4}\log_{10}(\nu/B) + 3.2\times10^{-4}] - 0.15. \quad (14)$$

By measuring T_m for two different rates (see Fig. 11), say, B_1 and B_2, we can determine ν from (14):

$$\frac{T_{m1}}{T_{m2}} = \frac{1.92\times10^{-4}\log_{10}(\nu/B_2) + 3.2\times10^{-4}}{1.92\times10^{-4}\log_{10}(\nu/B_1) + 3.2\times10^{-4}} . \quad (15)$$

From Fig. 10 we see that for $B_1 = 0.1$ °K/sec, $T_{m1} \simeq 250$ °K and for $B_2 = 0.035$ °K/sec, $T_{m2} = 243$ °K. Substituting these values in (15), ν is calculated to be approximately 2×10^{11} sec^{-1}. Using this value of ν in (14), we find that $E_1 \simeq 0.67$ eV. This value is in good agreement with that determined in Sec. V B, which is a further indication that the spread of the trap level is relatively narrow.

The spread of the trap level can be further checked by measuring the half-width ΔT of the SDRC curves. An accurate experimental determination of ΔT can only be obtained from the zero-bias curves shown in Fig. 8 since in this case the current flowing in the system is a pure SDRC. Under voltage-bias conditions the current is composed of the internal SDRC and the background current across the cathodic contact; the latter component tends to distort the SDRC peak; in particular it slightly enhances the half-width of the peak.

The half-width of the pure SDRC low-temperature peak in Fig. 8 is found to be approximately 24 °K. Now the theoretical half-width ΔT for a discrete trap level is given by[17]

$$\Delta T = 2KT_m^2/E_1 , \quad (16)$$

where E_1 is the depth of the trap below the bottom of the conduction band. Substituting the experimentally determined values $E_1 = 0.67$ eV and $T_m = 250$ °K—see above—in (16), we find ΔT to be 17 °K. This is only 7 °K smaller than the experimental value, indicating once again that the spread of the trap level is relatively narrow. From this 7 °K disparity we can in fact estimate approximately the spread in energy δE of the level as follows. From (14) we find that[18]

$$\delta E = (1.92\times10^{-4}\log_{10}(\nu/B) + 3.2\times10^{-4})\,\delta T , \quad (17)$$

where δT is the disparity in experimental and the-

oretical half-widths. Using $\delta T = 7\,^{\circ}\mathrm{K}$, $B = 0.1\,^{\circ}\mathrm{K}/\mathrm{sec}$, and $\nu = 2\times10^{11}\ \mathrm{sec}^{-1}$ we find the energy spread of the occupied[19] portion of the trap level to be $\delta E \simeq 1.9\times10^{-2}$ eV.

I. Q_r, N_d, and Electrode-Limited-to-Bulk-Limited Process

The dotted line in Fig. 9 is the theoretical Q_r-vs-V_d characteristic for $V_i = 0$, computed using (13). The value of the trap density $N_t(3\times10^{20}\ \mathrm{cm}^{-3})$ was judiciously chosen in order to fit the experimental data for lower values of $V_d(V_d \leq 3\,\mathrm{V})$. The reason for the deviation of the theoretical curve from the experimental curve can be explained in the following manner. The theoretical Q_r-vs-V_d characteristic (13) was derived on the basis of a cathodic contact that was blocking at all values of V_d. However, when Schottky barriers exist at the contact it has been shown that at some sufficiently high voltage V_T the conduction process can undergo an electrode-limited-to-bulk-limited transition.[1] What this means as far as we are concerned, is that for voltages above V_T only a fraction of the applied voltage in excess of V_T appears across the CDR, with the result that Q_r grows less rapidly with increasing voltage above V_T than it would if the contacts were perfectly blocking. Now, it is observed in Fig. 9 that the theoretical curve begins to deviate from the experimental curve at $V_d \simeq 3\,\mathrm{V}$. Thus, this value of V_d corresponds to the threshold voltage V_T.

The dotted curves in Fig. 6 are the theoretical Q_r-V_i characteristics for various constant V_d and V_i, were generated using (13) and

$$Q_r = (2\epsilon N_t)^{1/2}\left[(\Delta\psi_1 + eV_i)^{1/2} - (\Delta\psi_1 + eV_d)^{1/2}\right] \qquad (18)$$

where appropriate, and the same parameters ($N_t = 3\times10^{20}\ \mathrm{cm}^{-3}$, $\Delta\psi = 0.95$ eV) were used here as were used earlier to generate the theoretical curve in Fig. 9. The correlation between the theory and experiment is found to be quite good, justifying the parameters used.

VI. COMMENTS ON THE ANALYSES OF THIN-FILM MEASUREMENTS

This study clearly indicates the profound effects of Schottky barriers on the electrical properties of MIM systems, yet, generally speaking, the existence of Schottky barriers in MIM systems has been ignored. Ignoring this tacitly implies two things: The first is that linear-field concepts are applicable in MIM systems. By linear-field concepts we mean that the field is uniform throughout the insulator before and after the voltage is applied. Such conditions are highly unrealistic, particularly when the insulator is defect.[6,7] The second is that the system is in the steady state and, hence, the conduction process is a steady-state process. The work presented here strongly suggests that linear-field concepts are not generally applicable and often MIM systems are not in the steady state. This conclusion is supported by the fact that all the thin-film insulators we have studied show, to some degree or the other, the effects described here. These materials include MoO_3, CeF_3, Al_2O_3, SiO, $BaTiO_3$, Si_3N_4; the effects are also observed in thin-film semiconducting glasses.

Normally, the experimental data obtained from thin-insulating films are interpreted in terms of the Poole–Frenkel effect or the Richardson–Schottky effect. These processes are strongly field dependent. Thus, if Schottky barriers exist at the interfaces, but linear-field concepts are used to interpret the data, then clearly any conclusions drawn are false. This would be the case even if the system were in the steady state, which would not necessarily be the case. In this regard, it is interesting to note that a good deal of controversy surrounds the interpretation of the experimental data obtain from MIM systems. We speculate that it is a consequence of the points highlighted above. Certainly our experience with CeF_3, MoO_3, Al_2O_3, SiO, $BaTiO_3$, and Si_3N_4 clearly shows that, in these cases, linear-field steady-state concepts are not applicable.

VII. CONCLUSIONS

We have shown that the electrical properties of Al-CeF_3-Al samples are a strong function of previous voltage history and the heating rate, and exhibit pronounced structure. These phenomena have been successfully interpreted in terms of SDRC theory; in fact, every salient prediction of the SDRC theory has been experimentally confirmed. Thus, the measurements have demonstrated incontrovertibly that Schottky barriers exist at the Al-CeF_3 interfaces. Furthermore, the measurements have permitted a determination of the defect parameters of CeF_3 (in particular it was found that $N_d = 3\times10^{20}\ \mathrm{cm}^{-3}$ and that the trap depth is 0.68 V) and the energy diagram of the system (Fig. 17).

Finally, the theoretical concept presented in the two preceding papers and the experimental investigation presented here (and those obtained

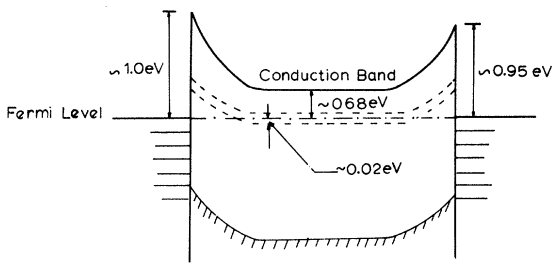

FIG. 17. Suggested energy diagram for Al-CeF_3-Al system as deduced from SDRC measurements (Ref. 19).

from the insulators mentioned above) strongly suggest that the *interpretation* of previous electrical measurements presented to date should be viewed with caution.

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[12]J. G. Simmons, and G. W. Taylor, second preceding paper, Phys. Rev. 6, 4804 (1972). In this reference and Ref. 11 the properties of the trap level were judiciously chosen such that the density of the occupied traps was $\frac{1}{2}N_t$. Here we have no *a priori* knowledge of the ratio of the occupied to unoccupied traps. Thus, in this paper we concern ourselves with only the *occupied* levels and assume that their density is N_t per unit volume. Hence, in order to obtain the equations presented here we simply substitute $2N_t$ for N_t in the corresponding equation in Refs. 11 and 12.

[13]Strictly speaking, under short-circuited conditions it is not possible to define whether a current is positive or negative. Thus, we assume that the current is positive if it flows in the same direction as the steady-state current did when the system was being cooled (with V_d applied).

[14]J. G. Simmons, Brit. J. Appl. Phys. 4, 613 (1971).

[15]See A. Van der Ziel, *Solid State Physical Electronics* (Prentice Hall, New York, 1968), p. 141; C. Kittel, *Introduction to Solid State Physics* (Wiley, New York, 1968), p. 247.

[16]Note that the contribution ΔQ to the charge circulating in the external circuit due to an increment of charge (electrons) injected into the insulator from say the counter electrode is given by $\Delta Q = \Delta Q\, x/L$, where x is the distance travelled by the electrons before they neutralize an equivalent amount of excess positive charge. Thus, the injected charge travels a distance $x \simeq L$ from the counter-electrode interface to neutralize excess positive charge in the lower-electrode depletion region but only a distance $X \ll L$ in neutralizing excess positive charge in the counter-electrode depletion region. Thus, it follows that the charge circulating the external circuit as the system relaxes to the steady state is approximately equal to that required to neutralize the excess positive charge in the lower-electrode depletion region.

[17]J. G. Simmons and G. W. Taylor, Phys. Rev. B (to be published). Note that if the trap level were discrete, then E_m would correspond to the depth E_1 of the trap below the bottom of the conduction band.

[18]The reader will probably appreciate that this procedure is intuitively correct. A rigorous treatment on the relating of the energy and temperature in this manner is given elsewhere. Furthermore, if δE turns out to be more than about $2kT_m$, then the shape of SDRC approximates that of the energy distribution of the filled traps (unpublished).

[19]We are assuming here that the Fermi level lies in the trap level, which will normally be the case (Ref. 7). Thus, we can only obtain information about the filled portion of the traps since only they contribute electrons to the SDRC. It is possible, though, that the trap level actually lies below the Fermi level, in which case δE would correspond to the total width of the trap-level band. Furthermore, in this event, Eq. (11) and the conclusions deduced from it would be invalid.