Dielectric Relaxation and Its Effect on the Isothermal Electrical Characteristics of Defect Insulators*

J. G. Simmons and G. W. Taylor
Department of Electrical Engineering, University of Toronto, Toronto, Canada
(Received 8 June 1971)

The effect is considered of dielectric relaxation on the I-V characteristics of metal-insulator-metal (MIM) systems when blocking contacts exist at the insulator surfaces. It is shown that the dielectric relaxation time (DRT) has a strong influence on the dc electrical properties of the insulator. If the DRT is short ($<10^{-3}$ sec), then the conduction mechanism measured is a steady-state process for increasing voltage bias, but for decreasing voltage bias the system exists in a quasisteady state if the insulator has good blocking contacts; this being the case, the J-V characteristics will manifest hysteresis. If the DRT is long ($>10^{4}$ sec), the conduction mechanism involved is essentially a non-steady-state process. Also, the DRT is a very sensitive function of temperature; it increases with decreasing temperature. Thus, a conduction mechanism that is a steady-state process at room temperature, may well be a non-steady-state process at low temperatures. In the MIM system under consideration, the steady-state conduction process (short DRT) is shown to be an *electrode-limited* process, while the non-steady-state measurement is a *bulk-limited* process, even though blocking contacts exist on the insulator surfaces. If the DRT is moderate ($\simeq 10^{2}$ sec), a time-dependent relaxation current is observed, from which the trap density, amongst other insulator properties, can be determined. Other non-steady-state processes, such as current reversal (i.e., current flowing in the opposite direction to conventional current) are described.

I. INTRODUCTION

Until recently[1-6] the fact that traps in an insulator can result in pronounced bending of the conduction band when a metal electrode is applied to its surface has, by and large, been neglected in experimental studies of the electrical properties of insulators. This is apparent by the fact that conduction processes through insulators are often described in terms of the conventional Schottky or Poole–Frenkel effects. Both these effects are reflected in the current (I) versus voltage (V) characteristics by the relationship

$$\ln I \propto V^{1/2} . \tag{1}$$

(Note that the term "conventional" used above also signifies that I above is a steady-state current.) This result is predicated on a conduction band that is flat and undistorted throughout the insulator (see Fig. 1) before and after the voltage is applied. Clearly, when blocking contacts exist at the electrode-insulator interface (Fig. 2) the steady-state conduction process is electrode-limited, but the I-V characteristics associated with the Schottky effect will be distinctly different from those associated with the conventional process. Furthermore, blocking contacts normally inhibit the conventional Poole–Frenkel effect, although it is observable under certain voltage conditions[1]; even then, the relationship expressed by (1) is not strictly appropriate.

It is possible for the conditions described by Fig. 1 to exist if the insulator is perfect (trap free). However, it is a fact that if localized states (traps) are distributed throughout an insulator (and this is generally thought to be the case[7,8] for real insulators, and is definitely the case for amorphous insulators[9]), then the band edges are, in general, severely distorted at the electrode-insulator interface,[4] as shown in Fig. 2 which illustrates the case for blocking contacts (Schottky barriers). If the

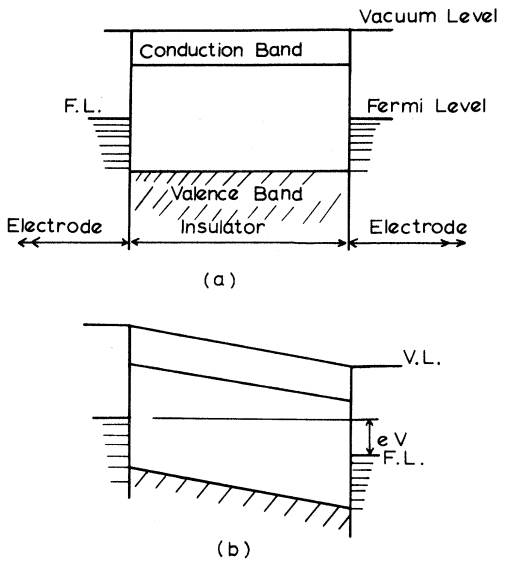

FIG. 1. Energy diagram required to observe "conventional" Poole–Frenkel or Schottky effects: (a) before voltage is applied, (b) with voltage V applied.

trap density is high, as is normally the case in the types of insulators under consideration, the depletion regions associated with the Schottky barriers may be only a few hundred angstroms or less in thickness.[5] The distinctive features of the energy diagrams [Figs. 1(a) and 2(b)] are also apparent when the systems are subjected to voltage bias [cf. Figs. 1(b) and 3(d)]. Since the system depicted by Fig. 2 has a much greater probability of existing than that corresponding to Fig. 1(b), one can conclude that the manifestation of the conventional Poole–Frenkel and Schottky effects is not very probable, except perhaps in very thin insulators (< 100 Å) where band bending due to space-charge effects is negligible. Indeed, where such apparent effects have been reported in the literature,[10–16] they have been open to question[17,18] or else shown to be inconclusive.[15–17] As a matter of fact, we will show that a non-steady-state Poole–Frenkel process may occur in insulators when Schottky barriers exist on the insulator, and hence may readily be misinterpreted as a conventional Poole–Frenkel process.

Normally, when dc measurements are made on a defective insulator and the current is observed to be apparently time-independent for a constant applied voltage, it is assumed that a steady-state conduction process is being observed. We will show here that this is not necessarily the case, even at room temperature, and in all probability not the case at low temperatures. Whether or not a conduction process is a steady-state process depends on the dielectric relaxation time (DRT) of the insulator. This parameter is strongly temperature dependent, so much so that the conduction mechanism in the insulator can be a normal steady-state process at room temperature and a non-steady-state process at low temperature. The DRT of insulators and its manifold effects on the isothermal J-V characteristics of the insulator are the kernel of this paper.

For the purposes of analyses, we have selected the simplest practical model of an insulator, but it may be regarded as a building block for more complex systems. Furthermore, we have avoided mathematical complexities that normally would add an extra degree of precision at the expense of clarity. In any event, the defect nature of practical insulators is an extrinsic property of, and very much dependent on, the previous history of the material, and as such is ill defined. Thus, for the problem at hand, mathematical exactitude is both redundant and illusory, since the resultant equations are analytically intractable. In short, the object of this paper is to provide an assimilable explanation of the dielectric relaxation effect and allied phenomena, which may be readily adapted and generalized to include any type of defect structure associated with discrete levels. It also presents a flexible analytical framework which will permit the determination of important trapping parameters for the insulator from experimental data.

It is our opinion that the simple experimental techniques suggested by the isothermal theory contained herein, together with those of the corresponding thermal theory,[19] yield the means for gleaning much relevant quantitative information on the defect structure of insulators.

II. METAL-INSULATOR-METAL SYSTEM

In the ensuing treatment we need only consider an insulator containing two trapping levels, since the solution to this problem is readily extended to an insulator containing several trapping levels.

Figure 2(a) illustrates the insulator before the electrodes are applied. The flat conduction band implies that any effects due to surface states are negligible. (Actually, for insulators containing a high density of traps, it is very doubtful that one can distinguish between surface states and bulk traps.) The insulator contains two trapping levels, the upper level containing N_t donor-type traps per unit volume and positioned at an energy E_1 below the bottom of the conduction band, and a lower level containing $\frac{1}{2}N_t$ acceptor-type traps per unit volume and positioned at an energy E_2 ($E_2 > E_1$) below the bottom of the conduction band. The insulator is thus a compensated system, the upper level having

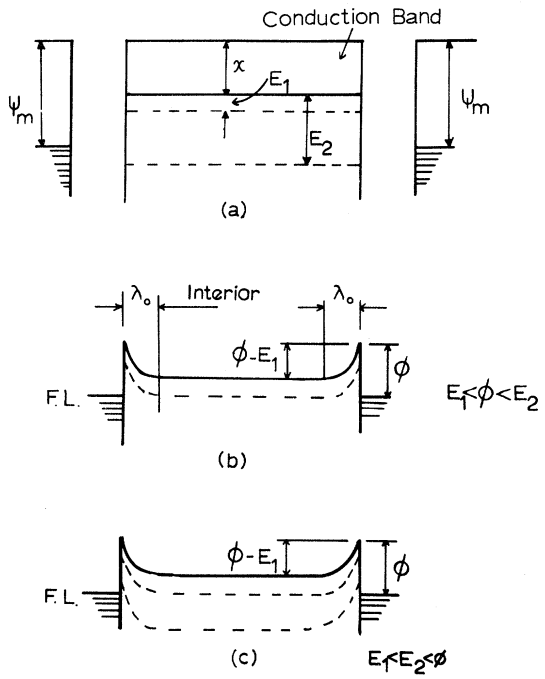

FIG. 2. Energy diagram of the type of MIM system under consideration: (a) the insulator before the electrodes are applied; (b) and (c) after electrodes are applied.

supplied $\frac{1}{2}N_t$ electrons to the lower level, thereby saturating it. The choice of this type of defect structure is simply an artifice for mathematical expediency, and in no way detracts from the generality of the problem. It also has the propitious effect of pinning the Fermi level exactly at the upper trap level at all practical temperatures[20] thus eliminating one variable and facilitating our presentation. Hence the work function of the insulator, ψ_i, which is the energy difference between the insulator vacuum level and the upper trap level [see Fig. 2(a)], is given by

$$\psi_i = \chi + E_1 .$$

Generally speaking, the electrode work function ψ_m will not be equal to ψ_i, so that when the electrodes are applied there is a transfer of charge between the electrodes and insulator, which is required to bring the system into equilibrium. If $\psi_m > \psi_i$, electrons flow out of the traps situated just inside the surface of the insulator into the electrodes, thereby lowering its potential with respect to that of the electrodes, until the insulator Fermi level lines up with that of the electrodes [Figs. 2(b) and 2(c)]. This process is identical to that which occurs when a metal electrode is applied to an n-type semiconductor, and just as a Schottky barrier is formed at the semiconductor surface, Schottky barriers[5] are formed at both surfaces of the insulator [Figs. 2(b) and 2(c)]. The interfacial barrier height in the absence of surface states is given by

$$\phi = \psi_m - \chi . \tag{2}$$

When

$$\psi_i < \psi_m < \chi + E_2 , \tag{3}$$

or[21]

$$E_1 < \phi < E_2 , \tag{4}$$

the lower trapping level is positioned below the system Fermi level after the electrodes are applied [Fig. 2(b)]; thus its occupancy remains essentially unchanged, and the upper level alone is responsible for the formation of the Schottky barriers. This being the case, the width of the Schottky barrier depletion regions λ_0 is given by the usual expression[22] (the space charge in this case is $\frac{1}{2}N_t$ per unit volume):

$$\lambda_0 = 2(\epsilon/q^2 N_t)^{1/2}(\phi - E_1)^{1/2} , \tag{5}$$

where ϵ is the permittivity of the insulator and q is the electronic charge.

The interior of the insulator is defined as the space-charge-free region existing in the insulator between the edges of the two depletion regions [Figs. 2(b) and 2(c)]. The significance of this region is that the free-carrier density is constant and equal in magnitude to the free-carrier density in the insulator before the electrodes were applied.

When

$$\psi_m > \chi + E_2 , \tag{6}$$

or if[21]

$$\phi > E_2 , \tag{7}$$

both trapping levels play a role in the formation of the Schottky barrier [Fig. 2(c)]. However, the upper trap level contributes a constant positive charge $\frac{1}{2}N_t$ throughout the entire depletion region. The lower level contributes a constant positive charge $\frac{1}{2}N_t$ over only a short region of the depletion region, namely that extending from the interface to approximately where the level intersects the system Fermi level. From this point onwards its charge contribution to the depletion region can be considered negligible, since it lies below the Fermi level and is essentially filled. The closer the lower trap level is to the upper level the greater is its over-all charge contribution (relative to the upper level) to the depletion region and, hence, the smaller is λ_0, all other parameters assumed constant. For simplicity, we will assume that (4) is satisfied, so that we can ignore the lower trap level.

III. DIELECTRIC RELAXATION

A. Physical Process

Consider a metal-insulator-metal (MIM) system containing blocking contacts [its energy diagram is illustrated in Fig. 3(a)]. Immediately after a voltage bias is applied to the system, the voltage is distributed uniformly throughout the solid, as illustrated by the straight Fermi level in Fig. 3(b). However, this is an unstable situation, since the current flowing in the interior of the insulator is greater than that flowing in the cathodic depletion region. This can be seen to be the case by an inspection of Figs. 3(b) and 3(c) and the fact that the current density $J(x)$ at any point x in the system is given by

$$J(x) = \mu n(x) q \frac{dE_F}{dx} , \tag{8}$$

where E_F is the Fermi energy of the insulator; $n(x)$ is the free-carrier density at any plane x in the insulator and is given by

$$n(x) = N_c \exp[(E_F - E_c + 2\beta F^{1/2})/kT] ;$$

μ is the electron mobility; N_c is the density of states in the insulator; E is the energy of the bottom of the conduction band; k is Boltzmann's constant; and T is the absolute temperature. The term $2\beta F^{1/2}$ is the Poole–Frenkel lowering of the trap level, F is the field at the trap,

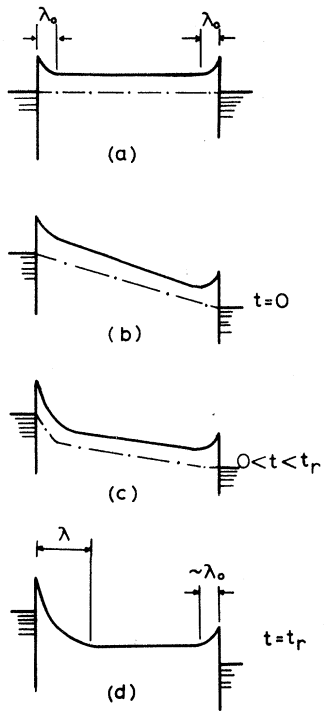

FIG. 3. Energy diagram of MIM system during various states of relaxation: (a) before bias is applied; (b) immediately after bias is applied; (c) during intermediate state of relaxation; (d) end of relaxation process. At low temperatures, state (b) prevails for all reasonable periods of time.

$$\beta = (q^3/4\pi\epsilon)^{1/2},$$

and ϵ is the permittivity of the insulator. Ultimately, after a time t_r which is the DRT, the system relaxes to the steady state described by the energy diagram in Fig. 3(d). This condition results when the current is spatially and temporally constant throughout the system.

Assuming the insulator is sandwiched between coplanar electrodes, the information necessary for determining the shape of the energy diagram as a function of time is contained in the one-dimensional Poisson's equation

$$\frac{dF}{dx} = \frac{\rho(x)}{\epsilon}$$

and the one-dimensional current continuity equation

$$\frac{dJ(x)}{dx} = \frac{d\rho(x)}{dt}, \tag{9}$$

where F and ρ are, respectively, the field and space charge at any point x in the insulator.

Except for the simple case of a uniform insulator or semiconductor, the equations are normally intractable to solution. However, with the aid of Eq. (9), Fig. 3, and physical reasoning we can determine to a good approximation how the system corresponding to the energy diagrams of Fig. 3 decays with time, as follows: From (9) the greatest rate of relaxation ($d\rho/dt$) occurs where the divergence of the current, dJ/dx, is greatest. Throughout the relaxation process, since dE_F/dx and $n(x)$ are constant in the interior of the insulator, J_i is spatially (but not temporally) constant in this region [see (8)]. Also J_i is much greater than the current at any point in the cathodic depletion region (CDR) $J_c(x)$, which will be apparent from an inspection of (8) and Figs. 3(b) and 3(c). Clearly, then, since dJ/dx has its maximum value at the edge of the CDR, the rate of charge accumulation in the CDR is equal to J, hence the width of the CDR λ_c grows during the relaxation process, as indicated in Figs. 3(b), 3(c), and 3(d). It will be noted that the cathodic Schottky barrier is reverse biased, and if V_c is that portion of the applied voltage absorbed across this barrier at any time during the relaxation period, λ_c is given approximately by

$$\lambda_c = 2(\epsilon/q^2N_t)^{1/2}(\phi - E_1 + eV_c)^{1/2}. \tag{10}$$

This barrier limits the rate of flow of electrons in the system when it is in the steady state; hence, in this case, the majority of the applied voltage is absorbed across this barrier. On the other hand, the anodic Schottky barrier is forward-biased and presents a low impedance to the electronic current flowing out of the insulator. Thus, to a first approximation, the depletion region of this barrier under voltage bias may be assumed to be equal to its zero-bias value λ_0.

B. Charge Transfer

The additional space charge accumulated in the CDR when a voltage is applied to the system is given by [see (5) and (10)]

$$Q_c = \tfrac{1}{2}eN_t(\lambda_c - \lambda_0). \tag{11}$$

The small-signal capacitance C_λ of the depletion region is, from (10) and (11),

$$C_\lambda = \frac{dQ_c}{dV} = \frac{\epsilon}{\lambda_c},$$

and the geometric capacitance C_g of the insulator is given by

$$C_g = \epsilon/L.$$

Thus, since[23] $C_\lambda \gg C_g$ (i.e., $\lambda_c \ll L$), it follows that the charge Q_c is *considerably* greater than the *displacement* charge Q_d (which is expressed as $Q_d = C_gV$) that would circulate the external circuit if the insulator were a perfect insulator.[24]

C. Dielectric Relaxation Time t_r

The rate of build up of positive charge, dQ/dt, in the CDR is equal (assuming we may neglect the

charge injected at the cathode) to the flow of current J_i, at any point in the *interior* of the insulator. Thus, we may write

$$J_i = \frac{dQ}{dt} = q\mu n_i F_i = q\mu N_c F_i \exp\left(\frac{2\beta F_i^{1/2} - E_1}{kT}\right), \tag{12}$$

where n_i and F_i are, respectively, the free-carrier density and field in the interior of the insulator. If the two depletion regions are small compared to the insulator thickness, which will normally be the case, we may write

$$F_i = [V - V_c(t)]/L \,. \tag{13}$$

The total charge in the CDR at any time, t, is

$$Q \simeq \tfrac{1}{2}(qN_t)\lambda_c(t) = (\epsilon N_t)^{1/2}(\phi_0 - E_1 + qV_c)^{1/2} \,,$$

from which we obtain

$$\frac{dQ}{dt} = q\left(\frac{\epsilon N_t}{\phi - E_1 + qV_c}\right)^{1/2} \frac{dV_c}{dt} \,. \tag{14}$$

From (12), (13), and (14) we have

$$\frac{dV_c}{dt} = \left(\frac{\phi - E_1 + qV_c}{\epsilon N_t}\right)^{1/2} \frac{\mu N_c (V - V_c)}{L} \times \exp\left\{\frac{1}{kT}\left[2\bar{\beta}\left(\frac{V - V_c}{L}\right)^{1/2} - E_1\right]\right\}. \tag{15}$$

Equation (15) cannot be integrated in closed form; however, the exponential term is the dominant variable. Thus, assuming this is the only variable, and noting that at the beginning of the decay process $V \gg V_c$, (15) yields the approximate solution

$$t = \frac{1}{2}\left(\frac{LkT}{\beta}\right)^2 \frac{(\epsilon N_t)^{1/2}}{(\phi - E_1)^{1/2} V\mu N_c}\left[\exp\left(\frac{E_1 - 2\beta F_i^{1/2}}{kT}\right) - \exp\left(\frac{E_1 - 2\beta F_0^{1/2}}{kT}\right)\right], \tag{16}$$

where $F_0 = V/L$. From (12) and (16) we find

$$t = \frac{1}{2}\left(\frac{LkT}{\beta}\right)^2 \frac{(\epsilon N_t)^{1/2} q}{(\phi - E_1)^{1/2} V}\left(\frac{F_i}{J_i} - \frac{F_0}{J_0}\right), \tag{17}$$

where $J_0 = e\mu n_i F_0$ is the current at the start of the relaxation process. From (17), when $F_i/J_i \gg F_0/J_0$, we see that the current decays hyperbolically with time.

The time t_r required for the relaxation current to decay to approximately one-half of its initial value is a measure of the relaxation time; thus, from (16) and (17) we have

$$t_r = \frac{1}{4}\left(\frac{LkT}{\beta}\right)^2 \frac{(\epsilon N_t)^{1/2}}{(\phi - E_1)^{1/2} V\mu N_c} \exp\left(\frac{E_1 - 2\beta F_i^{1/2}}{kT}\right). \tag{18}$$

Assuming $(\phi - E_1)/q = 1$ eV, $L = 10^{-4}$ cm, $\mu = 10$ cm^2/V sec^{-1}, $V/L = 10^5$ V cm^{-1}, $N_c = 10^{19}$ cm^{-3}, and $\epsilon = 5\epsilon_0$ (ϵ_0 is the permittivity of free space) we obtain

$$t_r = 10^{-23} N_t^{1/2} \exp[(E_1 - 2\beta F_i^{1/2})/kT] \,. \tag{19}$$

[Note that N_t in (19) is expressed in cm^{-3}.] If it is assumed that the trap density is 10^{18} cm^{-3} and $T = 300$ °K, then for $E_1 - 2\beta F_i^{1/2} = 0.5$ eV, $t_r = 10^{-5}$ sec and for $E_1 = 1.5$ eV, $t_r = 10^{12}$ sec. The former relaxation time is short compared to a dc measurement, hence the measurement yields the steady-state J-V characteristic of the system (see Sec. IV A). On the other hand, the latter relaxation time is long compared to a dc measurement, and hence the measurement yields the non-steady-state (relaxation) J-V characteristic (see Sec. IV A). Because $t_r = 10^{12}$ sec the relaxation current decays very slowly with time and can easily be misinterpreted as a steady-state measurement. If the insulator is cooled to, say, 100 °K, the two relaxation times, according to (19), are respectively 10^{14} and 10^{41} sec (however, see Sec. IV C). Clearly, if a constant voltage is applied at these low temperatures, the current measured in both cases is the relaxation (non-steady-state) current, which to all intents appears to be a constant and hence a steady-state current. Normally, in order to glean as much information as possible about the insulator, measurements are made over a wide range of temperature; thus the DRT and (as we shall see) the electrical properties of the sample will vary considerably owing to t_r being an exponential function of the temperature. This means, of course, we can only define a DRT if we define the temperature. [However, once it is known for a particular temperature, in principle it is known for all temperatures through (19).] Thus, for the purpose of comparison, the DRT of various insulators must be defined at a particular temperature, which for obvious reasons we will take to be 300 °K.

Here we will be concerned with three types of insulators: those which have a short , a long, and a moderate DRT at room temperature. By short DRT we mean a time that is short ($< 10^{-3}$ sec) compared to that required to make a dc measurement; thus the system is always in the steady state during the measurement. A long DRT means a time that is long ($> 10^5$ sec) compared to that required to make a dc measurement, which means that although the current will be essentially constant for a fixed voltage bias it is nevertheless a non-steady-state current. A moderate DRT means $t_r \simeq 10^2$ sec, so that during a dc measurement a strongly time-dependent non-steady-state current is observed to flow and eventually reach its steady-state value during the course of the measurement.

IV. ELECTRICAL CHARACTERISTICS: SHORT DRT

A. J-V Characteristics at Higher Temperatures

Let us assume that for the upper trap we have $E_1 < 0.5$ eV, so that at room temperature the in-

sulator has a short DRT [see (19)]. Thus, at room temperature when a voltage bias is applied to the system (Fig. 3) it relaxes quickly ($< 10^{-3}$ sec) to the steady state [Fig. 3(d)]. Since the cathodic Schottky barrier limits the rate of flow of electrons through the system, essentially all the applied voltage will be absorbed across the depletion region as shown in Fig. 3(d). The current flowing across this barrier and hence through the system is given by the Richardson–Schottky expression[25]

$$J_{RS} = 1.2\times10^{6}\, T^{2}\, e^{-\phi/kT}\, e^{\beta F_c^{1/2}/kT} . \tag{20}$$

In the above expressions J_{RS} is expressed in $A\,m^{-2}$,

$$\beta = (e^3/4\pi\epsilon)^{1/2} , \tag{21}$$

and F_c, which is the field at the cathode-insulator interface, is given by

$$F_c = (N_t/\epsilon)^{1/2}\,[\phi - E_1 + e(V-\Delta V)]^{1/2} , \tag{22}$$

where ΔV, which is normally a fraction of a volt, is that portion of the applied voltage absorbed across the interior and the forward-biased (anodic) Schottky barrier. Thus, at higher temperatures the current is a steady-state electrode-limited process. Also, the activation energy associated with the process, is from (20), $\phi - \beta F_c^{1/2}$, which is the energy of the interfacial barrier.[19,26]

At sufficiently high applied voltages, such that $F_c \simeq 10^6\ V\,cm^{-1}$, the interfacial potential barrier becomes permeable to electrons that can tunnel from the cathode into the insulator. When this process occurs, an electrode-limited–to–bulk-limited transition occurs in the conduction process.[1,27] In this case the activation energy associated with the process is that of the interior of the insulator (see Sec. IV B).

B. *J-V* Characteristic at Lower Temperatures

Consider what happens when the insulator is cooled to a low temperature, say 100 °K, when its relaxation time is now of the order 10^{12} sec. In this case, when the voltage is applied it remains uniformly distributed throughout the solid during the dc measurement [that is, the energy diagram will be as shown in Fig. 3(b)]. Hence the current measured in this case will be a bulk-limited and non-steady-state current. This relaxation current density can be identified with the current J_i flowing in the interior (see Sec. III A):

$$J_i = q\mu F N_c\, e^{-E_1/kT}\, e^{2\beta F^{1/2}/kT} , \tag{23}$$

where $F = V/L$ is the field in the interior of the insulator. In (23) we have used for the free-carrier density of the interior n_i the expression

$$n_i = N_c\, e^{-E_1/kT}\, e^{2\beta F^{1/2}/kT} , \tag{24}$$

in which the factor $e^{2\beta F^{1/2}/kT}$ arises owing to Poole–Frenkel lowering of the (donor-type) trap barriers.[17] Thus, at these low temperatures the conduction process manifests Poole–Frenkel conduction, but it is a *non-steady-state* process. The activation energy associated with this process is $[E_1 - 2\beta(V/L)^{1/2}]$, which is smaller than that associated with the steady-state high-temperature process—see (20)—and provides the activation energy of the upper trap level.[19] It will also be noted that, since the field in the interior is independent of the interfacial barrier heights, the magnitude of the current will be independent of the polarity of the voltage bias.

It will be apparent from the discussion in this and the previous sections that there will be a temperature, say T_0, above which the I-V characteristic is given by (20) and below which it is given by (23) (but see also Sec. IV C). Thus, around T_0 a distinctive change in the conduction process occurs, and these conduction processes are completely unrelated, since one is a steady-state process and the other a non-steady-state process. An approximate value for T_0 may be obtained from (19) by setting t_r equal to, say, 10 sec, yielding

$$T_0 \simeq E_1/1.15k(48 - \ln N_t) . \tag{25}$$

C. Very Low Temperatures and High Trap Densities

If the trap density is sufficiently high so that the wave functions of electrons in adjacent traps slightly overlap, and the temperature is sufficiently low, a thermally activated tunnel hopping process between the adjacent localized states will dominate the conduction process. In our case this current density is given by[9]

$$J_h = \tfrac{1}{2} e N_t\, \mu_h (V/L) , \tag{26}$$

where μ_h is the mobility associated with the hopping electrons and is given by

$$\mu_h = \nu_p\, (a^2/kT)\, e\, e^{-W/kT}\, e^{-2\infty a} , \tag{27}$$

where ν_p is the phonon frequency of the insulator ($\nu_p \simeq 10^{10} - 10^{13}\ sec^{-1}$), a is the average trap separation ($\simeq N_t^{-1/3}$), and W is the energy separation of allowed states of adjacent traps. The term $e^{-2\infty a}$ is the tunnel factor for adjacent traps; hence[28]

$$\infty = 4\pi(2m)^{1/2}\bar{\phi}^{1/2}/h , \tag{28}$$

where m is the electronic mass, h is Planck's constant, and $\bar{\phi}$ is the average height of the potential barrier separating adjacent traps. [In our discrete trapping level model it would appear that $W = aV/L$ and is hence a linear function of voltage. There are two reasons why this would not be so. First, the electrons can tunnel into excited states of the trap and subsequently fall into the lowest state. Second, the Coulombic interaction between

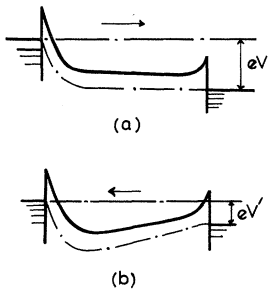

FIG. 4. Energy diagram of insulator: (a) after insulator has been cooled to low temperature with voltage applied; (b) after reducing voltage to V'. Arrows show direction of electronic current. Note that in (b) the sample is generating power JV'.

an empty, and hence a positively charged, donor-type trap (upper level) and a filled, and hence negatively charged, acceptor-type trap (lower level) perturbs the potential energy of the empty donor traps. Since the distance between acceptor-type and donor-type traps is random, so is the perturbation.] This is, of course, a non-steady-state process and the associated activation energy will normally be much smaller than for the two conduction processes, (20) and (23), previously discussed.

It will be apparent that, when this process is active, (19) is no longer applicable, except in that it defines the absolute upper limit for t_r.

D. Steady State at Low Temperature

Since the low temperatures described above are non-steady-state in nature, they cannot be related directly to the higher-temperature steady-state process. However, if the voltage bias is applied to the insulator at a sufficiently high temperature so that it relaxes to its steady state, and the sample then cooled slowly to low temperature, it will exist in the steady state at the low temperature. It follows, then, that if this procedure is repeated for all applied voltages, then an electrode-limited J-V characteristic will be obtained which may be related, through the appropriate activation energy, to the room-temperature measurements.[19]

It will be apparent that the current for a given voltage obtained by this procedure is necessarily lower than that obtained by applying the voltage after the temperature has been lowered, since the former represents the end of the decay process of the latter [cf. Figs. 3(b) and 3(d)].

E. Current Reversal and Power Generation

Let us assume that a voltage bias V is applied to the system at room temperature, and then the sample temperature lowered slowly so that it is in its relaxed state at low temperatures [Fig. 4(a)], as described in Sec. IV D. If now the voltage is *reduced* to V', since the system cannot relax at low temperatures, the energy diagram for the system is as shown in Fig. 4(b). This diagram is simply that of Fig. 4(a) with a positive linear field $(V - V')/L$ superimposed throughout the insulator. However, since the slope of the Fermi level is in the opposite direction to that shown in Fig. 4(a), the electronic current flows from the positively biased to the negatively biased electrode. This means that the conventional current flows from the negatively biased to the positively biased electrode; hence the system is generating power. Furthermore, this current is larger than the steady-state current, since the field in the interior, $(V - V')/L$, in the non-steady-state is larger than in the steady state [cf. Figs. 4(a) and 4(b)]. It will be apparent that the slope of the Fermi level in the interior of the insulator increases as the difference $(V - V')$ increases [cf. Figs. 4(a) and 4(b)] which means that the relaxation current *increases* with *decreasing* voltage. Also, it will be noted that when $V' < 0$ the applied voltage is of the *opposite* polarity to that which was applied as the sample was cooled; thus the current now flows in the conventional direction, but is non-steady-state.

F. Quasi-Steady-State

Consider an insulator with blocking contacts on its surfaces. It is assumed that the sample is at room temperature when a voltage is applied to the system so that the system relaxes quickly to the steady state during which time a relaxation current flows in the insulator in the cathodic to anodic direction. [This current, contrary to the essentially constant relaxation current generated at low temperatures (Sec. IV E) is a transient current and decays to zero in a time less than 10^{-4} sec.] Let us assume that the space charge in the cathodic space-charge region has increased by Q_c during the relaxation process. If the applied voltage is now reduced to V' [Fig. 5(b)], a rapidly decaying relaxation current flows in the system in the (original) anodic-to-cathodic direction by virtue of the fact that the Fermi level in the interior of the insulator slopes downward in that direction. Since the anodic contact is blocking, this current is essentially due to electrons generated in the interior of the insulator at the edge of the anodic depletion region (ADR). Physically what happens is that the ADR grows, and the resultant rate of release of charge provides the source of the relaxation current.

What happens to the relaxation current? It will be noted in Fig. 5(b) that the Fermi level everywhere in the cathodic depletion region (DR) lies below the cathodic Fermi level. Hence the relaxation current cannot flow out of the insulator at the cathode. In fact, there must be a net flow of current from the cathode into the insulator. However, since the cathode contact is assumed to be blocking, this current is negligible, but the fol-

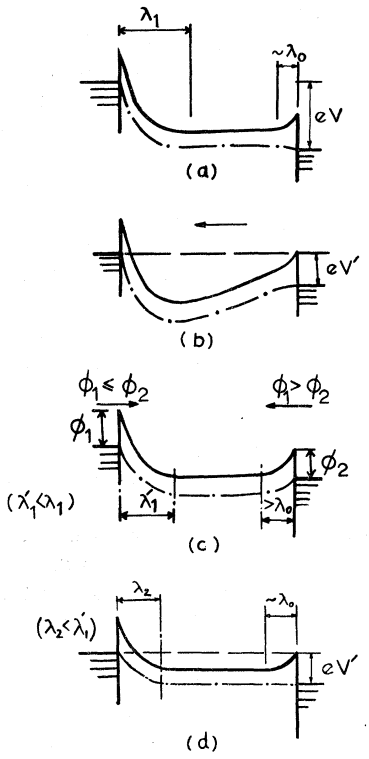

FIG. 5. Energy diagram of insulator: (a) initial steady state with voltage bias V applied; (b) immediately after reducing voltage to V'; (c) quasi-steady-state; (d) final steady state. Arrows show direction of electronic current.

lowing point has been made: The relaxation current does not flow out of the system at the cathode. Therefore, we conclude that the CDR acts as a sink for the relaxation current, with the result that the positive space-charge therein, and thus its width, decreases with time.

It will be apparent that the rate of increase of space charge in the ADR is essentially equal to the rate of decrease of space charge in the CDR. This state of flux continues until such times as the Fermi level in the interior is horizontal, Fig. 5(c), which means that the internal relaxation current ceases to flow, but the system is not yet in the steady state. This is because each depletion region contains an additional charge ΔQ over and above their steady-state values, where ΔQ is given by (see the Appendix)

$$\Delta Q = \frac{(q\epsilon N_t)^{1/2}}{2} \frac{(V - V')}{(V + \Delta\psi_1)^{1/2} + \Delta\psi_2^{1/2}} , \qquad (29)$$

where $\Delta\psi_1$ and $\Delta\psi_2$ are defined in the Appendix. This in turn means that the Fermi level in the interior is depressed below its steady-state position by an energy ΔE given by [see Fig. 5(c)]

$$\Delta E \simeq q(V_a - \Delta\psi_2) . \qquad (30)$$

We designate this state the quasi-steady-state. Normally, ΔE is approximately equal to the energy difference between the Fermi level in the interior and that of the positively biased electrode. (V_a is defined in the Appendix.)

For $V' < -V$, the applied voltage is *greater* than, and of opposite polarity to, that applied initially. Thus, during the relaxation process more than sufficient negative charge is released from the right depletion region to neutralize the excess space charge Q_c in the left depletion region. In other words, the system relaxes directly to the steady state.

G. Quasi-Steady-State-to-Steady-State Relaxation Process

The steady state is attained only when the space charge in the insulator corresponds to that required by the voltage bias under steady-state conditions. Thus, negative charge has to be injected into the insulator to reduce the excess positive charge; the source of this negative charge is the electrodes. If the two-electrode-insulator interfaces are identical, the currents associated with the negative charge flowing from the two electrodes into the insulator will be equal and opposite. Consequently, the current flowing in the external circuit will be zero. Also, since the contacts are assumed to be blocking at room temperature, the rate of flow of charge into the insulator will be small at that temperature. This in turn means that the time involved for the system to relax from quasi-steady-state to steady state will be relatively long.

Normally, the two interfaces will not be identical; thus, if the (original) cathodic interfacial barrier ϕ_1 is greater than the (original) anodic interface ϕ_2 [see Fig. 5(c)] the electronic relaxation current associated with the quasi-steady-state–to–steady-state process flows from anode to cathode [see direction of arrows in Fig. 5(c)]. If $\phi_1 < \phi_2$, this current flows from cathode to anode. The steady-state condition is shown in Fig. 5(c), for $0 < V' < V$.

Suppose the temperature is sufficient for the system to relax quickly to the steady state when a bias is applied, but requires a relatively long time to relax from the quasi-steady state to the steady state when the voltage is reduced. This means that the J-V characteristic for increasing voltage sweeps will differ from that for decreasing voltage sweeps, because in the former case the system is in the steady state and in the latter case in the quasi-steady-state. Thus, hysteresis will appear in the J-V characteristic for increasing and decreasing voltage sweeps. If, however, the system relaxes quickly ($< 10^{-2}$ sec) from the quasi-

steady-state to the steady state, the J-V characteristic will be essentially identical for increasing and decreasing voltage sweeps.

V. ELECTRICAL CHARACTERISTICS: LONG DRT

If $E_1 > 1$ eV then the DRT at 300 °K will be long. Thus, at this and lower temperatures the system will always be in non-steady-state [see Fig. 3(b)]. This means that the J-V characteristic will be of the non-steady-state Poole–Frenkel form, (12). (It is stressed here again that the current magnitude will be independent of polarity of bias.) Thus, although the contacts are blocking, the conduction process is a bulk property. At very low temperatures and large N_t, the tunnel hopping conduction process will prevail. Hence, generally speaking, the interpretation of these data will be less convertible than of insulators having short DRT. Nevertheless, it should be recognized that, in the case of the long DRT, one is always concerned with non-steady-state pehnomena.

At sufficiently high temperatures, of course, the insulator will have a sufficiently short DRT compared to the dc measurement so that the general comments of Sec. IV A regarding the steady-state conduction process will be applicable for this case.

VI. ELECTRICAL CHARACTERISTICS: MODERATE DRT

In Secs. IV and V we were concerned with constant, or essentially constant, steady-state (short DRT) and non-steady-state (long DRT) currents. Consider now a system having a moderate DRT, i.e., one in which the current is observed to be quite time dependent during the time a dc measurement is made. Moderate DRT's are defined as $t_r \simeq 10$ sec. (Such a DRT may be obtained in an insulator that does not satisfy the criterion at room temperatures by judiciously raising or lowering the temperature of the insulator.)

When a voltage bias V is applied to such a system, a non-steady-state time-dependent dc current given by (17)—see Fig. 6—will flow in the system as it relaxes from the state depicted by the energy diagram Fig. 3(a) to that of Fig. 3(b). The current will eventually relax to its equilibrium value given by (20). The excess charge in the CDR Q_c [see (11)] due to the applied voltage is given by

$$Q_c = \int_0^{t_r} (J_t - J_{RS})\, dt \ .$$

The integral corresponds to the shaded area shown in Fig. 6. Thus, knowing Q_c, the width of the depletion region, λ_c, can be estimated from (11)—if $\lambda_c \gg \lambda_0$—and hence the trap density N_t ($\simeq 2Q_c/q\lambda_c$) can be considered.

If the voltage is now further increased to, say, V_2, a time-dependent current given by (17) will again begin to flow as the system relaxes from the steady state corresponding to a voltage V_1 to that corresponding to V_2. The current corresponding to the initial portion of the decay will be greater than that for the initial voltage bias if $(V_2 - V_1) > V_1$ (i.e., if $V_2 > 2V_1$); otherwise it will be smaller, and will relax to its steady-state value[26] given by (20) (see Fig. 6).

On the other hand, if the voltage is decreased from V_1 to, say, $V_3 (> 0)$, initially a reverse current (i.e., one which flows in the opposite direction to the conventional current that normally flows for the applied bias) flows—see Fig. 6—as the system relaxes from the non-steady-state to the quasi-steady-state [see corresponding energy diagrams, Figs. 5(b) and 5(c)]. The current crosses the J axis when the (reverse) relaxation current is just equal to the current injected at the cathode. Thereafter, since the current injected at the cathode exceeds the relaxation current, the net current in the system flows in the positive direction as shown in Fig. 6. Note that in this case the system first decays relatively quickly to the quasi-steady state (see Sec. IV F), and then more slowly to the steady state (see Sec. IV G). If $V_3 < 0$, the polarity is the reverse of the initial voltage bias. Thus, the steady-state current corresponding to this bias will flow in the opposite direction to that of the initial voltage bias, as shown by the dotted line in Fig. 6(b).

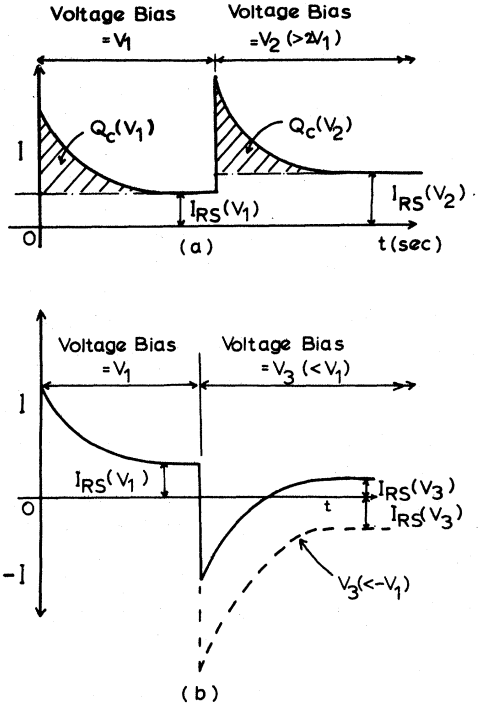

FIG. 6. J-T characteristic for insulator having a moderate DRT: (a) case $V = V_1$, V_2 ($> V_1$); (b) case $V = V_1$, $V_3 (< V_1)$; dotted line, case $V_3 < (-V_1)$.

VII. CONCLUDING REMARKS

It has been shown that the dielectric relaxation time plays an important role in determining the J-V characteristics of the insulator when blocking contacts exist on its surface. In the case of a long DRT the conduction process is non-steady-state in nature and is bulk-limited (Poole–Frenkel), even though blocking contacts exist on the insulator.

In the case of insulators in which the DRT is short, the system is in the steady state for increasing voltages. However, for decreasing voltages the system relaxes to a quasi-steady-state before finally decaying to the steady state. If the electrodes make good blocking contacts to the insulator, the relaxation to steady state may take a long period of time. This being the case, the current for decreasing voltages will differ from the steady-state current; thus, the J-V characteristics for increasing and decreasing voltage sweeps will exhibit hysteresis.

Because the DRT is a strong function of temperature, a conduction process which is steady state at higher temperatures will normally be non-steady-state at sufficiently low temperatures. On the other hand, if a voltage is applied to the system at a high voltage and subsequently cooled to low temperatures with the voltage applied, it will be in the steady state at the low temperature. However, if the voltage bias is now varied at the low temperature, non-steady-state currents will flow in the system. These non-steady-state currents will normally be greater than the steady-state current, even if the voltage bias is decreased; furthermore, in the latter case, the current is a reverse current, that is it flows in the opposite direction to the conventional direction of current flow.

The activation energies associated with the steady-state and non-steady-state current for the case of blocking contacts will normally be different. In the former case the conduction process is electrode limited and the activation energy reflects[19] the metal-insulator interfacial barrier.[27] The latter case reflects[19] a bulk-limited process, and the activation energy is that of the bulk.

Short and long DRT result in constant steady-state and essentially constant non-steady-state currents, respectively, from a dc point of view. Moderate DRT results in time-dependent dc currents, from which the charge in the depletion regions and trap density can be determined.

It is probable that blocking contacts exist at the metal-insulator interface, yet this point has only been considered in recent times, and by and large the possibility of such contacts has been ignored. This being the case, in view of the wide variety of conduction phenomena described above, it is not surprising that a good deal of mystery and controversy surrounds the nature of conduction mechanisms in thin films.[15–18] Clearly, a judicious analysis of conduction processes in insulators cannot ignore the possibility of blocking contacts existing on the insulator surface.

The equations presented herein are applicable to our particular insulator model. A more detailed model would include traps distributed throughout the band gap. Such a model would provide conduction processes (and equations) that differ in detail rather than in principle from what has been presented here. In other words, the ideas presented herein are expected to be qualitatively correct for any practical insulator model.

APPENDIX: CALCULATION OF ΔQ

From Fig. 5(c) we find

$$\phi_2 - qV_2 + qV_1 - \phi_1 = qV' \tag{A1}$$

or

$$V_1 - V_2 + \Delta\phi = V' , \tag{A2}$$

where

$$\Delta\phi = (\phi_2 - \phi_1)/q = (\psi_{m2} - \psi_{m1})/q . \tag{A3}$$

Let Q_T be the total charge in the CDR when a voltage V is initially applied to the system, and λ_c be the width of the CDR in the quasi-steady-state. Hence, the charge in the CDR in the quasi-steady-state is [see A(7)]

$$Q_T - \Delta Q = \tfrac{1}{2} N_t \lambda_c = (q\epsilon N_t V_c)^{1/2}$$

or

$$(Q_T - \Delta Q)^2 = q\epsilon N_t V_c . \tag{A4}$$

Similarly for the ADR we find

$$(\Delta Q + Q_{0a})^2 = q\epsilon N_t V_a , \tag{A5}$$

where Q_{0a} is the charge in the ADR at zero bias and under forward bias (approximately). From (A2), (A4), and (A5) we see

$$(Q_T - \Delta Q)^2 - (\Delta Q + Q_{0a})^2 = (q\epsilon N_t)(V' - \Delta\phi)$$

or

$$\Delta Q = \frac{(Q_T^2 - Q_{0a}^2) - (q\epsilon N_t)(V' - \Delta\phi)}{2(Q_T + Q_{0a})} . \tag{A6}$$

Now we have

$$Q_T^2 \simeq (q\epsilon N_t)(V + \Delta\psi_1) \tag{A7}$$

and

$$Q_{0a}^2 \simeq (q\epsilon N_t \Delta\psi_2) , \tag{A8}$$

where

$$\Delta\psi_1 = \frac{(\phi_1 - E_t)}{q} = \frac{\psi_{m1} - \psi_i}{q} \tag{A9}$$

and

$$\Delta\psi_2 = \frac{(\phi_2 - E_t)}{q} = \frac{\psi_{m2} - \psi_i}{q} . \tag{A10}$$

Substituting (A7) and (A8) in (A6) we obtain

$$\Delta Q = \frac{(q\epsilon N_t)^{1/2}(V - V')}{2[(V + \Delta\psi_1)^{1/2} + \Delta\psi_2^{1/2}]} . \tag{A11}$$

*Supported in part by Defense Research Board and National Research Council of Canada under Grant No. A7124.

[1]J. G. Simmons, Phys. Rev. 166, 912 (1968).

[2]J. G. Simmons and G. S. Nadkarni, J. Vac. Sci. Tech. 6, 9 (1969).

[3]J. G. Simmons, G. S. Nadkarni, and M. C. Lancaster, J. Appl. Phys. 41, 538 (1970).

[4]G. S. Nadkarni and J. G. Simmons, J. Appl. Phys. 41, 545 (1970).

[5]J. G. Simmons, J. Phys. Chem. Solids 32, 2581 (1971).

[6]J. G. Simmons, *Handbook of Thin Film Technology* (McGraw-Hill, New York, 1970), Chap. 14.

[7]A. Rose, *Concepts in Photoconductivity and Allied Problems* (Interscience, New York, 1963).

[8]R. Bube, *Photoconductivity of Solids* (Wiley, New York, 1960).

[9]N. F. Mott, Advan. Phys. 16, 49 (1967).

[10]I. T. Johannsen, J. Appl. Phys. 37, 449 (1966).

[11]H. Hirosha and Y. Wada, Japan. J. Appl. Phys. 3, 179 (1964).

[12]C. A. Mead, Phys. Rev. 128, 2088 (1962).

[13]M. Stuart, Brit. J. Appl. Phys. 18, 1637 (1967).

[14]M. Stuart, Phys. Status Solidi 23, 595 (1967).

[15]T. E. Hartman, J. C. Blair, and R. Bauer, J. Appl. Phys. 37, 2468 (1966).

[16]T. E. Hartman, J. C. Blair, and C. A. Mead, Thin Solid Films 2, 79 (1968).

[17]J. G. Simmons, Phys. Rev. 155, 657 (1967).

[18]J. C. Schug, A. C. Lilly, and D. A. Lowitz, Phys. Rev. B 1, 4811 (1970).

[19]J. G. Simmons and G. Taylor, following paper, Phys. Rev. 6, 4804 (1972).

[20]This property likens our system to one in which a distribution of traps exists in the insulator, in which the Fermi level is also essentially temperature independent (see Ref. 5).

[21]The inequality (4) is a more general statement than (3) and accommodates any effects due to surface states. Only when (2) is invoked are surface states assumed to be negligible; in this case (4) transfers to (3).

[22]With λ expressed in the form (5) effects of surface states, should they be manifest, have been accommodated. Only when (2) is invoked are surface-state effects assumed to be negligible.

[23]Strictly speaking, the large signal capacitance C_λ' of the CDR should be compared with C_g since we are normally concerned with large variations in voltage. However, the calculation of C_λ' is tedious, and not given here, since the same conclusion prevails as obtained considering C_λ.

[24]Or if the capacitance were measured at a frequency such that $f \gg t_r^{-1}$.

[25]J. G. Simmons, Phys. Rev. Letters 15, 967 (1965).

[26]The interfacial barriers are not necessarily, and most probably not, equal. If this is so, the magnitude of the activation energy will depend on the polarity of bias (Ref. 19).

[27]If the trap density is sufficiently high, the field at the interface can be greater than 10^{-6} V cm^{-1} even at zero bias. When this is the case, the activation energy even at the lowest applied voltages will not reflect that of the interfacial barrier, nor will the J-V characteristic be given by (20) (see Ref. 1 for further details).

[28]J. G. Simmons, J. Appl. Phys. 39, 1793 (1963).