Dispersion and tunneling analysis of the interfacial gate resistance in Schottky barriers

H. Rohdin, N. Moll, A. M. Bratkovsky, and C.-Y. Su*
Hewlett-Packard Laboratories, P.O. Box 10350, Palo Alto, California 94303
(Received 15 January 1999)

We present a theoretical explanation of the interfacial component in the gate resistance of Schottky-barrier-gate field-effect transistors (SBGFETs). This component was recently established and was found, for GaAs- and InP-based SBGFETs, to have the smallest practically achievable normalized value r_{gi} on the order of $10^{-7}\ \Omega\,\mathrm{cm}^2$. We show that r_{gi} in this range can be modeled as an ac tunneling resistance r_{IT} between the three-dimensional (3D) gate metal and the 2D semiconductor surfaces states. We extend Cowley and Sze's static Schottky-barrier lineup model to include high-frequency modulation of the surface-state occupation by an ac gate voltage. We find that, since r_{IT} is not simply a dc resistance in series with the standard parasitic gate resistance, the resulting experimentally observed r_{gi} is smaller by an amount that depends on the interfacial layer and surface-state density. However, for the typically observed values, r_{gi} acts like a series resistance up to presently attainable frequencies. Thus, while Cowley and Sze's phenomenological ''interfacial layer of the order of atomic dimensions'' is more or less ''transparent to electrons,'' it presents a resistance that cannot be ignored at microwave and millimeter-wave frequencies. We apply our theory using interfacial-layer parameter values corresponding to alternative models for Schottky-barrier formation, and compare the predictions to experimental observations. Our results are consistent with models that involve defects near the semiconductor-metal interface. [S0163-1829(99)10119-X]

I. INTRODUCTION

We recently established[1,2] a previously overlooked interfacial component R_{gi} in the gate resistance R_g of Schottky-barrier-gate field-effect transistors (SBGFETs) such as modulation-doped field-effect transistors (MODFETs) and metal-semiconductor field-effect transistors (MESFETs). R_{gi} was shown experimentally to dominate the input resistance R_{in} of short-gate high-speed SBGFETs. The other two components, the gate metallization resistance R_{ga} and the gate-source capacitance charging resistance R_i (or R_{GS}), used in the past to account fully for R_{in}, were shown to be of secondary importance for these FETs. Furthermore, the skin-effect correction factor to R_{ga} was shown by three-dimensional (3D) numerical analysis to be negligible at any presently attainable frequency. R_{gi} is thus of practical importance to the performance, modeling, and optimization of high-speed SBGFETs, as discussed in Ref. 2. The origin of R_{gi} was proposed to be an interfacial barrier between the gate metal and the semiconductor surface. A large number of data on a variety of InP- and GaAs-based SBGFETs suggests that a smallest routinely achievable normalized interfacial gate resistance r_{gi} is on the order of $10^{-7}\ \Omega\,\mathrm{cm}^2$.[2] In this paper we theoretically evaluate the notion that this minimum value is related to the behavior of a Schottky barrier formed as ideally as a practical manufacturing environment will allow. The paper has essentially three parts. The first investigates the frequency dependence of the admittance of such a ''practically ideal'' Schottky barrier. The second develops a theory for electron tunneling between the metal and semiconductor surface states and compares this with an existing theory. The third part uses the theory to calculate the interfacial resistance component r_{IT} in the admittance, and the resulting measurable interfacial gate resistance r_{gi}, assuming alternative models for Schottky-barrier formation found in the literature.

II. THE COWLEY-SZE MODEL AS A BASIS FOR ANALYZING THE INTERFACIAL GATE RESISTANCE

As discussed in Ref. 2, we consider $r_{gi}=3\times 10^{-7}\ \Omega\,\mathrm{cm}^2$ the lowest reproducible value for our epitaxial III-V semiconductor material system, and 0.1-μm gate process.[5] Experimental variations in this value may occur due to differences in wet chemical cleanup of the deep submicron openings in the resist prior to gate evaporation, and in surface oxidation between the clean-up dip and evaporation. For some individual devices with longer gates we have seen values as low as $4\times 10^{-8}\ \Omega\,\mathrm{cm}^2$, however, the correction term for the channel resistance in series with r_{gi} is overestimated for longer gates with the method used.[2] In this respect, deep submicron devices are particularly well suited for studying the interfacial gate resistance. Also, to properly subtract out other components in the gate resistance, one should look at several gate *widths* for each gate length,[2] something we have only been able to do for our standard 0.1-μm-long gates. Although it is easier to clean up a large resist cut prior to evaporation, our sintered gate process[5] should result in a Schottky barrier that approaches the physically ideal. Summarizing the experimental findings, there appears to exist a smallest value $r_{gi}^{(\mathrm{min})}$ for the interfacial gate resistance which is on the order of $10^{-7}\ \Omega\,\mathrm{cm}^2$, and which we believe corresponds to a metal-semiconductor interface free of contaminants.

A widely used, and analytically tractable, model for Schottky-barrier formation is that by Cowley and Sze.[3,4] They explained the barrier heights of a variety of metals on Si, GaP, GaAs, and CdS, by assuming the existence of an interfacial layer between the metal and semiconductor. This has to have a thickness that is on the order of a few atomic layers to be transparent to electrons, and has to withstand a potential across it to account for the deviation of real barrier heights from the difference between the metal work function

 ©1999 The American Physical Society

Φ_M and the semiconductor affinity $X_{\rm sc}$. An interfacial layer with 4–5-Å-thickness, and vacuum electronic properties, was assumed. While this picture is not a precise representation of physical reality, it can explain the behavior of a wide variety of barriers, and it probably does contain the macroscopic physics of Schottky barriers. Its simplicity and adaptability make it a potentially attractive basis for analyzing the interfacial gate resistance. However, the tunneling behavior of Schottky barriers in the Cowley-Sze model is much more sensitive to details of the representation than is the barrier height. It becomes important to understand more precisely the physical situation that the Cowley-Sze interfacial layer represents.

First-principles models for Schottky-barrier formation typically assume an ideal barrier in the sense that the metal and semiconductor atoms are nearest neighbors,[6–8] with no interpenetration of materials. In the most ideal case,[6] metal electron wave functions penetrate into the semiconductor, where they populate part of a continuum of gap states, which are referred to as MIGS, for metal-induced gap states. The Fermi level is pinned near a ''canonical'' energy, which is a function of the bulk semiconductor band structure, and corresponds to local charge neutrality.[9] This picture of Schottky-barrier formation is controversial, and its failure, upon closer inspection,[7,8,10,11] to predict the generally observed essentially metal-independent Fermi level pinning suggests that the problem is more complicated than assumed. The most likely complication is that defects, with associated energy levels pinning the Fermi level inside the forbidden gap, form in the semiconductor close to the interface. There are many possible alternative microscopic origins of these defects, including antisites (for III-V compounds) and vacancies,[8,11] new chemical compounds, and changes in atomic geometry.[10] These can be affected by such factors as morphology, stoichiometry, surface reconstruction, surface preparation, and metal reactivity.[12] One prominent defect model relies on semiconductor native defects,[13,14] and is in its final refined form[14] referred to as the advanced unified defect model (AUDM). Another proposed complication is the formation of a thin bond-disordered layer in the semiconductor near the interface, resulting in a continuum of disorder-induced gap states (DIGS).[15,16] Similar to the MIGS case, the Fermi level is proposed to be pinned near a ''neutral level'' which depends only on the bulk semiconductor band structure. Some combination of these[17] and other mechanisms[18,19] may be involved in determining the barrier height.

While the details of why the midgap states come to exist differ radically in all these pictures, the existence of a dipole layer between the metal and semiconductor is not controversial. Thus in some sense, the Cowley-Sze model can be adapted to any physical reality, whether it corresponds to a barrier dominated by MIGS, defects, or bond disorder, through judicious choice of the properties of the interfacial layer and midgap states. For some interfacial conditions the Cowley-Sze model is not just a convenient construct for analytical modeling, but also a good physical representation. In addition to the case of a thin native oxide, surface reconstruction of GaAs has been proposed to result in true MIS-like (MIS denotes metal-insulator-semiconductor) Schottky barriers.[20] In Secs. III and IV, we will use the Cowley-Sze picture to lay the theoretical groundwork for the existence of the interfacial gate resistance, without tying it to any particular physical interpretation. In Sec. V we will examine the interfacial gate resistance that we predict for different choices of interfacial-layer properties, appropriate to different physical models.

III. THE MODULATION DYNAMICS OF THE SEMICONDUCTOR SURFACE STATES IN A SCHOTTKY BARRIER AT MICROWAVE AND MILLIMETER-WAVE FREQUENCIES

The interfacial-layer model[3,4] was developed to explain the static lineup of the bands. Similar models have been used to analyze I-V and low-frequency C-V characteristics.[21–25] In this section we will use the model to understand quantitatively how an interfacial layer can produce a dominant component in the important parasitic gate resistance of high-performance Schottky-barrier FETs.[2] We will thus examine the effect of modulating the metal (gate) voltage at microwave and millimeter-wave frequencies. At these frequencies, and normal bias, recombination of bulk semiconductor carriers at the surface state can be neglected. This makes the admittance analysis considerably less complicated than in Refs. 21, 22, and 25.

Figure 1 corresponds closely to Sze's Fig. 15.[4] In Sec. V, we will consider situations where the interfacial layer is not a vacuum, and we have therefore introduced an affinity X_i, a conduction-band edge E_{Ci}, and a valence-band edge E_{Vi} for the interfacial layer. Otherwise we use the same nomenclature, with a few exceptions (d_i, V_i, $X_{\rm sc}$, and $V_{\rm sc}$). The signature difference is that we let a nonstationary voltage V be applied to the metal. This results in a varying electron quasi-Fermi level $E_{F\rm sc}$ in the semiconductor, and a Fermi level split $E_{Fi}=E_{FS}-E_{FM}$ across the thin interfacial layer, where E_{FS} and E_{FM} are the Fermi levels for the surface states and the metal, respectively. Sze's built-in voltage $V_{\rm BI}$ in the semiconductor (sc) will also change, and we denote this modified voltage $V_{\rm sc}$. Ideally, $V_{\rm sc}=V_{\rm BI}-V$, but even at dc this is generally not the case.[24] We are interested in small-signal ac variations, prefixed by δ, in a bias and frequency regime not dominated by dc conduction across the semiconductor barrier. We will see a deviation from ideality due to the voltage division between the semiconductor and the interfacial layer. The ac driving force δV will result in similarly denoted ac variations in the ''primary'' variables E_{Fi}, V_i, and $V_{\rm sc}$. Variations in $Q_{\rm sc}$, Q_M, Q_S, and J can be expressed in terms of these. The other parameters in Fig. 1 are fixed, independent of V.

The voltage division is expressed by

$$\delta V=-\delta V_i-\delta V_{\rm sc}. \quad (1)$$

Charge conservation requires that

$$\delta Q_{\rm sc}+\delta Q_M+\delta Q_S=0, \quad (2)$$

where

$$\delta Q_{\rm sc}=c_D(V_{\rm sc})\delta V_{\rm sc}, \quad (3)$$

$$\delta Q_M=-c_i\delta V_i, \quad (4)$$

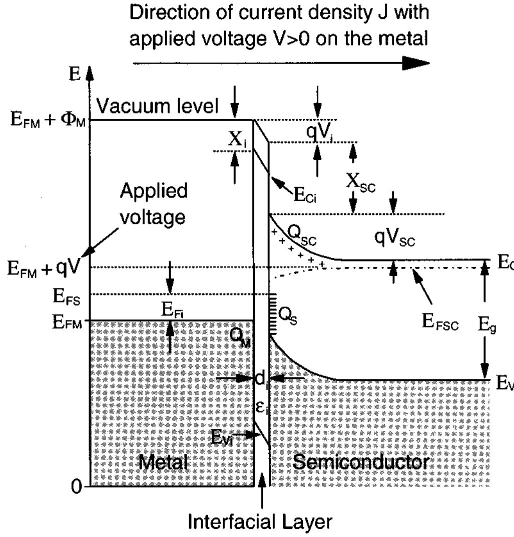

FIG. 1. Cowley and Sze's energy-band diagram (Ref. 4) for a metal-semiconductor (n-type) contact with an interfacial layer. The electron energy E is referenced to the bottom of the metal conduction band. The voltage drops V_i and V_{sc}, and the Fermi energy split E_{Fi} are positive as drawn.

and

$$\delta Q_S = -c_S(\delta V_i + \delta E_{Fi}/q). \tag{5}$$

$c_D(V_{\mathrm{sc}})$ is the doping- and structure-dependent semiconductor depletion capacitance per unit area. The other two normalized capacitances are

$$c_i = \frac{\varepsilon_i}{d_i} \tag{6}$$

for the interfacial layer, and

$$c_S = q^2 D_S \tag{7}$$

for the surface states, where D_S is the density of surface states at the bias position of E_{FS}. Some defect models involve sharp peaking of $D_S(E)$ at the pinning position.[13] The MIGS model[6] suggests a rather uniform distribution which tends to increase near the valence- and conduction-band edges. In the DIGS model[15,16] the Fermi level is pinned near a pronounced minimum in $D_S(E)$. These details do not affect our analysis. For small δE_{Fi}, the tunneling current density δJ_t can be expressed in terms of a linear resistance, the interfacial tunneling resistance r_{IT}. δJ_t is a real (in-phase) conductive current in the interfacial layer, and the metal; i.e., unlike the parallel displacement current, it does not contribute to the metal charge Q_M. Like the displacement current, however, δJ_t is an ac current. It is proportional to the small ac ''unpinning'' of the Fermi level, described by δE_{Fi}:

$$\delta J_t = \frac{d\,\delta Q_S}{dt} = j\omega\,\delta Q_S = \frac{\delta E_{Fi}/q}{r_{\mathrm{IT}}}. \tag{8}$$

The standard dc diode current across the depletion region can be accounted for in the equivalent circuit by conductances in parallel with the gate-source and gate-drain capacitances. These conductances are negligible at high frequency, and we ignore them.

The preceding equations lead to solutions, first for the voltage division:

$$\frac{\delta V_{\mathrm{sc}}}{\delta V} = -\frac{1}{1 + \dfrac{c_D}{c_i + \dfrac{c_S}{1 + j\omega c_S r_{\mathrm{IT}}}}}, \tag{9}$$

and ultimately for the admittance per unit area:

$$y(\omega) = \frac{\delta J}{\delta V} = j\omega c_D\left(\frac{-\delta V_{\mathrm{sc}}}{\delta V}\right) = \frac{j\omega c_D}{1 + \dfrac{c_D}{c_i + \dfrac{c_S}{1 + j\omega c_S r_{\mathrm{IT}}}}}. \tag{10}$$

For the total ac current density δJ in Eq. (10), we used the expression $j\omega c_D(-\delta V_{\mathrm{sc}})$ which is valid in the depletion region. The expression $\delta J_t + j\omega c_i(-\delta V_i)$, valid in the metal and interfacial layer, leads to the same result, as it should. The denominator in Eq. (9) is the ac ideality factor associated with a nonideal ($c_i < \infty$) interface. Not surprisingly, the result in Eq. (10) is very similar to that of a metal-oxide-semiconductor (MOS) analysis. In fact, the result of Terman's original MOS admittance analysis [Eq. (13) in Ref. 26] is identical to our Eq. (10), after exchanging his parameters ε_{ox}/W_{ox}, C_D, $|dQ_s/dV_s|$, and τ with our c_D, c_i, c_s, and $r_{\mathrm{IT}}c_s$, respectively. The parameter exchange stems from the surface states, in our case, communicating with the nearby metal, rather than with the semiconductor. Terman's ''energy loss mechanism,'' associated with charging and discharging the surface states through the semiconductor, becomes in our case the loss due to tunneling through the interfacial layer. The equivalent circuit for the admittance in Eq. (10) is shown in Fig. 2(a). We also show the circuit in Fig. 2(b) because it corresponds to the standard zero drain basis SBGFET equivalent circuit in Ref. 2, Fig. 4 (without the source and drain access resistances), used to extract the gate resistance. It has the simple one-pole admittance

$$y(\omega) = \frac{j\omega c_g}{1 + j\omega r_{gi} c_g}. \tag{11}$$

With

$$r_{gi} = \frac{r_{\mathrm{IT}}}{(1 + c_i/c_S)^2} \tag{12}$$

and

$$c_g = \frac{c_D}{1 + [c_D/(c_i + c_s)]}, \tag{13}$$

the circuit in Fig. 2(b) has the same admittance as that in Fig. 2(b), to second order in $j\omega$. We have thus identified the phenomenological, experimentally inferred, interfacial gate resistance r_{gi} in terms of the underlying physical tunneling resistance r_{IT}, the interfacial layer capacitance c_i, and capacitance c_s associated with the surface states. We have also

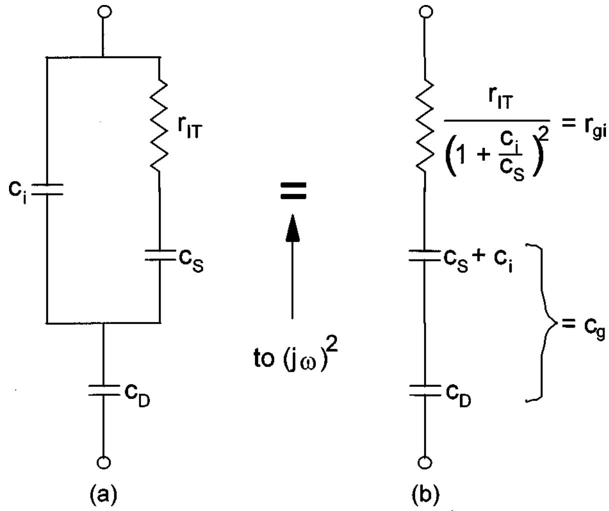

FIG. 2. (a) Equivalent circuit for the admittance in Eq. (10), and (b) the standard FET equivalent circuit, corresponding to Eq. (11). The two are equivalent to second order in $j\omega$.

identified the normalized SBGFET gate capacitance c_g as being c_d and $c_i + c_s$ in series. The denominator in Eq. (13) is the dc limit of the ac ideality factor discussed above. It is consistent with the dc analysis in Ref. 24 in the bias regime where the surface states are in equilibrium with the metal. The value is close to unity for a physically ideal GaAs Schottky barrier, and presumably also for AlInAs, since we have found essentially the same $r_{gi}^{(\mathrm{min})}$ for AlInAs and GaAs Schottky-barrier layers. For GaAs we can demonstrate this by assuming, as suggested in Ref. 3, interfacial-layer parameters $d_i = 5$ Å and $\varepsilon_i = \varepsilon_o$, and using the relation

$$\gamma = \frac{\partial \Phi_{B0}}{\partial \Phi_M} = \frac{1}{1 + q^2 D_S d_i / \varepsilon_i} \tag{14}$$

for the sensitivity of the Schottky-barrier height to metal work function and its 0.074 experimental value,[3] to calculate $D_S = 1.38 \times 10^{14}$ cm^{-2}/eV. This results in $c_s = 22$ μF/cm^2 and $c_i = 2.0$ μF/cm^2 (the latter being quite similar to that extracted for metal-Si diodes by fitting interfacial-layer theory to experimental I-V curves[23]). With a typical depletion capacitance $c_D = 0.45$ μF/cm^2, corresponding to a 25-nm gate-channel spacing, the dc limit of the ideality factor is 1.02.

Figure 3 shows that the two circuits in Fig. 2 are, for our model GaAs Schottky barrier, practically equivalent up to very large frequencies. We have plotted the equivalent series capacitance $\mathrm{Im}(y)/\omega$, and the r_{gi} estimate $\mathrm{Re}(y)/\mathrm{Im}^2(y)$,[2] applied to Eqs. (10) and (11). Equations (12) and (13) determine the r_{gi} and c_g used in Eq. (11). The choice $r_{\mathrm{IT}} = 2.18 \times 10^{-7}$ Ω cm^2 is based on results in Sec. V. It leads to $r_{gi} = 1.84 \times 10^{-7}$ Ω cm^2, which is in the range of the experimentally observed $r_{gi}^{(\mathrm{min})}$. At frequencies >100 GHz deviations develop, but these are insignificant compared to the experimental uncertainties. Thus, there is no bypassing of $r_{gi}^{(\mathrm{min})}$ at practical frequencies. The frequency independence of $\mathrm{Re}(y)/\mathrm{Im}^2(y)$ reinforces its usefulness in providing an estimate of the gate resistance, although a better choice would have been $\mathrm{Re}(1/y)$. For the cases we study, the two lead to indistinguishable results.

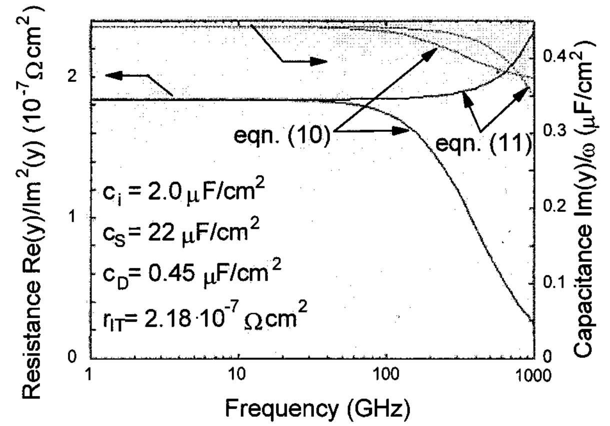

FIG. 3. Frequency dependence of the equivalent series R-C circuit elements for the admittances in Eqs. (10) and (11), with typical value for the interfacial gate resistance ($r_{gi} \approx r_{gi}^{(\mathrm{min})}$).

The results in this section indicate that the minimum interfacial gate resistance that we extracted in Ref. 2 is consistent with metal-to-surface-state tunneling, and does not go away at high frequencies of interest. The model has been developed consistently with Cowley and Sze's classical interfacial-layer model for Schottky-barrier formation. We now move on to develop the tunneling theory to be used in Sec. V to predict the interfacial tunneling and gate resistances with different representative interfacial-layer parameters.

IV. THEORY FOR THE INTERFACIAL TUNNELING RESISTANCE

Of the earlier modeling work referenced above, only Freeman and Dahlke[21] analyzed the physics of the tunneling problem. They developed a theory for tunneling through the insulator between metal and surface states in a MIS structure. The natural application for this theory is silicon MOS, where the oxide insulator is intentionally present. A small dc current can still flow because of tunneling, the presence of carriers at the semiconductor interface, and their recombination at the interface states. Our situation is quite different in that (1) the tunneling barrier is an unintentional interfacial layer with thickness on the order of a few monolayers; and (2) we are interested in frequencies and biases where the surface states communicate only with the adjacent metal, i.e., we can neglect generation and recombination of bulk carriers at the surface states. Nevertheless, this situation is a special case for which the theory in Ref. 21 applies. Our analysis of the tunneling current will, however, differ from that in Ref. 21 in one major and several minor respects. The major difference is the quantum mechanical representation of the surface state. Reference 21 treated the surface states as a two-dimensional electron gas confined in the interface plane by a one-dimensional δ potential. The effects of lateral localization were accounted for by a phenomenological tunneling capture cross section. We calculate r_{IT} from tunneling to individual, localized states using Fermi's golden rule, as it translates to tunneling current,[27] and Bardeen's method[28] for calculating the tunneling matrix element. We will point out the minor differences at the appropriate points of the analysis, and in the end compare the theory in Ref. 21 with ours.

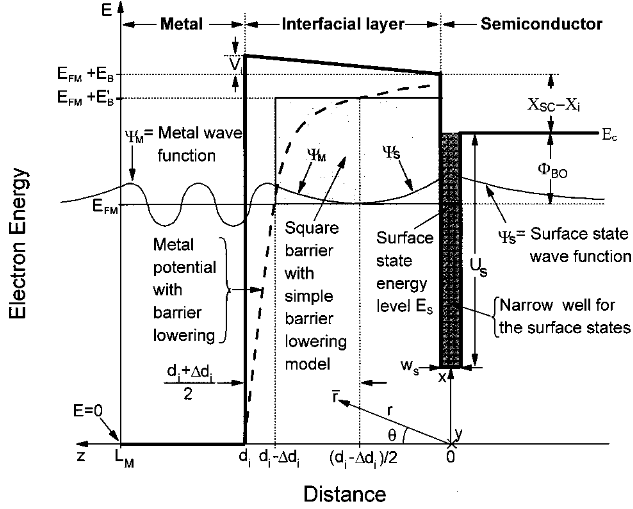

FIG. 4. Detailed energy-band diagram for the metal-to-surface-state tunneling problem. In Ref. 21 the potential well for the surface state is a 1D δ-function potential $[\delta(z); w_s \to 0, U_s \to \infty, w_s U_s = \text{const}]$ in the xy plane. In our alternative picture the well is a 3D θ-dependent δ potential $[g(\theta)\delta(r); w_s \to 0, U_s \to \infty, w_s^2 U_s = \text{const}]$ centered at the individual surface state.

A. General formalism for tunneling between metal and surfaces states

The tunneling problem to be solved here is illustrated in Fig. 4. Energy (E), transverse momentum ($\mathbf{k}_{xy}$), and spin are conserved. We do not consider inelastic tunneling and other possible complications.[29] The expression for the metal-to-surface state tunneling current density[27] is

$$J_t = \frac{q}{\pi\hbar}\int d^2k_{xy}\int dE[f(E-E_{Fi})-f(E)] \times \rho_S(E-E_{Fi})\rho_M(E,k_{xy})|M_{SM}(E,k_{xy})|^2. \quad (15)$$

E is referenced to the bottom of the metal conduction band, and the Fermi distribution f has thus been raised on the semiconductor side by E_{Fi} due to the applied bias V (Fig. 1). ρ_M is the one-dimensional density of states in the metal, spin not included. With cosine wave-function solutions (Fig. 4) and associated (nonperiodic) boundary conditions, ρ_M is given by

$$\rho_M(E,k_{xy}) = \frac{L_M}{\pi}\left(\frac{\partial E}{\partial k_z}\right)^{-1} = \frac{L_M m_M}{\pi\hbar^2 k_z(E,k_{xy})}, \quad (16)$$

where L_M is the thickness of the metal, k_z is the component along the z axis of the wave vector, and m_M is the electron effective mass in the metal. Assuming isotropic effective mass, k_z is given by

$$k_z^2(E,k_{xy}) = \frac{2m_M E}{\hbar^2} - k_{xy}^2. \quad (17)$$

The density of surface states is

$$\rho_S(E) = \sum_{s'} \delta(E-E_{S'}), \quad (18)$$

where the $E_{S'}$'s are the energies of the surface states. We will solve for the tunneling current from a single surface state (energy E_S) to the metal, and then perform the sum, which can be expressed as an integral:

$$\sum_{S'} = A_{xy}\int dE_{S'} D_S(E_{S'}), \quad (19)$$

where A_{xy} is the cross-sectional area in the xy plane, and the integral should be taken over the E_{Fi} gap in Fig. 1. For our small excursions from equilibrium, the sum becomes the factor $A_{xy}D_S E_{Fi}$.

The factor of 2 for spin is already included in Eq. (15),[27] thus the absence of it in both Eqs. (16) and (18). This is the first minor modification of Ref. 21. M_{SM} is the tunneling matrix element, calculated by Bardeen's method:[28]

$$M_{SM}(E,k_{xy}) = -\frac{\hbar^2}{2m_i}\int_{S_{SM}} d\mathbf{S}(\Psi_S^*\nabla\Psi_M - \Psi_M\nabla\Psi_S^*), \quad (20)$$

where m_i is the electron effective mass in the interfacial tunneling barrier, Ψ_S is the surface-state wave function, and Ψ_M is the metal electron wave function. S_{SM} is a simple, but arbitrary-shaped, surface that completely separates the surface state from the metal, and lies in the barrier region between the two.

B. Models for the tunneling barrier, metal wave-function tail, and effective masses

Before we can determine the two wave functions in Eq. (20), we must define the details of our tunneling problem. Considering that we are interested in very thin layers with only approximately known characteristics, we neglect details in the barrier shape, and changes to this induced by the ac voltage. We thus assume a constant square barrier height E_B, which implies that V_i in Figs. 1 and 4 is zero. For an intermediate metal work function ($\Phi_M \approx 4.9$ V), this is a good approximation for GaAs, but one can expect V_i to vary approximately ± 0.8 eV with different metals (Al,Ti,Pt, Mo).[30] The applied ac voltage is too small to significantly affect the barrier. The variability on the metal side of the barrier is overshadowed by the image force[31] indicated qualitatively in Fig. 4. We express the tunneling barrier in terms of quantities on the semiconductor side in Fig. 4:

$$E_B = \Phi_{B0} + X_{sc} - X_i. \quad (21)$$

Using Eq. (3-99) in Ref. 31, the image force extends the range of the metal potential beyond the background ionic core by

$$\Delta d_i = \frac{q^2}{16\pi\varepsilon_i^{(\infty)} E_B}\frac{E_{FM}}{E_{FM}+E_B}, \quad (22)$$

at $E = E_{FM}$. In the simple free electron gas model E_{FM} is expressed as

$$E_{FM} = \frac{\hbar^2 k_{FM}^2}{2m_M}, \quad (23)$$

in terms of the Fermi sphere radius:

$$k_{FM}=(3\pi^2 n_M)^{1/3}\approx 1.2 \ \text{Å}^{-1}. \quad (24)$$

n_M is the concentration of metal carriers, assumed to be equal to the atomic concentration ($\approx 6\times 10^{22}$ cm^{-3}). $\varepsilon_i^{(\infty)}$ is the high-frequency dielectric constant appropriate for tunneling.[32] The tunneling distance for electrons at the Fermi level will be reduced from the geometrical interfacial-layer thickness d_i to d_i' given by

$$d_i'=d_i-\Delta d_i. \quad (25)$$

Judging from the predicted 9–14-eV occupied depths E_{FM} of the metal conduction band for Ag, Au, and Al,[7,8] a representative choice for m_M is one-half of the free electron mass m_0. The corresponding Δd_i is 0.5 Å for a metal-vacuum interface, and 0.3 Å for a metal-GaAs interface. The actual barrier narrowing could be different by an amount that is probably less than these estimates themselves. Two opposing effects have been neglected. The first is a negative shift in the z position ($z=d_i$ in Fig. 4) of the effective image plane for an electron far removed from the metal (see Ref. 33, and references therein). The second is a positive shift of the z position where the electron energy becomes effectively zero ($z=d_i$ in Fig. 4), due to partial depletion of a thin metal surface layer (see, for instance, Fig. 1 of Ref. 34). Additional effects that occur for real atomic metals[33] are too complex to include in our simple model. To estimate the lowered barrier

$$E_B'=E_B-\Delta E_B, \quad (26)$$

we again apply Eq. (3-99) of Ref. 31, and use, as a uniformly lowered barrier E_B', the value calculated at the midpoint $z=(d_i-\Delta d_i)/2$. Thus, the barrier lowering is estimated as

$$\Delta E_B=E_{FM}+E_B-\frac{(E_{FM}+E_B)^2}{E_{FM}+E_B+\dfrac{q^2}{8\pi\varepsilon_i^{(\infty)}(d_i+\Delta d_i)}}. \quad (27)$$

Assuming a constant barrier (and barrier lowering) is reasonable,[34] particularly considering the uncertainties in parameter values. It allows us to integrate Eq. (15) directly, which is the second minor modification to Ref. 21.

In the third modification to Ref. 21, we allow for different electron effective mass in the metal (m_M), interfacial layer (m_i), and semiconductor ($m_{\rm sc}$). With the varying effective mass, we determine the metal wave function in the tunneling region by matching Ψ_M and $m^{-1}\partial\Psi_M/\partial z$ (Ref. 27) at the effective metal-barrier interface $z=d_i'=d_i-\Delta d_i$ (Fig. 4). The alternative WKB approach used in Ref. 21 for a constant mass would require the generalization described in Ref. 27 for position-dependent mass. With the wave-function matching approach, the metal wave-function tail in the tunneling layer is given by

$$\Psi_M=\left(\frac{2}{A_{xy}L_M}\right)^{1/2}\frac{m_i k_z}{\sqrt{m_M^2\eta_b^2+m_i^2k_z^2}}e^{-\eta_b(d_i'-z)}e^{i\mathbf{k}_{xy}\mathbf{r}_{xy}},$$
$$0<z\leq d_i'. \quad (28)$$

$\mathbf{k}_{xy}$ and k_z are related by Eq. (17), with $E=E_{FM}$ [Eq. (23)], i.e.,

$$k_{xy}^2+k_z^2=k_{FM}^2. \quad (29)$$

η_b is the interfacial layer decay factor:[21]

$$\eta_b(k_{xy})=\frac{1}{\hbar}\sqrt{2m_iE_B'+\hbar^2k_{xy}^2}. \quad (30)$$

$\mathbf{r}_{xy}$ is the transverse component of $\mathbf{r}$ in Fig. 4, i.e., the projection of $\mathbf{r}$ onto the xy plane. If the interfacial tunneling layer is not a vacuum ($m_i=m_0, X_i=0$), but instead is an oxide, or the semiconductor itself, the uncorrected barrier in Eq. (21) can be expressed in terms of the interfacial-layer conduction-band edge E_{Ci}, and the surface-state energy E_S:

$$E_B=E_{Ci}-E_S. \quad (31)$$

In the case of a semiconductor interfacial-layer barrier, the associated effective mass m_i for tunneling in the forbidden gap can be estimated from $\mathbf{k}\cdot\mathbf{p}$ theory[35] in terms of E_S and the valence-band edge E_{Vi}:

$$\frac{m_i}{m_0}=\frac{(E_S-E_{Vi})(E_S-E_{Vi}+\Delta)}{E_P(E_S-E_{Vi}+2\Delta/3)}. \quad (32)$$

This expression comes from Kane's secular equation for the three-band ''small-gap'' case. E_P is an interaction energy ($\approx$23 eV for III-V semiconductors), and Δ is the valence-band spin-orbit split at Γ (0.34 eV for GaAs). For a GaAs interfacial-layer tunneling barrier, with $E_B=E_C-E_S=0.85$ eV, the associated tunneling effective mass is $0.031m_0$. This is a very small value, about one-half of the conduction-band (Γ) effective mass [$m_e=0.067m_0$ (Ref. 36)]. It corresponds to a 6.3-Å characteristic distance $1/2\eta_b(0)$ for the radial exponential drop in electronic charge of the individual state. This is roughly consistent with the 2.8-Å one-dimensional decay length of MIGS ($d_{\rm MIGS}$) that results from averaging of the electronic charge parallel to the interface (Ref. 6, Fig. 13).

In Sec. IV C below, we will refer to the decay constant

$$\eta_s(0)=\frac{1}{\hbar}\sqrt{2m_{\rm sc}(E_C-E_S)} \quad (33)$$

of the surface-state wave function. This will describe the decay into the bulk of the semiconductor, beyond the tunneling barrier. $m_{\rm sc}$ is given by the right-hand side of Eq. (32), without the i subscript. For GaAs it turns out that $m_{\rm sc}$ is well approximated by a simple analytical parabolic continuation of the conduction band and the light hole valence band:

$$\frac{m_{\rm sc}}{m_0}=\frac{m_e}{m_0}\frac{m_{\rm lh}(E_S-E_V)}{m_{\rm lh}(E_S-E_V)+m_e(E_C-E_S)}. \quad (34)$$

With $\mathbf{k}\cdot\mathbf{p}$ theory as the basis, this is not surprising since the heavy hole valence band, to zeroth order, does not couple to the other bands in the ''small-gap'' approximation,[35] and the split-off valence band lies deeper. We will use Eq. (34) for the evanescent wave function in the semiconductor. This model for $m_{\rm sc}$ appears similar to the approach in Ref. 21, where the semiconductor decay constant was also expressed in terms of a parabolic continuation of the conduction band and a valence band into the band gap. However, there the two bands were assumed to have the same effective mass (the free electron mass m_0), and the approach led to a com-

plicated $\eta_s(k_{xy})$ dependence that we do not see, using the $\mathbf{k}\cdot\mathbf{p}$ result. If we apply Eq. (32) to the case of a typical oxide barrier ($E_{Ci}-E_S=4$ eV, $E_S-E_{Vi}=5$ eV, $E_g=9$ eV, $X_i=1$ eV), assuming that the interaction energy E_P is the same as for III-V semiconductors (23 eV) and that the spin-orbit splitting Δ is negligible, we predict $m_i=0.22m_0$. This is not dramatically different from the $0.29m_0$ used in Ref. 32, and by us in Sec. V, for Al_2O_3. Still, our approach is only approximate when we are dealing with a deep localized level whose wave function is made up of k vectors significantly larger than can be accounted for by a theory where higher order terms of $\mathbf{k}$ are neglected.

C. The surface-state wave function

We will take the integration surface S_{SM} in Eq. (20) to be a spherical shell, with radius a_S, around the surface state, outside the attractive core. We refer to Fig. 4, but initially consider the midgap state of energy E_S to be a bulk state. For this, we assume a spherically symmetric square-well potential[37] of short range $w_s/2$. This approximates the potential affecting an electron from an atomic core, screened by deeper-lying electrons. The potential is E_C for $r>w_s/2$. For $w_s/2<8$ Å, there will be no bound excited states for the semiconductors of interest. The ground state will be a spherically symmetric s-type state. We actually let a_s approach zero in order to integrate Eq. (20) analytically. This, in effect, requires that we assume a 3D δ-function potential. In this limit, the wave function has the simple form

$$\Psi_S=\left(\frac{\eta'_{ss}}{2\pi}\right)^{1/2}\frac{e^{-\eta r}}{r}, \tag{35}$$

where η is a decay constant and η'_{ss} is determined by normalization. For the spherically symmetric δ potential, η and η'_{ss} are equal to $\eta_s(0)$ in Eq. (33). However, a surface state is not spherically symmetrical, since it is adjacent to a potential barrier which is different than E_C-E_S. The wave function decays differently into the semiconductor and the tunneling barrier. We account for this approximately by introducing a θ dependence (Fig. 4) in the decay ''constant'' η in Eq. (35). We require that the δ potential produce a decay factor η that is equal to the appropriate decay constants for tunneling normal ($k_{xy}=0$) to the interface; i.e., $\eta=\eta_b(0)$ for $\theta=0$, and $\eta=\eta_s(0)$ for $\theta=\pi$. $\eta_b(0)$ is given by Eq. (30) above, with $k_{xy}=0$. With $\eta_{bo}\equiv\eta_b(0)$ and $\eta_{so}\equiv\eta_s(0)$, a functional form that satisfies these two requirements, and leads to an analytical solution, is

$$\eta(\theta)=\frac{\eta_{bo}+\eta_{so}}{2}+\frac{\eta_{bo}-\eta_{so}}{2}\cos(\theta). \tag{36}$$

The normalization constant η'_{ss} in Eq. (35) is now given in terms of the two decay constants on the right-hand side of Eq. (36):

$$\eta'_{ss}=\frac{\eta_{bo}-\eta_{so}}{\ln(\eta_{bo}/\eta_{so})}. \tag{37}$$

Note, as indicated in Fig. 4, that the surface-state wave-function decay is typically smaller in the semiconductor than in the barrier ($\eta_{so}<\eta_{bo}$). This works to reduce the tunneling.

D. Tunneling resistance and capture cross section

With the metal and surface-state wave functions in Secs. IV B and IV C, respectively, the tunneling matrix element M_{SM} [Eq. (20)] becomes

$$M_{SM}=-\hbar^2\left(\frac{4\pi\eta'_{ss}}{A_{xy}L_M}\right)^{1/2}\frac{k_{FM}}{\sqrt{(m_M\eta_{bo})^2+(m_ik_{FM})^2}}e^{-d'_i\eta_b(k_{xy})}, \tag{38}$$

where we have made use of the fact that the strongest dependence on $\mathbf{k}_{xy}$ occurs in the exponential factor by evaluating the prefactor at $\mathbf{k}_{xy}=\mathbf{0}$. The same approximation was made in Ref. 21, and it allows us to perform the integral in Eq. (15) analytically. Then, at zero temperature,

$$J_t=\frac{2q\hbar D_SE_{Fi}}{m_i{d'_i}^2}\frac{(m_M\eta'_{ss})(m_ik_{FM})}{(m_M\eta_{bo})^2+(m_ik_{FM})^2}\times(1+2d'_i\eta_{bo})e^{-2d'_i\eta_{bo}}. \tag{39}$$

The expression for the gate tunneling resistance [Eq. (8)] becomes

$$r_{\mathrm{IT}}=\frac{\delta E_{Fi}/q}{\delta J_t}=\frac{m_i{d'_i}^2}{2q^2\hbar D_S}\frac{(m_M\eta_b)^2+(m_ik_{FM})^2}{(m_M\eta'_{ss})(m_ik_{FM})}\frac{e^{2d'_i\eta_{bo}}}{1+2d'_i\eta_{bo}}. \tag{40}$$

In order to make a comparison meaningful between our approach and that in Ref. 21, we apply to the latter, the minor modifications mentioned above. We derive the following alternative expression for r_{IT}:

$$r_{\mathrm{IT}}^{(FD)}=\frac{m_i{d'_i}^2}{2q^2\hbar D_S}\frac{\pi\eta'_{ss}}{\sigma_T\eta_{bo}^2\eta_{ss}}\frac{(m_M\eta_{bo})^2+(m_ik_{FM})^2}{(m_M\eta'_{ss})(m_ik_{FM})}\times\frac{e^{2d'_i\eta_{bo}}}{1+2d'_i\eta_{bo}}. \tag{41}$$

This differs from Eq. (40) only in the second factor, where η_{ss} is determined by the semiconductor and interfacial-layer decay constants:[21]

$$\eta_{ss}=\frac{\eta_{bo}\eta_{so}}{\eta_{bo}+\eta_{so}} \tag{42}$$

(analogous to our η'_{ss}), and σ_T is the tunneling capture cross section for the surface state. σ_T was introduced phenomenologically in Ref. 21, independent of the tunneling problem. This was only natural in a theory where capture cross sections for Shockley-Read-Hall recombination at the oxide-semiconductor interface states play a central role. However, one is then faced with having to guess a value for σ_T before r_{IT} can be calculated. In the MOS cases modeled in Ref. 21 $\sigma_T=10^{-15}$–10^{-14} cm^2 were chosen.

In our theory, there is no independent cross section. The wave-function parameters, which are the result of our micro-

TABLE I. Interface parameters for the tunneling calculation, corresponding to five different models for Schottky-barrier formation on GaAs. Fixed parameters: $m_M=0.5m_0$, $n_M=6\times10^{22}$ cm^{-3}; $E_g=1.424$ eV, $X_{sc}=4.07$ eV, $\Phi_{B0}=0.85$ eV, $m_e=0.067m_0$, $m_{lh}=0.087m_0$, $d_{ML}=2.83$ Å, $c_D=0.45$ μF/cm^2.

Model	Vacuum IL [a]	Oxide IL [b]	MIGS [c]	AUDM [d]	DIGS [e]
X_i (eV)	0	0.95	4.12	4.07	4.07
m_i/m_0	1	0.29	0.031	0.031	0.031
$\varepsilon_i/\varepsilon_0$	1	9	13.1	13.1	13.1
$\varepsilon_i^{(\infty)}/\varepsilon_0$ [f]	1	2.99	13.3	13.3	13.3
d_i	4–5 Å	5–15 Å	$d_{TF}+d_{MIGS}=3.3$ Å	$(1–20)d_{ML}$	$(3–19)d_{ML}$
$\gamma=\dfrac{\partial\Phi_{B0}}{\partial\Phi_M}$	0.074	0.074	$\dfrac{1}{1+q^2D_S(d_{TF}/\varepsilon_0+d_{MIGS}/\varepsilon_{sc})}=0.13$		0.074
D_S	$\dfrac{\varepsilon_i}{q^2d_i}\left(\dfrac{1}{\gamma}-1\right)$	$\dfrac{\varepsilon_i}{q^2d_i}\left(\dfrac{1}{\gamma}-1\right)$	5×10^{14} cm^{-2}/eV	2.5×10^{14} cm^{-2}/eV	$\dfrac{\varepsilon_i}{q^2d_i}\left[\cosh^{-1}\left(\dfrac{1}{\gamma}\right)\right]^2$

[a]The Cowley-Sze vacuum interfacial-layer (IL) model (Refs. 3 and 4). Interfacial-layer thickness range as suggested in Ref. 3. Density of surface states calculated using the fitted sensitivity γ of barrier height Φ_{B0} on the metal work function Φ_M (Ref. 3).

[b]First alternative: The vacuum replaced, more realistically, with an unintentional oxide. Reasonable candidates are Ga and Al oxides. We use the effective mass and dielectric properties of Al_2O_3 (Ref. 32) and the affinity of SiO_2. A thickness range thought to be reasonable for an unintentional oxide is chosen.

[c]Second alternative: Based on numerical *ab initio* modeling of ideal intimate contact on GaAs(110) (Ref. 6). The tunneling barrier is primarily in the semiconductor. The values for X_i, m_i, ε_i, and $\varepsilon_i^{(\infty)}$ are thus those for GaAs; X_i increased by 0.05 eV to compensate for the slightly lower 0.8-eV Schottky-barrier height calculated in Ref. 6. The density of MIGS used is that calculated in Ref. 6.

[d]Third alternative: Based on numerical *ab initio* modeling of intimate contact on GaAs(110) with *bulklike* defects in monolayers near the interface (Ref. 8). The barrier is in the semiconductor. The value for D_S is the density of states calculated in Ref. 8 for the case of all the defects located in one monolayer, but is then distributed over the number of monolayers that the defects are spread over. This model is discussed in more detail in the text.

[e]Fourth alternative: Based on the disorder-induced gap state model (Refs. 15 and 16). For the tunneling analysis, this model is nearly indistinguishable from the AUDM case. We can use the experimental γ (Ref. 3) to calculate the volume density N_{DG} of DIGS by Eq. (3) in Ref. 15. D_S is then calculated as $N_{DG}d_i$, and spread over the number of monolayers as in the AUDM case.

[f]The square of the index of refraction.

scopic model for the surface state, lead directly to an analytical solution to the tunneling current. The accuracy of this solution is limited by how well the actual surface-state potential is approximated by a (θ-dependent) δ function. A more realistic potential with a nonzero range $w_s/2$ (Fig. 4) will lead to a smaller η'_{ss} than predicted by Eq. (37). This reduces the wave-function tail in the barrier region where the integral in Eq. (20) is taken, which increases the tunneling resistance. The two expressions for r_{IT} above, derived under otherwise identical assumptions, allow us to identify the value for σ_T that corresponds to our simple model for the surface state. This is of interest since it allows comparison with the large body of published experimental bulk cross sections. Setting the two Eqs. (40) and (41) equal requires that

$$\sigma_T=\frac{\pi}{\eta_{bo}^2}\frac{(\eta_{bo}/\eta_{so})^2-1}{(\eta_{bo}/\eta_{so})\ln(\eta_{bo}/\eta_{so})}. \tag{43}$$

Equation (43) expresses the interesting point that the tunneling cross section depends on the barrier. For typical nonspherical ($\eta_{bo}>\eta_{so}$) tunneling cases of interest, the cross section will be significantly (one to two orders of magnitude) lower than the corresponding cross section for the spherically symmetric bulk case ($\eta_{bo}=\eta_{so}$) given by

$$\sigma_T=\frac{2\pi}{\eta_{so}^2}\equiv\sigma_T^{(B)}. \tag{44}$$

With GaAs parameters, for a bulk trap located at 0.85 eV ($\approx\Phi_{B0}$) below the conduction band we get $\sigma_T^{(B)}=1.0\times10^{-13}$ cm^2. The experimental range for such traps is from about 10^{-14} to 10^{-11}.[38] Neglecting experimental errors, the wide range is due to the different, and basically unknown, bulk impurity potentials. If one assumes that the uncertainty in surface-state potential is equally large, one concludes that the predictions of r_{IT} in the next section could have error bars of ±2 orders of magnitude.

V. THEORETICAL ESTIMATES OF THE INTERFACIAL TUNNELING AND GATE RESISTANCES

We now apply the theory developed in Secs. III and IV by adapting the parameters to represent alternative pictures of Schottky-barrier formation. The most critical tunneling parameters describe the interfacial layer (IL) and its interface with the semiconductor. These parameters are varied, as shown in Table I, and explained in footnotes. The remaining parameters, those describing the metal and semiconductor, are fixed as shown in the first footnote. The resulting interfacial gate resistance at dc and at 50 GHz (the highest frequency available to us) is shown in Fig. 5.

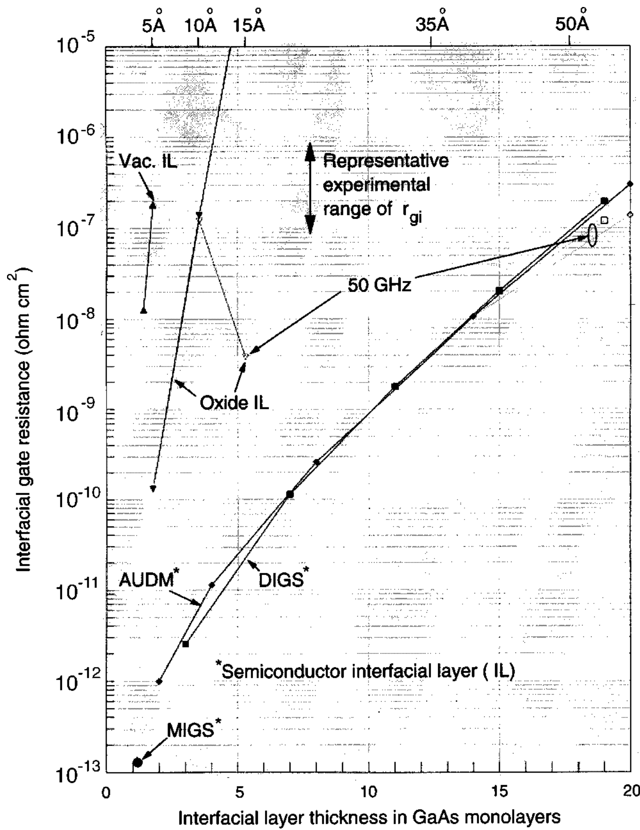

FIG. 5. Calculated interfacial gate resistance at dc (solid symbols) and 50 GHz (open symbols) versus interfacial-layer (IL) thickness for the five cases defined in Table I.

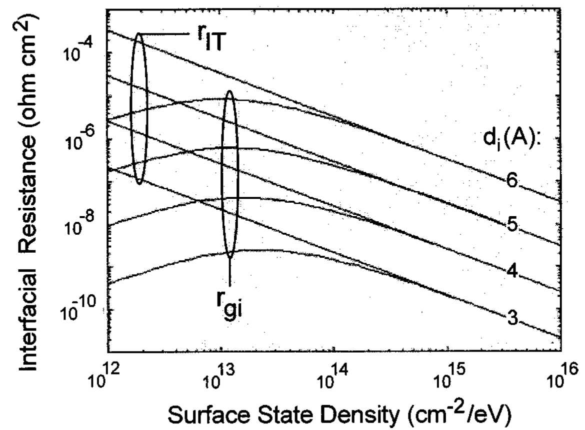

FIG. 6. Calculated interfacial tunneling and gate resistance versus surface-state density for a 3–6-Å range of interfacial-layer thickness. Cowley and Sze's vacuum picture (Refs. 3 and 4) is assumed with parameters given in Table I (except that the dependence of D_S on d_i is abandoned).

Cowley and Sze's vacuum picture, in the upper part of the 4–5-Å thickness range, leads to the observed values for the minimum interfacial gate resistance, and the observed lack of dispersion. The sensitivity to thickness is, however, particularly strong here because of the large intrinsic barrier (approximately equal to the metal work function) and interfacial-layer effective mass (equal to the free electron mass). The effect of including barrier lowering (and narrowing) is also particularly large, because of the low dielectric constant. The strong exponential dependence on interfacial-layer thickness is evident in Fig. 5, and also in Fig. 6 where we let d_i and D_S vary independently. Figure 6 shows r_{gi} and $r_{\rm IT}$ versus surface-state density for an interfacial-layer thickness range extended 1 Å above and below that suggested in Ref. 3. In the 10^{13}–10^{15}-cm^{-2}/eV D_S range, which should cover reasonable experimental conditions, r_{gi} varies less than the underlying $r_{\rm IT}$ because of Eq. (12). In fact, r_{gi} has a maximum at $D_S=\varepsilon_i/q^2d_i$ before it starts to approach zero as D_S approaches zero. In this ideal limit, the FET-degrading gate-resistance parameter r_{gi} approaches zero, even as $r_{\rm IT}$, for a finite d_i, approaches infinity.

A moderately thick oxide can also lead to predictions consistent with experiments as seen for the 10-Å case in Fig. 5. Thicker oxides, however, quickly approach the MOS case, where there is a very large (ideally infinite) tunneling resis-

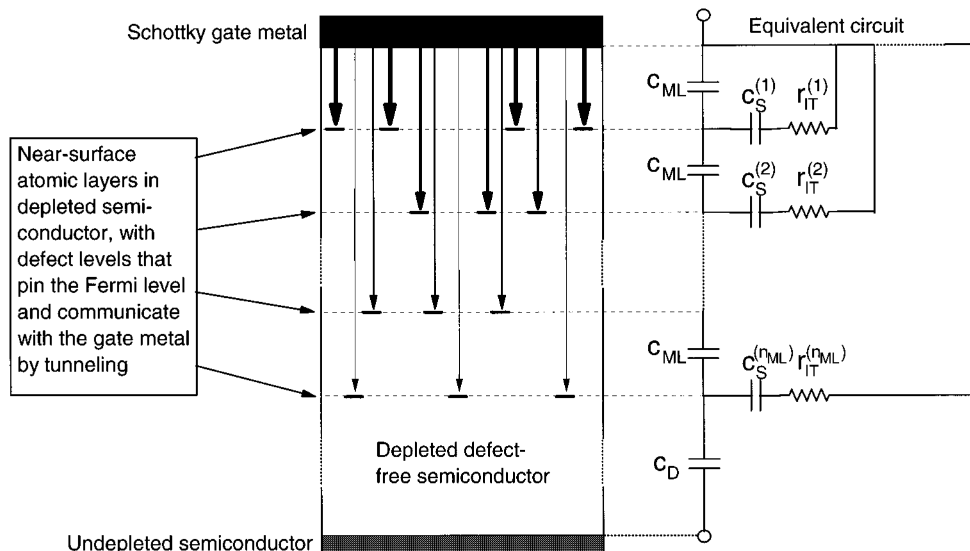

FIG. 7. Physical illustration and equivalent circuit for the case of tunneling between the metal gate and defects in the semiconductor near the interface. The metal and semiconductor are in intimate contact. The defects are located in equidistant monolayers of the semiconductor, and are thus no longer surface states.

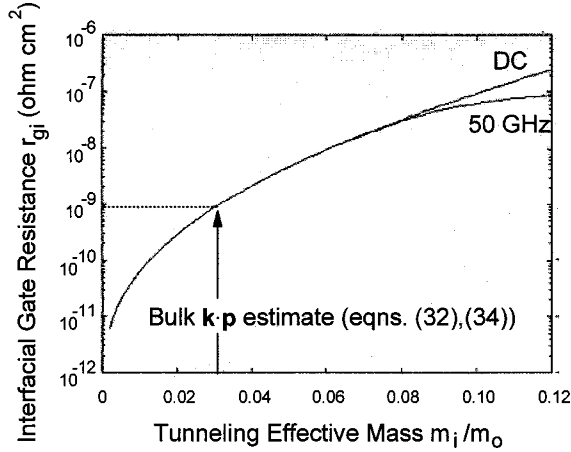

FIG. 8. Calculated interfacial gate resistance at dc and 50 GHz versus tunneling effective mass m_i for bulklike defects distributed over 10 monolayers.

tance, which does not degrade the FET performance since it is bypassed at very low frequencies. The large low-frequency value (off scale at 7.8×10^{-5} $\Omega\,\mathrm{cm}^2$) and dispersion for the 15-Å case in Fig. 5 are inconsistent with our experimental observations; for normal FETs r_{gi} is close to $r_{gi}^{(\min)}\approx3\times10^{-7}$ $\Omega\,\mathrm{cm}^2$ and there is little dispersion up to 50 GHz.[2] However, the larger average and experimental spread in r_{gi} in the earlier part of our process development (Ref. 2, Fig. 8) could very well have been due to an interfacial oxide and possibly organic residues. A III-V surface can be sensitive to even a small controlled exposure to oxygen,[13] and real device wafers in a fabrication environment get a significant amount of uncontrolled exposure. We have achieved $r_{gi}\approx3\times10^{-7}$ $\Omega\,\mathrm{cm}^2$ with reduced variability by (1) optimizing preevaporation cleanup dips, (2) minimizing evaporation delays, and (3) using sintered Pt gates.[5] Pt gates, annealed at 285 °C, are thought to form a uniform $PtAs_2$ layer beneath the original interface.[39] The $PtAs_2$-semiconductor interface may be as close to an ideal intimate metal-semiconductor Schottky contact as one can expect to get in a practical processing environment. Nevertheless, we have not been able to reduce r_{gi} further, even using thicker Pt, which results in deeper sintering, or using Pd.

The MIGS case in Table I and Fig. 5 represents the most ideal Schottky barrier physically conceivable. There is no physical barrier in this case. If we, however, still represent the situation with an interfacial layer, as was done in Ref. 6 to estimate γ [Eq. (14)], we can get an upper conceivable limit for r_{gi}. In Ref. 6 d_i/ε_i was replaced by $d_{\mathrm{TF}}/\varepsilon_0+d_{\mathrm{MIGS}}/\varepsilon_{\mathrm{sc}}$, where d_{TF} (=0.5 Å) is the Thomas-Fermi screening length, resulting in $\gamma=0.13$ for GaAs. This is larger than the 0.07 experimental value, but not by much considering the experimental uncertainties in γ, the use of an interfacial-layer representation of the intimate contact, and the use of jellium for the metal. For our upper-limit tunneling calculation we choose $d_i=d_{\mathrm{TF}}+d_{\mathrm{MIGS}}$ and $\varepsilon_i=\varepsilon_{\mathrm{sc}}$. The predicted value for r_{gi} in Fig. 5 is still exceedingly small, six orders of magnitude lower than our experimental observations, and three orders of magnitude smaller than an estimate for the negligible vertical metallic resistance associated with the 0.1-μm stem of the T gate.[2,5]

From the preceding results and discussion it might appear that there remains, in Schottky-barrier FETs and diodes produced in practical fabrication environments, even with sintered gates, a significant interfacial tunneling barrier. The gate resistance is too large to be reconciled with an ideal defect-free intimate metal-semiconductor contact, but it can be modeled by a thin oxide or a vacuum interfacial layer. The oxide picture is troublesome, however, in the context of sintered gates. The vacuum picture is unsatisfactory in that it is, by itself, unphysical. There is, however, a third alternative, denoted AUDM in Table I and Fig. 5. Here, the barrier is composed of metal in intimate contact with the semiconductor, as in the MIGS case, but with defects in the semiconductor near (and not just at) the interface. This is an important distinction for us, since these defects will truly act as terminal states for tunneling from the metal, with a nonzero barrier in the semiconductor itself. The original importance of the defects was that they could explain the experimentally observed insensitivity to the choice of metal of the Schottky-barrier height on GaAs. This was shown in Ref. 8 with a quantitative first-principles numerical model. It was also shown that the defect-free MIGS model cannot explain this important feature.[7,8] This may be somewhat surprising considering the good prediction of γ based on the interfacial-layer analysis above. However, other analyses have resulted in similar criticism of the MIGS model.[10,11] It may well be that an interfacial-layer representation fails quantitatively in the MIGS case.

In formulating the parameters that we put into our model to represent the AUDM case, we rely on Ref. 8. The physical picture of that work was based in spirit on the advanced unified defect model,[14] which is the reason we used AUDM to denote this case. A likely defect to be involved in Schottky-barrier formation on GaAs,[14] and the one used in Ref. 8, is the $\mathrm{As_{Ga}}$ antisite, which is believed to be the same as the deep donor EL2. The Schottky-barrier height and EL2 bulk binding energy are very similar. It is worth noting that the capture cross section of 10^{-13} cm^2 that we effectively use [Eq. (44)] is relatively close to the experimental values of 10^{-14}–10^{-12} cm^2 for this level.[38] In Ref. 8, all the EL2 defects were located in a monolayer at various distances from the interface. It was shown that, for proper pinning, the defects needed to be located in the second monolayer from the surface, or deeper. In reality, the defects will be spread over several monolayers. Although our Schottky barriers are formed on a (100) surface rather than the (110) surface used in Ref. 8, we use the surface-state density deduced from Ref. 8. In Ref. 8 the Ga atoms in the top atomic layer were replaced by metal atoms for energetic reasons. We will also assume that the first layer of metal atoms replaces Ga atoms, which corresponds to an entire atomic layer in our case.

To account in the tunneling analysis for the spatial distribution of the defect states, we generalize the dispersion analysis of Sec. III as illustrated in Fig. 7. The normalized admittance, with tunneling to n_{ML} layers, is given by the following set of expressions:

$$y^{(n_{\mathrm{ML}})}=\left(\frac{1}{j\omega c_D}+\frac{z_{n_{\mathrm{ML}}}}{1+q_{n_{\mathrm{ML}}}}\right)^{-1}, \tag{45}$$

$$z_k = r_{\mathrm{IT}}^{(k)} + \frac{1}{j\omega c_S^{(k)}}, \quad k=1,2,\ldots,n_{\mathrm{ML}} \tag{45a}$$

$$q_k = \frac{p_k}{1+\dfrac{p_{k-1}}{1+q_{k-1}}}, \quad q_0 \neq -1 \tag{45b}$$

$$p_k = j\omega c_{\mathrm{ML}} z_k, \quad p_0 = 0 \tag{45c}$$

where $r_{\mathrm{IT}}^{(k)}$ is the tunneling resistance to layer k, $c_S^{(k)} = q^2 D_S^{(k)}$ is the ''surface''-state capacitance associated with layer k, and $c_{\mathrm{ML}} = \varepsilon_{\mathrm{sc}}/d_{\mathrm{ML}}$ is the capacitance for a semiconductor monolayer thickness d_{ML}. In the present case we assume that all $D_S^{(k)}$ are equal, and are given by D_S/n_{ML}. The earlier Eq. (10) for tunneling to one layer of states is recovered by setting $n_{\mathrm{ML}}=1$ and $c_{\mathrm{ML}}=c_i$. We have ignored that the top capacitor in Fig. 7 is somewhat larger than the others because of the barrier narrowing ($\Delta d_i \approx 0.3$ Å $\approx 0.1 d_{\mathrm{ML}}$). The result for bulklike defects spread over n_{ML} monolayers, with n_{ML} between 2 and 20, is shown in Fig. 5.

A variation on this result is found for the disorder-induced gap states model.[15,16] As shown in Table I and Fig. 5, the outcome is essentially identical to the AUDM case. This is not too surprising since in both cases the tunneling is through the semiconductor to bulklike defects. The DIGS theory, however, contains an analytic connection between γ and D_S (Table I) which we use in calculating the associated value of r_{gi}. For both the DIGS and AUDM models, the predicted interfacial gate resistance is quite close to the experimental values for defect depths of 15–20 monolayers. It is worth recalling that the curves of Fig. 5 are subject to a variety of uncertainties which may move the curves up or down by an order of magnitude. For example, an actual deep level may confine more of the wave function to the attractive core potential, leading to a smaller value of η'_{ss} in Eq. (35) or of capture cross section, and to a larger value of r_{IT}. Of course, the effective cross section $\sigma_T^{(B)}$ is close enough to experimental values for EL2 that this source of variation should not be more than an order of magnitude. The dependence on D_S is qualitatively similar to that shown in Fig. 6 for the Cowley-Sze vacuum picture. r_{gi} peaks quite near $D_S = 10^{14}$ cm^{-2}/eV. An order-of-magnitude variation in r_{gi} would require more than an order of magnitude change in D_S and could only decrease r_{gi}. The sensitivity to a variation in the metal effective mass is also rather weak; in a typical case a factor of 2 change from the nominal $m_M = 0.5 m_0$ changes r_{gi} only by 25%. However, if the tunneling effective mass were larger or smaller than the original estimate of $0.031 m_0$ [Eq. (34)] the r_{gi} curve would move up or down considerably. Figure 8 shows the effect for the realistic intermediate case of a semiconductor barrier with bulklike defects spread over the first 10 monolayers (28 Å). A moderate increase of m_i to $0.06 m_0$ increases the predicted r_{gi} from 10^{-9} to 10^{-8} Ω cm^2, with negligible increase in dispersion. The defect model is attractive in that it can, with physically reasonable adjustments in parameter values from their ''nominal,'' get quite close to predicting the experimentally observed interfacial gate resistance. Deep penetration of defects leads to larger dispersion, as seen in Fig. 5. This may be the reason that we occasionally observe FETs with large r_{gi} and dispersion.

VI. CONCLUSION

We have analyzed theoretically, by analytical modeling, the interfacial gate resistance component that has recently been shown to exist and to dominate in short-gate microwave and millimeter-wave Schottky-barrier-gate field-effect transistors. We focused on what appears experimentally to be a lower practical bound of this parameter. This resistance is conceptually and quantitatively well explained by electron tunneling between metal and semiconductor surface states. A MOS-like admittance analysis showed that what in principle is a rather complex frequency dependence can be captured by the standard gate-resistance component in the FET equivalent circuit up to very high frequencies. Of course, the magnitude and scaling of this interfacial gate resistance is very different from the conventional gate metallization access resistance, which has several important consequences.[2] We developed an analytical tunneling model and showed that the value and low level of dispersion, of the lower limit of the interfacial gate resistance is in quantitative agreement with Cowley and Sze's static band lineup model for Schottky-barrier formation. Our predictions are also consistent with more physically appealing models involving near-surface crystal imperfections. However, the interfacial resistance of Schottky barriers on practical III-V FETs appears to be inconsistent with the idealized picture of a perfect metal-semiconductor interface as contained in the MIGS model.

ACKNOWLEDGMENT

We are grateful to Professor Patrick Roblin for enlightening discussions.

---

*Present address: Hewlett-Packard Wireless Semiconductor Division, San Jose, CA 95131.

[1] H. Rohdin, A. Nagy, V. Robbins, C.-Y. Su, C. Madden, A. Wakita, J. Raggio, and J. Seeger, *Proceedings of the 7th International Conference on InP and Related Materials* (IEEE, Piscataway, 1995), p. 73.

[2] H. Rohdin, N. Moll, C.-Y. Su, and G. S. Lee, IEEE Trans. Electron Devices **45**, 2407 (1998).

[3] A. M. Cowley and S. M. Sze, J. Appl. Phys. **36**, 3212 (1965).

[4] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York, 1981), pp. 270–279.

[5] H. Rohdin, A. Nagy, V. Robbins, C.-Y. Su, A. S. Wakita, J. Seeger, T. Hwang, P. Chye, P. E. Gregory, S. R. Bahl, F. G. Kellert, L. G. Studebaker, D. C. D'Avanzo, and S. Johnsen, Hewlett-Packard J. **49**, 37 (1998).

[6] S. G. Louie, J. R. Chelikowsky, and M. L. Cohen, J. Vac. Sci. Technol. **13**, 790 (1976).

[7] M. van Schilfgaarde and N. Newman, Phys. Rev. Lett. **65**, 2728 (1990).

[8] M. van Schilfgaarde and N. Newman, J. Vac. Sci. Technol. B **9**, 2140 (1991).
[9] J. Tersoff, Phys. Rev. Lett. **52**, 465 (1984).
[10] C. B. Duke and C. Mailhiot, J. Vac. Sci. Technol. B **3**, 1170 (1985).
[11] W. A. Harrison, J. Vac. Sci. Technol. B **3**, 1231 (1985).
[12] L. J. Brillson, Surf. Sci. **299/300**, 909 (1994).
[13] W. E. Spicer, I. Lindau, P. Skeath, and C.-Y. Su, J. Vac. Sci. Technol. **17**, 1019 (1980).
[14] W. E. Spicer, Z. Liliental-Weber, E. Weber, N. Newman, T. Kendelewicz, R. Cao, C. McCants, P. Mahowald, K. Miyano, and I. Lindau, J. Vac. Sci. Technol. B **6**, 1245 (1988).
[15] H. Hasegawa, *Proceedings of the 18th International Conference on the Physics of Semiconductors* (World Scientific, Singapore, 1987), Vol. 1, p. 291.
[16] H. Hasegawa and H. Ohno, J. Vac. Sci. Technol. B **4**, 1130 (1986).
[17] W. Mönch, Surf. Sci. **299/300**, 928 (1994).
[18] R. Ludeke, G. Jezequel, and A. Taleb-Ibrahimi, J. Vac. Sci. Technol. B **6**, 1277 (1988).
[19] J. L. Freeouf and J. M. Woodall, Appl. Phys. Lett. **39**, 727 (1981).
[20] J. L. Freeouf, J. M. Woodall, L. J. Brillson, and R. E. Viturro, Appl. Phys. Lett. **56**, 69 (1990).
[21] L. B. Freeman and W. E. Dahlke, Solid-State Electron. **13**, 1483 (1970).
[22] P. Muret and A. Deneuville, J. Appl. Phys. **53**, 6289 (1982).
[23] Y.-S. Lou and C.-Y. Wu, IEEE Trans. Electron Devices **41**, 558 (1994).
[24] G. Gomila and J. M. Rubi, J. Appl. Phys. **81**, 2674 (1997).
[25] P. Cova, A. Singh, and R. A. Masut, J. Appl. Phys. **82**, 5217 (1997).
[26] L. M. Terman, Solid-State Electron. **5**, 285 (1962).
[27] W. A. Harrison, Phys. Rev. **123**, 85 (1961).
[28] J. Bardeen, Phys. Rev. Lett. **6**, 57 (1961).
[29] A. M. Bratkovsky, Appl. Phys. Lett. **72**, 2334 (1998).
[30] *CRC Handbook of Chemistry and Physics*, edited by D. R. Lide and H. P. R. Fredrikse (CRC Press, Boca Raton, 1997), pp. 12-124.
[31] J. S. Blakemore, *Solid State Physics*, 2nd ed. (Cambridge University Press, Cambridge, England, 1985), pp. 192 and 193.
[32] R. Stratton, J. Phys. Chem. Solids **23**, 1177 (1962).
[33] M. Garcia-Hernandez, P. S. Bagus, and F. Illas, Surf. Sci. **409**, 69 (1998).
[34] G. Binnig, N. Garcia, H. Rohrer, J. M. Soler, and F. Flores, Phys. Rev. B **30**, 4816 (1984).
[35] E. O. Kane, in *Semiconductors and Semimetals*, edited by R. K. Willardson and A. C. Beer (Academic, New York, 1966), Vol. 1, p. 75.
[36] S. Adachi, J. Appl. Phys. **58**, R1 (1985).
[37] L. I. Schiff, *Quantum Mechanics*, 3rd ed. (McGraw-Hill, New York, 1968), p. 83.
[38] G. M. Martin, A. Mitonneau, and A. Mircea, Electron. Lett. **13**, 191 (1977).
[39] N. Harada, S. Kuroda, and K. Hikosaka, IEICE Trans. Electron. **E75-C**, 1165 (1992).