Theoretical and experimental study of the quasistatic capacitance of metal-insulator–hydrogenated amorphous silicon structures: Strong evidence for the defect-pool model

J. P. Kleider and F. Dayoub
Laboratoire de Génie Electrique de Paris (CNRS, URA 0127), Ecole Supérieure d'Electricité, Universités Paris VI et Paris XI, Plateau de Moulon, 91192 Gif-sur-Yvette Cedex, France
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The density of localized states in hydrogenated amorphous silicon (a-Si:H) is studied by means of the quasistatic capacitance technique applied to metal-insulator a-Si:H structures. Calculations in the framework of the defect-pool model show that the changes in the quasistatic capacitance versus gate bias curves (qs-CV curves) after bias annealing reveal the changes in the density of dangling-bond states predicted by the model, and are sensitive to the defect-pool parameters. The comparison of theoretical qs-CV curves with experimental curves obtained in a wide range of bias-anneal voltages V_{ba} on several kinds of structures (top gate oxide, top gate nitride, and the most commonly used bottom gate nitride structures) strongly support the defect-pool model, and values for the model parameters are deduced. It is shown that for all structures the dominant phenomenon for bias annealing at positive V_{ba} (i.e., under electron accumulation) is the creation of defects in the lower part of the gap in the a-Si:H. Bias annealing under hole accumulation reveals the creation of defects in the upper part of the gap of a-Si:H, but the precise dependence of the qs-CV curves upon V_{ba} depends on the nature of the insulator–a-Si:H interface. In particular, it is affected by a higher density of interface trap levels in the top gate nitride structures, and by hole injection and trapping from the a-Si:H into the nitride layer in the bottom gate nitride structures. [S0163-1829(98)03040-9]

I. INTRODUCTION

The defect pool model has been attracting much attention for several years, since it gives a coherent picture of the formation and equilibration of silicon dangling bonds in hydrogenated amorphous silicon (a-Si:H). The basic idea is that silicon dangling bonds can form at different energies in potential defect sites (the defect pool) from the breaking of silicon-silicon weak bonds characterized by the valence-band tail.[1–5] Several microscopic reactions with different contributions of the hydrogen atoms have been studied, but they all lead to rather similar expressions of the density of states (DOS) due to dangling bonds.[6–16] The major feature of this DOS is the dependence upon the Fermi level, which is due to the minimization of the free energy of the system. In particular, it is found that dangling bonds form at energies below midgap if the Fermi level is close to the conduction band, whereas they form in the upper part of the gap if the Fermi level lies closer to the valence band. This dependence upon the Fermi level is of critical importance when considering field-effect devices, wherein the position of the Fermi level relatively to the band edges can be controlled by applying a gate bias.

The metastability of a-Si:H thin-film transistors (TFT's), which is essentially characterized by shifts of the threshold voltage, has thus been explained by the modification of the DOS in a-Si:H in the framework of the defect-pool model.[17,18] However, threshold voltage shifts can also be produced by charge trapping into the insulator.[19–21] In addition, the subthreshold slope of TFT's, that depends on the DOS in the semiconductor near the interface with the insulator, also strongly depends on the interface state density at the rear interface (i.e., the interface between the semiconductor and the substrate) because the active semiconductor layer is very thin in TFT's in order to avoid high access and contact resistances.[22,23] These drawbacks can be avoided by using the quasistatic capacitance of metal-insulator–semiconductor (MIS) structures. Indeed, in MIS structures the a-Si:H layer can be made much thicker than in TFT's, since the quasistatic capacitance does not depend on the resistance of the semiconductor. Furthermore, the curve of the quasistatic capacitance as a function of the gate bias (qs-CV) of MIS structures is known to reflect the shape of the interface trap density in the case of crystalline semiconductors. In a recent paper, we extended the study of the quasistatic capacitance of MIS structures to the case of amorphous semiconductors, and showed that a simple treatment of the qs-CV data can be used to derive the variation of the DOS as a function of the energy.[24] However, this simple treatment might not be used if the semiconductor is nonhomogeneous. Therefore, we developed a computer modeling to calculate the qs-CV curves in the framework of the defect pool model, and demonstrated that the quasistatic capacitance still remains a powerful tool to study the defects in the a-Si:H layer, the shape of the qs-CV curve providing an image of the DOS near the insulator/semiconductor (I/S) interface. Preliminary results of thermal bias-annealing experiments on aluminum/silicon dioxide (SiO_2)/a-Si:H top gate structures, in agreement with the defect-pool model, were obtained.[25] In this paper, we extend the theoretical study of the quasistatic capacitance in the framework of the defect-pool model, and add a lot of experimental data obtained on both top gate and bottom gate a-Si:H structures having different I/S interfaces.

In Sec. II, we expose the theoretical bases of the calculation of the quasistatic capacitance, taking into account the defect-pool DOS. We also detail the influence of the model parameters on the theoretical qs-CV curves. In Sec. III we present the different kinds of structures used in this study as well as the experimental quasistatic capacitance data obtained in a wide range of thermal annealing biases. Finally, in Sec. IV, we discuss all these experimental results. The comparison with the theoretical predictions strongly supports the defect-pool model, and allows one to quantify the effect of interface trap level density and charge injection into the insulator on these different structures.

II. MODELING OF THE QUASISTATIC CAPACITANCE IN THE FRAMEWORK OF THE DEFECT-POOL MODEL

The basis of the quasistatic capacitance calculation consists in the resolution of Poisson's equation, taking into account the specific DOS given by the defect-pool model. We shall consider the problem one dimensional, and assume that all quantities of interest vary only in the direction perpendicular to the I/S interface, the origin of the abscissa x being taken at the interface. This assumption is fully justified owing to the geometry of the studied structures.

A. Determination of theoretical qs-CV curves

The calculation is performed in two steps. In the first step, corresponding to the thermal bias annealing, the DOS is calculated in the whole semiconductor layer according to the bias annealing conditions (temperature and gate voltage). Then, in the second step, this DOS is assumed frozen in, and the quasistatic capacitance is calculated as a function of the gate bias.

1. Thermal bias-annealing step

In this step the MIS structure is supposed to be under thermal bias-annealing conditions, i.e., at a temperature T_{ba} higher than the defect equilibration critical temperature T_{cr} which is of the order of 180–200 °C in undoped a-Si:H.[26–28] The gate voltage applied during this step, that determines the dangling-bond defect distribution in the semiconductor layer through the induced band bending, will be called in the following the bias-anneal voltage (V_{ba}). To obtain both the defect distribution and the band bending, one must solve Poisson's equation, which is written as

$$\frac{d[\varepsilon\xi(x)]}{dx}=\rho(x), \tag{1}$$

where $\xi(x)$ is the electric field at the abscissa x, ε is the dielectric permittivity and $\rho(x)$ the charge density at x that contains three contributions: free carriers

$$\rho_{fc}(x)=q[p(x)-n(x)], \tag{2}$$

where $p(x)$ and $n(x)$ are the densities of free holes and free electrons, respectively, and q is the absolute value of the electron charge; band tails

$$\rho_{bt}(x)=q\int_{E_v(x)}^{E_c(x)}N_{vbt}(E)[1-f(E)]dE - q\int_{E_v(x)}^{E_c(x)}N_{cbt}(E)f(E)dE, \tag{3}$$

where $N_{\mathrm{vbt}}(E)$ and $N_{\mathrm{cbt}}(E)$ are the densities of states in the valence-band tail and in the conduction-band tail, respectively, and $f(E)$ is the probability of a tail state being occupied by an electron, that will be taken equal to the equilibrium Fermi-Dirac function; and deep defects

$$\rho_{dd}(x)=q\int_{E_v(x)}^{E_c(x)}D(E)[f^{+}(E)-f^{-}(E)]dE, \tag{4}$$

where $D(E)$ is the density of dangling-bond (DB) states at the energy E, i.e., the density of DB states having a ''ground level'' corresponding to the transition between unoccupied and singly occupied at E, and $f^{+}(E)$ and $f^{-}(E)$ are the probabilities of such a DB being occupied by zero or two electrons, respectively. The thermal equilibrium distribution functions $f(E), f^{+}(E), f^{0}(E)$ (corresponding to a singly occupied dangling bond), and $f^{-}(E)$ are given by

$$f(E)=\frac{1}{1+\exp\left(\frac{E-E_F}{kT}\right)}, \tag{5}$$

$$f^{+}(E)=\frac{1}{1+2\exp\left(\frac{E_F-E}{kT}\right)+\exp\left(\frac{2E_F-2E-U}{kT}\right)},$$

$$f^{0}(E)=2\exp\left(\frac{E_F-E}{kT}\right)f^{+}(E),$$

$$f^{-}(E)=\exp\left(\frac{2E_F-2E-U}{kT}\right)f^{+}(E), \tag{6}$$

where E_F is the Fermi level, k the Boltzmann constant, T the temperature, and U the correlation energy of the amphoteric dangling-bond states.

The particularity of $D(E)$ in the defect-pool model is that it depends on the Fermi-level position. In order to take this dependence into account, we used the expression of $D(E)$ given by Powell and Deane[13]

$$D(E)=\gamma\left(\frac{2}{f^{0}(E)}\right)^{\beta(kT_{\mathrm{ba}}/E_{v0})}P\left(E+\frac{\beta\sigma^2}{E_{v0}}\right), \tag{7}$$

where

$$\beta=\frac{E_{v0}}{E_{v0}+kT_{\mathrm{ba}}}, \tag{8}$$

and

$$\gamma=H\left(\frac{2E_{v0}}{2E_{v0}-kT_{\mathrm{ba}}}\frac{N_{v0}E_{v0}}{H}\right)^{\beta}\exp\left[\frac{-\beta}{E_{v0}}\left(E_p-E_v-\frac{\beta\sigma^2}{2E_{v0}}\right)\right]. \tag{9}$$

In these expressions, E_{v0} is the characteristic width of the valence-band tail, N_{v0} is the DOS at the valence-band edge,

H is the hydrogen concentration, and $P(E)$ is the defect formation probability at the energy E, which is assumed to be a Gaussian distribution centered at E_p with a characteristic width σ. Other expressions of $D(E)$ given either by Schumm,[15] or Powell and Deane,[16] have also been tested. Similar results can be obtained by allowing for some slight changes in the defect-pool parameters, and we therefore present only the results obtained using the defect-pool DOS given by Eq. (7). We note that the DOS depends on the Fermi level through $f^0(E)$.

Introducing the electrostatic potential $V(x)$,

$$\frac{dV(x)}{dx} = -\xi(x), \tag{10}$$

and taking into account that $(E_F - E_v)(x)$ is simply shifted from $qV(x)$ by a constant value, we obtain from Eqs. (1)–(4) the second order one-dimensional equation

$$\frac{d^2(E_F-E_v)}{dx^2} = -\frac{q^2}{\varepsilon}\left[p(x)-n(x)+\int_{E_v(x)}^{E_c(x)}\{N_{vbt}(E)[1-f(E)]-N_{cbt}(E)f(E)+D(E)[f^+(E)-f^-(E)]\}dE\right]. \tag{11}$$

Two boundary conditions are needed to obtain the solution $(E_F - E_v)(x)$ of Eq. (11). For the first one, we assume that the value of $(E_F - E_v)$ at the rear interface ($x = L_s$) is the intrinsic bulk value, that has been taken equal to 1.05 eV in a-Si:H. It is worth noticing that we consider a-Si:H layers thick enough (typically $L_s > 6000$ Å) so that the semiconductor can reach bulk equilibrium properties far from the I/S interface. Then we can assume that the rear electrode at $x = L_s$ provides an Ohmic contact, neglecting the existence of a possible band bending at this interface (that can be due, for instance, to a Schottky-type back electrode or to the presence of a thin doped layer). We have checked that this latter assumption has no consequence on the final results for the values of L_s we are dealing with.

The second boundary condition is related to the bias-anneal voltage $V_{\rm ba}$ applied between the gate and rear electrodes:

$$V_{\rm ba} = \Delta\Phi_{MS} - \frac{\tilde{Q}_i}{C_i} - \frac{A\sigma_{\rm int}}{C_i} + \frac{(E_F-E_v)(0)}{q} - \frac{(E_F-E_v)(L_s)}{q} - \frac{\varepsilon_s L_i}{q\varepsilon_i}\left[\frac{d(E_F-E_v)}{dx}\right]_{(x=0)}, \tag{12}$$

where $\Delta\Phi_{MS}$ is the work-function difference between the gate metal and the a-Si:H layer, C_i is the insulator capacitance, ε_i is the insulator dielectric permittivity, L_i is the insulator thickness, L_s is the a-Si:H layer thickness, and A is the area of the MIS structure. $\sigma_{\rm int}$ is the areal density of charge at the I/S interface due to interface states, that depends on the Fermi-level position $(E_F - E_v)(0)$ at this interface, and $\tilde{Q}_i$ is an effective fixed charge in the insulator, that does not depend on $(E_F - E_v)(0)$ and that can be written

$$\tilde{Q}_i = Q_i + \frac{A}{L_i}\int_{-L_i}^{0} x\rho_i(x)dx, \tag{13}$$

where Q_i and $\rho_i(x)$ are the total charge and the charge density in the insulator, respectively.

The solution of Eq. (11) is then obtained using a numerical finite-difference method and an iterative procedure, since $D(E)$ itself depends on the band bending and therefore must be accommodated. Figure 1(a) shows an example of the band bending obtained at 200 °C under electron accumulation using the ''standard'' defect-pool parameters of Table I. In Fig. 1(b) we present the corresponding DOS calculated from Eq. (7) as a function of both the energy (referred to the valence band edge E_v) and the abscissa x. It is clearly observed that the DOS is highly nonhomogeneous, and varies rapidly near the I/S interface due to the band bending, with a bump appearing in the lower part of the gap. This kind of nonhomogeneous DOS was already emphasized by Powell and Deane.[29] Figure 2(a) shows an example of band bending in

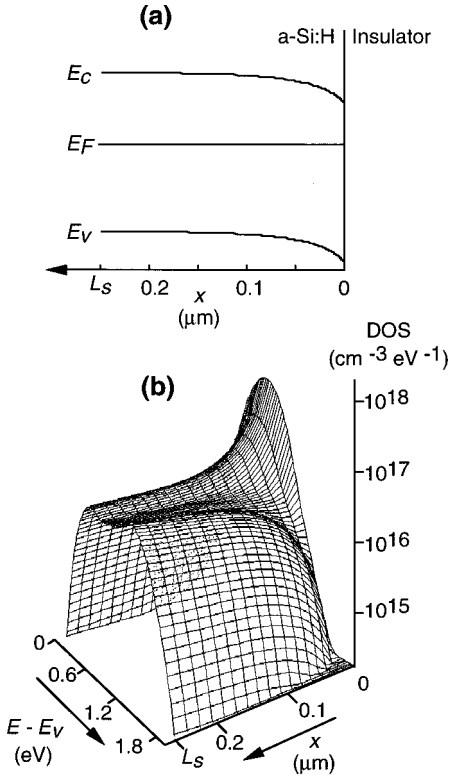

FIG. 1. Example of (a) band bending and (b) density-of-states (DOS) profile in the a-Si:H layer obtained in the framework of the defect-pool model if the layer equilibrates under electron accumulation.

TABLE I. Values of the defect-pool parameters used in the simulation of the quasistatic capacitance curves; E_{v0} and E_{c0} are the characteristic widths of the valence- and conduction-band tails, respectively, σ is the characteristic width of the defect pool, E_p-E_v is the position of the pool maximum referred to the valence-band edge, E_G is the gap energy, and U is the correlation energy of the dangling bond states. For all calculations, we used values of the density of states at the valence- and conduction-band edge equal to 2×10^{21} and 1×10^{21} cm^{-3} eV^{-1}, respectively, and the hydrogen content [H] was equal to 5×10^{21} cm^{-3}. The values in the column ''standard'' were found by Deane and Powell from modeling of the threshold voltage shift of TFT's (see Ref. 13), and are used to illustrate the theoretical calculations (Figs. 1–5). The values given in the other columns are those giving the best fit to the experimental qs-CV curves obtained on the structures studied in this work, namely, top gate silicon dioxide (TG-SiO_2), top gate silicon nitride (TG-SiN_x), and two different bottom gate silicon nitride (BG1-SiN_x and BG2-SiN_x) structures. Also reported in the last line is the value of the effective areal charge density in the insulator used in the calculations; this is directly related to the flatband voltage in the structures.

Parameters	Standard	TG-SiO_2	TG-SiN_x	BG1-SiN_x	BG2-SiN_x
E_{v0} (eV)	0.056	0.05	0.05	0.05	0.048
E_{c0} (eV)	0.028	0.03	0.03	0.025	0.03
σ (eV)	0.178	0.157	0.157	0.157	0.155
E_p-E_v (eV)	1.27	1.16	1.16	1.06	1.16
E_G (eV)	1.9	1.8	1.8	1.7	1.8
U (eV)	0.2	0.15	0.15	0.15	0.15
$\tilde{\sigma}_i$ (C cm^{-2})	-	4.8×10^{-8}	6.1×10^{-8}	3.6×10^{-7}	7.7×10^{-8}

the a-Si:H layer obtained at 200 °C under hole accumulation, and the corresponding DOS is presented in Fig. 2(b). Again, the DOS is highly nonhomogeneous, but the DOS maximum near the I/S interface now appears in the upper part of the gap.

2. Quasistatic capacitance calculation

The DOS calculated in the preceding step is assumed to be frozen in. As will be seen in the experimental details, the quasistatic capacitance measurements are performed at a temperature below the critical temperature of a-Si:H, so that the DOS cannot be changed during acquisition of the qs-CV data.

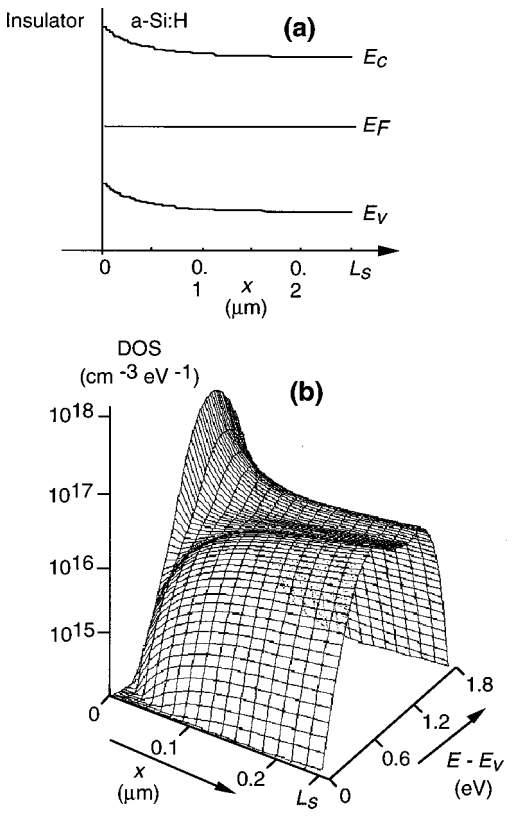

FIG. 2. Example of (a) band bending and (b) density-of-states (DOS) profile in the a-Si:H layer obtained in the framework of the defect-pool model if the layer equilibrates under hole accumulation.

The theoretical qs-CV curve is then obtained by calculating the variation with the applied gate voltage V_G of the total charge Q_T in the MIS structure. The quasistatic capacitance C at a given gate voltage V_G is then given by

$$C(V_G)=-\frac{dQ_T}{dV_G}. \tag{14}$$

Q_T is expressed as

$$Q_T=Q_i+A\sigma_{\rm int}+A\int_0^{L_s}\rho(x)dx. \tag{15}$$

Thus, in order to calculate Q_T for a given value of V_G, we must once again solve Poisson's equation with the same boundary conditions as in the preceding step, except that $D(E,x)$ no longer depends on the applied voltage, and $V_{\rm ba}$ has to be replaced with V_G in Eq. (12).

B. Discussion of theoretical qs-CV curves

1. Evolution of the qs-CV curves with the bias-anneal voltage

The evolution of the qs-CV curves with the bias-anneal voltage has already been discussed in a previous rapid communication.[25] Here we just briefly recall the main arguments.

First, it has to be recalled that in the framework of the defect-pool model the changes that can be observed in the qs-CV curve (after changing the bias-annealing voltage) reflect the changes in the one-electron density of states close to the I/S interface. The one-electron DOS $N_{\rm DB}(E)$ due to the dangling bonds is defined from the density $D(E)$ as $N_{\rm DB}(E)=D[E+kT\ \ln(2)]+D[E-U-kT\ln(2)]$.[13] The total one-electron DOS, taking all states (dangling bonds and conduction- and valence-band tails) into account is thus given by

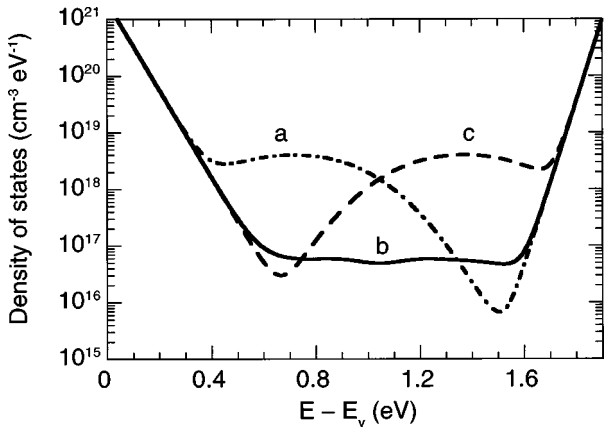

FIG. 3. One-electron density of states in the a-Si:H layer at the insulator/a-Si:H interface after equilibration under (a) electron accumulation, (b) flatband conditions, and (c) hole accumulation. This was calculated using the standard defect-pool parameters of Table I.

$$g(E)=D[E+kT\ \ln(2)]+D[E-U-kT\ \ln(2)]+N_{\mathrm{vbt}}(E)+N_{\mathrm{cbt}}(E). \tag{16}$$

Figure 3 presents the one-electron DOS at the I/S interface after three different bias annealings corresponding to (a) electron accumulation, (b) flatbands, and (c) hole accumulation. Figure 4 shows the corresponding qs-CV curves. In this figure, as well as for all qs-CV curves presented in the following, the quasistatic capacitance values are normalized to the insulator capacitance C_i. For Figs. 4 and 5, we took $C_i = 39\ \mathrm{nF\ cm^{-2}}$, and the values of $\Delta\Phi_{MS}$ and $\tilde{Q}_i$ were such that the flatband voltage V_{fb} (which is the bias-anneal voltage producing flatband during annealing) was equal to -1.7 V. The defect-pool parameters used in the calculation are the ''standard'' values given in Table I. Cases (a) and (c) were calculated at bias-anneal voltages symmetric with respect to V_{fb}, for which the corresponding interface Fermi levels during annealing were also symmetric with respect to the intrinsic Fermi level E_{Fi}. Therefore, according to the model, defects form at different energies and the peak energies in the one-electron DOS are symmetric with respect to E_{Fi}, which is visible in Fig. 3 (where we have $E_{Fi}-E_v=1.05$ eV).

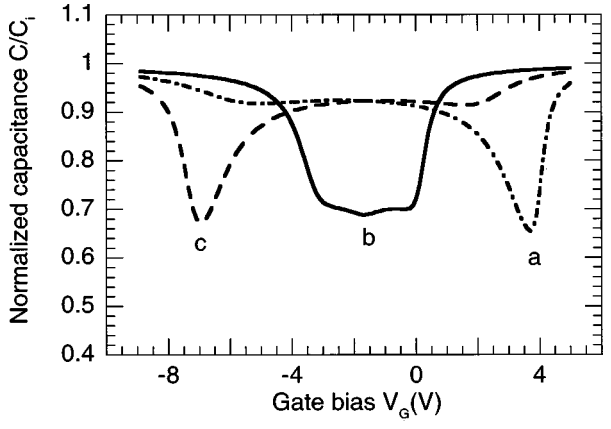

FIG. 4. Normalized quasistatic capacitance C/C_i as a function of the gate bias V_G calculated at $T=353$ K after bias annealing at $T=473$ K under (a) electron accumulation, (b) flatband conditions, and (c) hole accumulation calculated with the standard defect-pool parameters of Table I, no interface states, and a flatband voltage $V_{\mathrm{fb}}=-1.7$ V. The corresponding one-electron DOS at the insulator/a-Si:H interface is shown in Fig. 3.

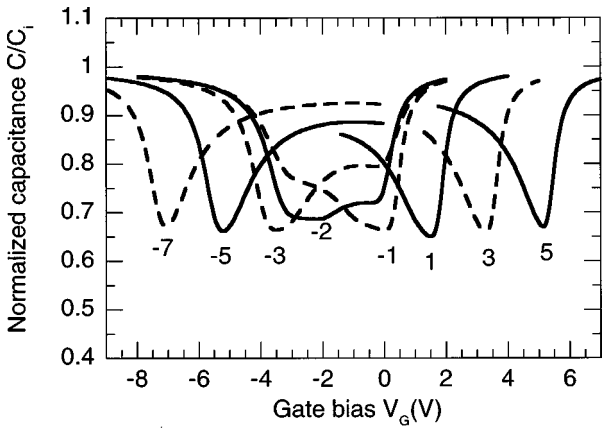

FIG. 5. Theoretical normalized quasistatic capacitance C/C_i as a function of the gate bias V_G calculated at $T=353$ K using the same parameters as in Fig. 1, after bias annealing at $T=473$ K under various bias-anneal voltages. The curves are labeled according to the bias-anneal voltage. They are shown, alternately, by plain and dashed lines, and only parts of the whole curves are shown for the sake of clarity.

The comparison of Figs. 3 and 4 emphasizes that there is a strong correspondence between the qs-CV curves and the one-electron DOS near the I/S interface. In particular, the relatively flat one-electron DOS in case (b) is reflected in the qs-CV curves in a well-defined capacitance minimum plateau. For (a) and (c) we always observe two minima in the total one-electron DOS, at the intercept of the one-electron DOS due to the dangling bonds $N_{\mathrm{DB}}(E)$ with the conduction- and valence-band tails, respectively. Following a thermal annealing under moderate electron accumulation, the DOS related to dangling bonds increases below midgap and decreases above midgap. Therefore, the minimum in the upper part of the gap is very sharp, while the minimum in the lower part of the gap is much higher. This results in a well-defined capacitance minimum in the qs-CV curve that will be called the conduction-band-tail (CBT) minimum, and in a secondary capacitance minimum called the valence-band-tail (VBT) minimum, that is much broader and corresponds to C/C_i values quite close to one due to the high value of the DOS at this minimum. Following a thermal annealing under moderate hole accumulation, the DOS minimum in the upper part of the gap is much higher than the one in the lower part of the gap. As a consequence, the CBT minimum in the qs-CV curve becomes broad with a high C/C_i value, while the VBT minimum is sharp and becomes the main one.

We would like to comment here on the correspondence between the one-electron DOS and the qs-CV curve. It is well known that for MIS structures on *crystalline* semiconductors, the quasistatic capacitance probes interface states, and there is a correspondence between the probed energy and the gate voltage.[30] Indeed, the capacitance is essentially sensitive to the states located at the interface Fermi level. Therefore, changing the gate bias changes the position of the interface Fermi level within the band gap, and thus allows

interface trap level spectroscopy to be performed. The correspondence between the probed energy and the gate voltage was proposed by Berglund,[31]

$$E-E_0=q(\psi_s-\psi_{s0})=q\int_{V_{G0}}^{V_G}\left[1-\frac{C}{C_i}\right]dV_G, \qquad (17)$$

where E is the energy of the states probed at the gate voltage V_G corresponding to the band bending $\psi_s=V(0)-V(L_s)$. V_{G0} is an initial gate voltage corresponding to ψ_{s0} and E_0. For MIS structures on *homogeneous amorphous* semiconductors, assuming that interface states give a negligible contribution compared to bulk states, we showed that it is still possible to relate the quasistatic capacitance to the DOS using (i) Eq. (17) for the correspondence between gate voltage and probed energy, and (ii) a formula somewhat more complicated than in the crystalline case.[24] In particular the DOS at a given energy is not simply related to the capacitance as in the crystalline case but also to the derivative and the integral of the capacitance with respect to and over the gate voltage, respectively, that account for the fact that the states are distributed in the whole semiconductor layer and not only at the interface. Concerning MIS structures on *amorphous* semiconductors in the framework of the *defect-pool model*, localized states are distributed in the whole semiconductor layer, but not uniformly. The fact that defects are created close to the interface [see Figs. 1(b) and 2(b)] makes the situation intermediate between that of an ideal homogeneous amorphous semiconductor (homogeneous density of states in the bulk) and that of an ideal crystalline semiconductor (no states in the bulk and only at the interface) MIS structures. This explains the strong correspondence between the shape of the qs-CV curve and that of the one-electron DOS at the insulator interface. Therefore, the most specific feature of the defect-pool model, namely, that the mean defect energy level changes when the defect is created in different charge states following thermal annealing under either electron or hole accumulation, is well reflected in the changes of the shape of the qs-CV curve. Comparing cases (a) and (c) in Fig. 3, there is a symmetry of the one-electron density of dangling-bond states close to the interface which is reflected in the symmetry of the corresponding qs-CV curves.

In Fig. 5 are presented the theoretical qs-CV curves corresponding to a larger set of bias-anneal voltages V_{ba}, in order to emphasize the changes in these curves due to changes in V_{ba}. For $V_{ba}>-1$ V and $V_{ba}<-3$ V, only the part of the curve around the main minimum is shown for the sake of clarity, the secondary minimum having C/C_i values becoming quite close to 1. As indicated above, the flatband voltage V_{fb} was equal to -1.7 V. This is why the main capacitance minimum flips from the VBT one for $V_{ba}<-1.7$ V, to the CBT one for $V_{ba}>-1.7$ V. In addition, qs-CV curves calculated for bias-anneal voltages symmetric with respect to $V_{fb}=-1.7$ V also appear symmetric with respect to V_{fb}, reflecting the symmetry of the one-electron density of dangling-bond states at the interface with respect to the intrinsic Fermi level. Obviously, this is a specificity of the defect-pool model. If the energy of the created defects did not change from $V_{ba}>V_{fb}$ to $V_{ba}<V_{fb}$, such a flip between the CBT and VBT minima would not occur, and the qs-CV curves would not exhibit such a symmetrical change around V_{fb}.

For $V_{ba}>V_{fb}$, we mainly observe a small decrease of the CBT minimum value as the bias-anneal voltage is increased up to 1 V, and then, for $V_{ba}>1$ V, the value of the CBT minimum increases. In addition, the position V_{min} of the CBT minimum shifts towards higher values. The variation of the CBT minimum value reflects the evolution of the value of the DOS minimum at the intercept between $N_{DB}(E)$ and $N_{cbt}(E)$. Indeed, for -1.7 V$<V_{ba}<1$ V, this minimum DOS value decreases as V_{ba} increases, due to the decrease of $N_{DB}(E)$ in the upper part of the gap. For $V_{ba}>1$ V, though the Gaussian distribution of dangling-bond states peaked above midgap (at $E=E_p$) decreases, the increase of the Gaussian distribution of dangling-bond states peaked below midgap is such that the whole one-electron density of states due to the dangling bonds $N_{DB}(E)$ increases whatever the energy, resulting in an increase of the CBT minimum. The positive shift of V_{min} can be explained as follows. The applied bias can be related to the charges Q_{int} and Q_S at the I/S interface and in the semiconductor, respectively, and to the effective charge $\tilde{Q}_i$ in the insulator through

$$V_G=\Delta\Phi_{MS}-\frac{\tilde{Q}_i}{C_i}-\frac{Q_{int}}{C_i}-\frac{Q_S}{C_i}+\psi_s, \qquad (18)$$

For the curves of Figs. 4 and 5, we did not involve specific interface states in our calculation, so that $Q_{int}=0$. In addition, $\Delta\Phi_{MS}$ and $\tilde{Q}_i$ are independent of the bias-anneal voltage. Therefore, the variation ΔV_{min} of the position of the CBT minimum from one curve to another can be simply written as

$$\Delta V_{min}=-\frac{(\Delta Q_S)_{min}}{C_i}+(\Delta\psi_s)_{min}, \qquad (19)$$

where $(\Delta Q_S)_{min}$ is the variation in the semiconductor charge, and $(\Delta\psi_s)_{min}$ the variation in surface band bending at the CBT minimum. In the qs-CV curve, the CBT minimum occurs when the Fermi level close to the I/S interface is swept through the minimum of the total one-electron DOS $g(E)$. This means that if one compares two curves corresponding to $\Delta V_{ba}>0$, $(\Delta\psi_s)_{min}$ is quite small because the energy position of the DOS minimum changes only a little bit, but $(\Delta Q_S)_{min}$ has quite a large negative value, due to the created dangling-bond states that are almost all negatively charged for $V_G=V_{min}$. The positive shift of the CBT minimum as V_{ba} increases is therefore explained by the increase of a negative charge in the semiconductor due to the created dangling bonds.

The same kinds of remarks can be done for the evolution of the VBT minimum for decreasing values of V_{ba} below V_{fb}. The value of the VBT minimum first slightly decreases, then slightly increases. This reflects first a decrease, then an increase, of the DOS minimum at the intercept of the valence-band tail with the dangling-bond states distribution. In addition, the position V_{min} of the VBT minimum shifts toward negative values as V_{ba} becomes more negative, related to an increasing positive charge in the semiconductor

due to the created dangling bonds that are positively charged when the qs-CV curve goes through the VBT minimum.

2. Effect of the defect-pool parameters on the evolution of the qs-CV curve

The features described above are quite general, and do not depend on specific values for the defect-pool parameters. However, the intensities of both the shifts of the capacitance minima position and the variations of the capacitance minima values depend on these parameters, because these parameters determine the dependence of the density of dangling-bond states on the Fermi-level position.

In order to study the influence of the defect-pool parameters, namely, E_p, σ, U, and E_{v0}, we changed the values of each parameter around the standard value in Table I, the other parameters being kept constant, and we looked at the evolution of the qs-CV curves with V_{ba}. One of the most important feature when looking at a set of qs-CV curves corresponding to different bias-anneal voltages is the positive shift of the CBT minimum $V_{\min}$ for increasing values of the positive bias-anneal voltage. This shift is equivalent to that of the TFT's threshold voltage, and has been clearly identified for all our MIS structures (see Sec. III). Another characteristic evolution is that of the corresponding minimum capacitance value $C_{\min}$. Therefore, the influence of the defect-pool parameters will be studied through the influence on $V_{\min}$ and $C_{\min}$. As an illustration, Fig. 6 shows the dependence of $V_{\min}$ and $C_{\min}$ for different values of the pool maximum E_p. We observe that $V_{\min}$ always increases with V_{ba}, whereas $C_{\min}/C_i$ slightly decreases and then increases with V_{ba} whatever the value of E_p. However, the quantitative changes are quite sensitive to this value.

To simplify the study of the parameter influence, we consider a range of V_{ba} where both $V_{\min}$ and $C_{\min}/C_i$ increase with V_{ba} (typically for $V_{\mathrm{ba}}>V_{\mathrm{fb}}+2$ V), and characterize the curves by the mean values of the slopes $s_V=dV_{\min}/dV_{\mathrm{ba}}$ and $s_C=d(C_{\min}/C_i)/dV_{\mathrm{ba}}$. From a systematic study of the role of each parameter, we came to the conclusion that s_V and s_C only depend on E_{v0} and on a combination of the other parameters that will be called Δ_i, representing the difference between the intrinsic Fermi level E_{Fi} of a-Si:H and midgap. Using the formula giving E_{Fi},[13] we can write

$$\Delta_i=E_p-E_v+\frac{U}{2}-\frac{\beta\sigma^2}{E_{v0}}-\frac{E_G}{2}. \tag{20}$$

As an illustration, Fig. 7 shows the dependence of $V_{\min}$ and $C_{\min}/C_i$ for a given value of E_{v0} and four different sets of the other parameters, giving the same value of Δ_i. We observe that the $V_{\min}$ vs V_{ba} curves are practically identical, while the $C_{\min}/C_i$ vs V_{ba} curves are only separated by a constant value, the slope s_C being the same.

Figure 8 shows the dependence of s_V and s_C on E_{v0}. Since changing E_{v0} also changes Δ_i, we chose to change the parameters (E_G, E_p-E_v, σ, and U) in order to maintain the same value of Δ_i (equal to 0.143 eV) for all values of E_{v0}. We observe that increasing E_{v0} results in an increase of s_V and in a decrease of s_C.

Similarly, Fig. 9 shows the dependence of s_V and s_C on Δ_i, E_{v0} being set at 0.056 eV. We observe that s_V is close to 1 and only slightly depends on Δ_i for $\Delta_i<0.1$ eV. For $\Delta_i>0.1$ eV, s_V rapidly decreases if Δ_i increases. s_C increases with Δ_i in the whole range, but the increase is more pronounced for $\Delta_i<0.1$ eV.

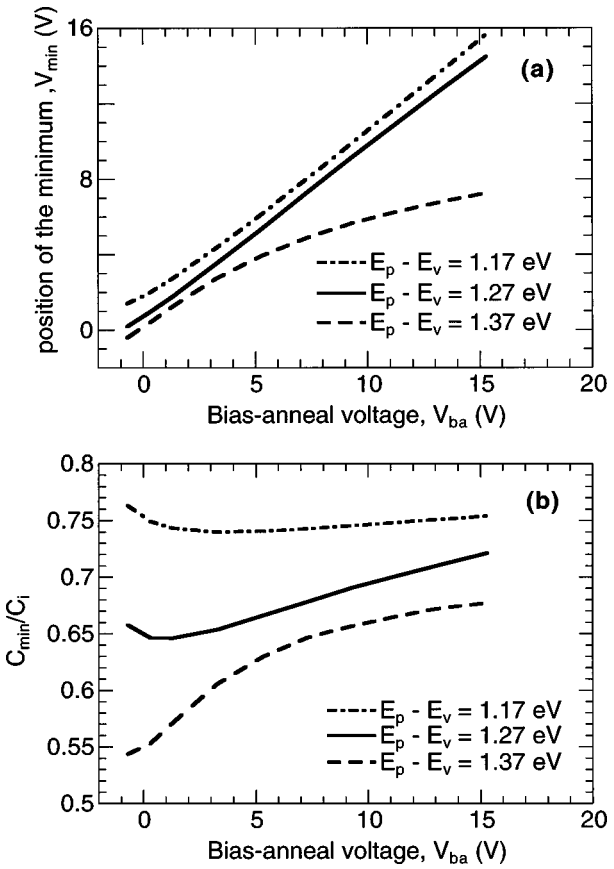

FIG. 6. Variations with the positive bias-anneal voltage (corresponding to bias annealing under electron accumulation) of (a) the position of the minimum capacitance, and (b) the value of the normalized quasistatic minimum capacitance value, for three different values of the position E_p-E_v of the pool maximum. The value of the other defect-pool parameters are the standard values in Table I.

In conclusion of the study of the influence of the defect-pool parameters on the evolution of the qs-CV curves after positive bias annealing, we want to stress several points that will be very helpful to determine the parameters giving the best fits to our experimental data, as discussed in Sec. IV. First, it is not possible to increase s_V without decreasing s_C. Second, if one can find two values for Δ_i and E_{v0} that reproduce the evolution of s_C and s_V, the choice of the defect-pool parameters is *a priori* not unique, since different values of E_G, E_p-E_v, σ, and U can give the same value of Δ_i. The choice of these parameters is then adjusted according to the absolute value of $C_{\min}$ that strongly depends on it. The choice of the parameters is further tested from the qs-CV curve obtained after bias annealing under flatband conditions. Indeed, it is known that the qs-CV curves should exhibit quite a wide minimum plateau after annealing under flatband conditions. Since the DOS is quite flat and homogeneous after such annealing, there is a direct relation between the constant DOS value g and the value of the capacitance C at the plateau,[24]

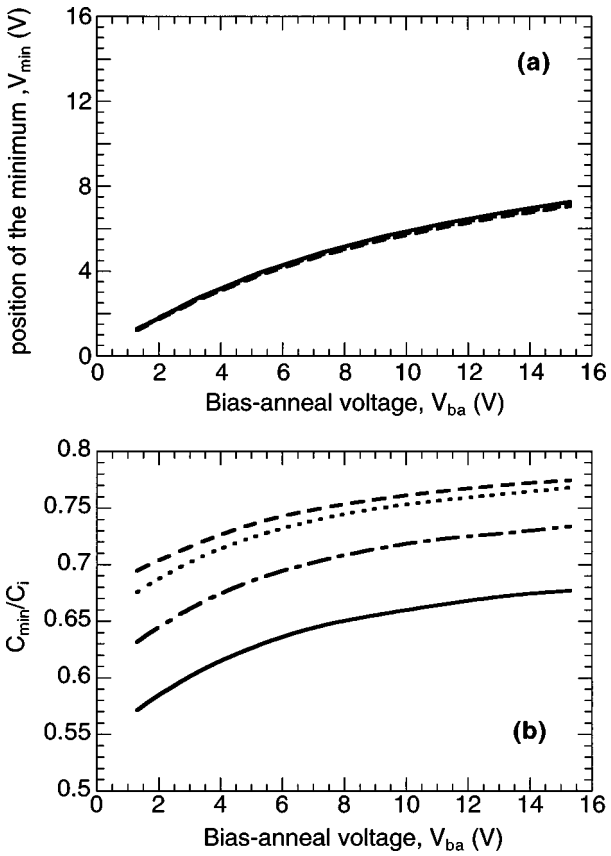

FIG. 7. Variations with the positive bias-anneal voltage (corresponding to bias annealing under electron accumulation) of (a) the position of the minimum capacitance, and (b) the value of the normalized quasistatic minimum capacitance value for four different sets of defect-pool parameters such that E_{v0} and Δ_i are kept constant. The parameters that have been changed are for the curves in dashed lines, $E_G=1.7$ eV; dotted lines, $E_G=1.7$ eV and $U=0.3$ eV; dashed-dotted lines, $\sigma=0.148$ eV; and solid lines, $E_p-E_v=1.37$ eV. The values of the other parameters are those given in Table I.

$$g=\frac{1}{\varepsilon q^2 A^2}\left(\frac{C}{1-C/C_i}\right)^2. \tag{21}$$

Given the value of Δ_i and E_{v0}, this can be used to obtain the value E_p-E_v, σ and U. Finally, the same set of parameters must also fit the behavior of the qs-CV curves after bias annealing under hole accumulation ($V_{\rm ba}<V_{\rm fb}$).

III. EXPERIMENT

A. MIS structures

The studied structures are sketched in Fig. 10. Four different a-Si:H MIS structures have been studied. Two are top gate (TG) structures, meaning that the a-Si:H layer has been deposited first, followed by the insulator layer and the metal gate electrode, while the two others are bottom gate structures, the a-Si:H layer being deposited after the insulator, that has itself been deposited on top of the metal gate electrode.

Two TG structures differing by the nature of the insulator have been deposited on a Corning 7059 glass substrate covered with ITO. For both structures, two layers of n^+a-Si:H (40 Å thick) and intrinsic a-Si:H (1 μm thick) were deposited at France Telecom CNET laboratory in a hot wall rf (13.56 MHz) glow discharge plasma-enhanced chemical-vapor deposition (PECVD) system at a substrate temperature of 200 °C, and a pressure of 50 Pa. Then, for the first type of structure (that will be denoted TG-SiO_2 in the following), a high-quality distributed electron cyclotron resonance (DECR)-PECVD silicon dioxide layer was deposited at 100 °C at Thomson-CSF research laboratory, while for the second type of structure (that will be denoted TG-SiN_x in the following) a standard PECVD silicon nitride layer was deposited at CNET. Finally, to form the gate electrode, a 3000-Å-thick aluminum layer was evaporated through a mask, thus defining 1-mm-diameter circular dots. More details on the deposition conditions can be found elsewhere.[23,32] Note that the thickness of these silicon dioxide and silicon nitride layers (800 and 1000 Å, respectively) were chosen such as to yield approximately the same value for C_i. This ensures a direct comparison of the normalized qs-CV curves. Since both TG structures have the same a-Si:H layer, the comparison of the results obtained on these structures will be used to identify the contribution of the bulk a-Si:H material and that of the states specific to the interfaces formed by a-Si:H with the DECR SiO_2 and SiN_x in the top gate configuration.

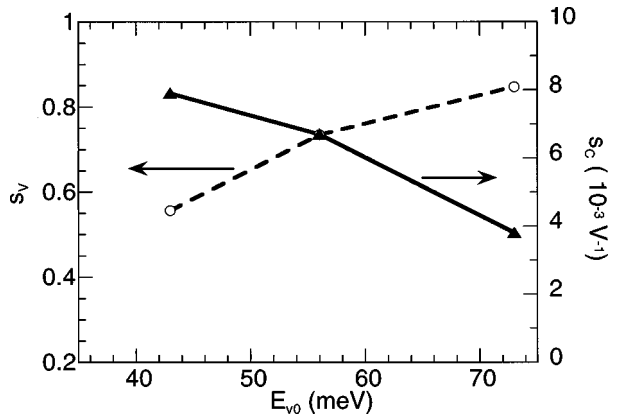

FIG. 8. Variations of s_V and s_C as functions of the characteristic width of the valence-band tail E_{v0}. The value of Δ_i is kept constant, equal to 0.143 eV.

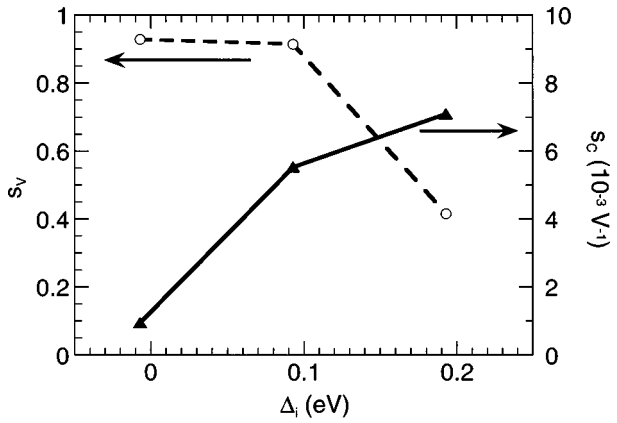

FIG. 9. Variations of s_V and s_C as functions of the characteristic parameter Δ_i. The characteristic width of the valence-band tail E_{v0} is kept constant, equal to 0.056 eV.

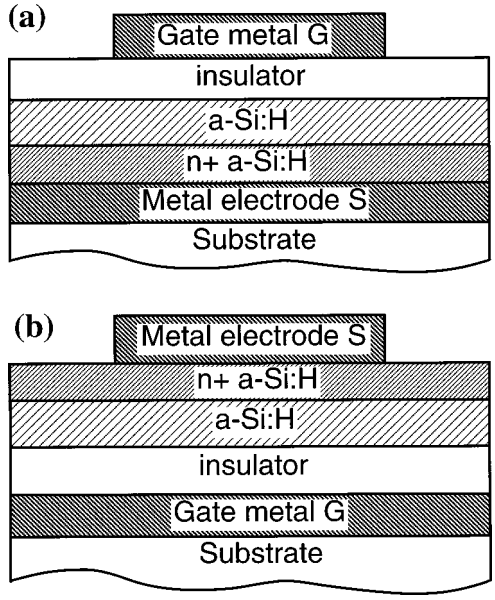

FIG. 10. Sketch of (a) top gate, and (b) bottom gate MIS structures studied in this work.

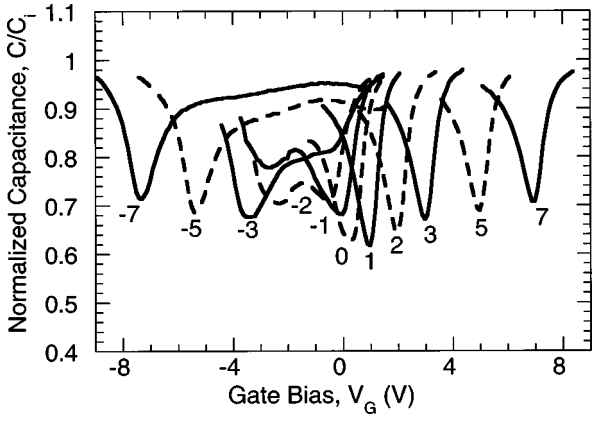

FIG. 11. Experimental normalized quasistatic capacitance C/C_i measured at $T=353$ K on the silicon dioxide top gate structure (TG-SiO_2) as a function of the gate bias V_G after bias annealing at $T=473$ K under different bias-anneal voltages. The curves are labeled according to the bias-anneal voltage. They are shown, alternately, by plain and dashed lines, and only parts of the whole curves are shown for the sake of clarity.

Both bottom gate (BG) structures use PECVD silicon nitride as the insulator. The first one (that will be denoted BG1-SiN_x in the following) was fabricated at Philips Research Laboratories on a chromium covered glass substrate forming the gate electrode. A 500-Å-thick layer of silicon nitride was deposited by PECVD, followed by a 0.2-μm-thick layer of intrinsic a-Si:H and a 400-Å-thick layer of n^+ a-Si:H, both also deposited by PECVD. Then a 3000-Å-thick layer of aluminum was deposited and etched to form 0.5-mm-diameter circular source electrodes. The second one (that will be denoted BG2-SiN_x in the following) was fabricated at Balzers Process Systems on a clean p-type crystalline silicon wafer that acts as the gate electrode, and the thicknesses of the silicon nitride, undoped a-Si:H and n^+ a-Si:H layers (all deposited by PECVD) were 1000 Å, 0.6 μm, and 400 Å, respectively. Finally, a 3000-Å-thick Al layer was deposited and patterned to form 1-mm-side-square electrodes. The comparison of the results obtained on the silicon nitride top gate and bottom gate structures will help to discuss the influence of the deposition order on the SiN_x/a-Si:H interface characteristics.

B. Experimental procedure

This consists of subsequent thermal bias annealing and quasistatic capacitance measurements steps. The thermal bias anneal and quasistatic capacitance measurement temperatures were equal to $T_{ba}=200$ °C and $T_m=80$ °C, respectively. Before any bias-annealing treatment, each MIS diode to be studied was first annealed under short circuit conditions for about 1 h at 200 °C, and then cooled down to 80 °C, where a first series of measurements provided the initial qs-CV curve of the sample.

For each value of the bias-anneal voltage V_{ba}, the equilibration of the sample was tested in two ways. First, during bias annealing, we measured the current flowing through the structure, and the bias-annealing conditions were maintained until this current was found to saturate. Typically, the duration of this bias-annealing step ranged between 20 mn and 5 h. Second, after cooling down to 80 °C and acquisition of a first qs-CV curve, the sample was bias annealed again at the same V_{ba} value, cooled down again at T_m, and a second qs-CV curve was obtained. By comparing both curves we verified that they were the same within 5% (which is typically the experimental error that can be estimated from both capacitance and temperature measurements) and, consequently, that defect equilibration was effectively reached.

After each sequence of thermal bias annealing and measurement steps, the sample was annealed under short-circuit conditions at 200 °C for 12 h. By determining a subsequent qs-CV curve, we checked that this long annealing under short circuit allowed one to restore the initial state.

The measurement temperature of 80 °C was a good tradeoff between lower temperatures, where the increase of time response of deep states makes the determination of the true quasistatic capacitance both longer and more influenced by leakage currents, and higher temperatures where partial reequilibration during measurements can become significant. For the results presented in the following we checked that this last effect was negligible by successively determining two qs-CV curves for increasing and decreasing values of the gate bias, respectively, which were identical.

C. Experimental results

In this section we present and discuss the effect of thermal bias annealing on the quasistatic capacitance for each structure, and in Sec. IV we shall separate the behavior after positive bias annealing, corresponding to $V_{ba}>0$, from that obtained under negative bias annealing, corresponding to $V_{ba}<0$.

The qs-CV curves obtained on the TG SiO_2 structure are presented in Fig. 11. As already indicated previously,[25] these results are quite well explained in the framework of the defect-pool model. Indeed, as far as the results after positive bias annealing are concerned, the qs-CV curves present a well-defined minimum similar to that observed on the calcu-

lated qs-CV curves (see, for instance, Fig. 5). Increasing V_{ba} results in a positive shift of the position of the minimum along with an increase of the minimum value, but the overall shape of the qs-CV curve is not strongly modified. Conversely, negative bias annealing can completely modify the shape of the qs-CV curve. Indeed, considering the minimum observed on the curve obtained at $V_{ba}=0V$, we observe that this minimum increases when V_{ba} changes from -1 to -3 V. In the same time, we observe the appearance of another minimum, the value of which decreases rapidly so that it becomes the main minimum for $V_{ba}\leqslant -3$ V. By comparing with the theoretical trends observed in Fig. 5, we identify these two minima with the CBT and VBT minima, respectively. When changing the bias-anneal voltage from -1 to -3 V, we thus observe that the main minimum flips from the CBT to the VBT minimum, the other one increasing due to an increase of created dangling bonds in the upper part of the gap. This evolution is experimental evidence of what is predicted by the defect-pool model when, during thermal bias annealing, the structure goes from electron accumulation ($V_{ba}=-1$ V) to hole accumulation ($V_{ba}=-3$ V), because defects are not formed at the same energy.[13] If defects were formed at the same energy, such a flip between the CBT and VBT minima would not occur. For an intermediate bias-anneal value, $V_{ba}\approx -2$ V, the structure is annealed under flatband conditions. Under such conditions, the Fermi-level position is the same throughout the a-Si:H layer, meaning that the DOS is uniform and quite flat. Therefore, the corresponding qs-CV curve should also exhibit a rather flat minimum plateau. Indeed, the qs-CV curve obtained for $V_{ba}=-2$ V clearly exhibits both minima at approximately the same level, and the capacitance values between these two minima (where the quasistatic capacitance probes the states around midgap) are at their lowest level, compared to the curves obtained at higher or lower bias-anneal voltages. The flatband voltage for this structure can thus be clearly identified at $V_{fb}\approx -2$ V. However, we observe a small bump between the two minima. This can be attributed to interface states, as described in Sec. IV. In addition, such a negative value for V_{fb} implies that there is a small positive charge in the insulator, of the order of 4×10^{-8} C cm^{-2} (see Sec. IV).

If one further decreases the bias-anneal voltage ($V_{ba}\leqslant -5V$), we observe that the main minimum, i.e., the VBT minimum, shifts to more negative gate voltages, and that its value slightly increases (just like the CBT minimum slightly increases and shifts to more positive gate voltages if V_{ba} is increased above 1 V). As explained in Sec. II B, this behavior is predicted by the defect-pool model due to the creation of dangling bonds in the upper part of the gap.

In summary, all the main features of the experimental qs-CV curves are well predicted by the defect-pool model. This also means that specific interface states at the SiO_2/a-Si:H interface play a minor role in the behavior of this structure after bias annealing. Their density is small enough so that the contribution of the dangling bonds in a-Si:H in the vicinity of the interface is predominant, whatever the energy and whatever the bias-anneal voltage.

We now turn to the results obtained on the structures having silicon nitride as an insulator. We first examine the results obtained on the top gate SiN structure, because this structure has exactly the same a-Si:H layer as the TG SiO_2 structure. The qs-CV curves obtained for different values of the bias-anneal voltage are shown in Fig. 12. Comparing Figs. 11 and 12, we observe that the behaviors after positive bias annealing are quite the same for both top gate structures, independently of the insulator. Thus the increase of the dangling-bond state density below midgap in the a-Si:H near the I/S interface is still the dominant consequence of positive bias annealing. Conversely, the behaviors after negative bias annealing are somewhat different. Indeed, as in Fig. 11, in Fig. 12 we still observe a strong increase of the CBT minimum, along with the appearance of the VBT minimum becoming the main minimum, when the bias-anneal voltage has been changed from -1 to -3 V, and we also identify the flat-band voltage to be between -1 and -2 V. However, the VBT minimum does not decrease further when the bias-anneal voltage is changed from -2 to -3 V. Since the a-Si:H layer is the same in both top gate structures, this different behavior is attributed to the presence of interface states that make a significant contribution to the capacitance measured on the TG-SiN_x structure in the bias range around $V_G=-3$ V. Therefore, the VBT minimum is somewhat hidden by these interface states.

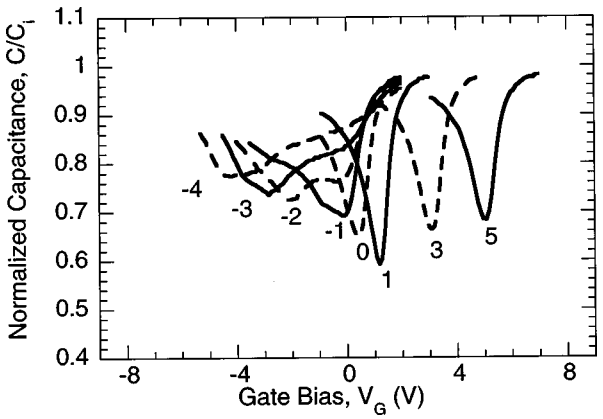

FIG. 12. Experimental normalized quasistatic capacitance C/C_i measured at $T=353$ K on the silicon nitride top gate structure (TG-SiN_x) as a function of the gate bias V_G after bias annealing at $T=473$ K under different bias-anneal voltages. The curves are labeled according to the bias-anneal voltage. They are shown, alternately, by plain and dashed lines, and only parts of the whole curves are shown for the sake of clarity.

Finally, we turn to the results obtained for the bottom gate SiN_x structures. These are shown in Figs. 13 and 14 for the BG1 and BG2 structures, respectively. Concerning positive bias-anneal voltages, the evolution of the qs-CV curves with V_{ba} is still the same as for the preceding structures, namely, a shift of the position of the minimum capacitance along with a slight increase of the minimum value. As far as negative bias annealing is concerned, we can distinguish some of the characteristic details that have been identified for the top gate structures. In particular, the CBT minimum increases when V_{ba} decreases, and it is shifted toward negative voltages, while we observe the appearance of another capacitance minimum that is identified to the VBT minimum. This is clear if we look at the curves corresponding either to $V_{ba}=-2$ and -4 V in Fig. 13 or to $V_{ba}=-1$ and -3 V in Fig. 14. However, we also observe that the evolution of these minima with the bias-anneal voltage is very different from

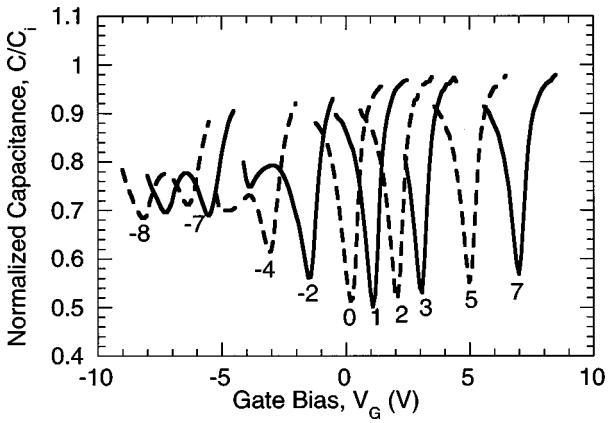

FIG. 13. Experimental normalized quasistatic capacitance C/C_i measured at $T=353$ K on the first silicon nitride bottom gate structure (BG1-SiN$_x$) as a function of the gate bias V_G after bias annealing at $T=473$ K under different bias-anneal voltages. The curves are labeled according to the bias-anneal voltage. They are shown, alternately, by plain and dashed lines, and only parts of the whole curves are shown for the sake of clarity.

that observed on the top gate structures. First, while the CBT minimum rapidly increases and tends to disappear for $V_{\mathrm{ba}}<-3$ V for the TG structures, it increases less rapidly and remains visible even on curves corresponding to very low negative bias-anneal voltages ($V_{\mathrm{ba}}=-8$ V in Fig. 13 or even $V_{\mathrm{ba}}=-15$ V in Fig. 14). For $V_{\mathrm{ba}}<-4$ V, the main trend is an overall shift of the whole qs-CV curve, with only slight changes in the shape, and the VBT minimum becomes the main minimum only for $V_{\mathrm{ba}}<-7$ V. This rather slow evolution of the shape of the qs-CV curve, compared to the case of the TG structures, is attributed to hole injection from the a-Si:H layer into the silicon nitride. Indeed, from Eq. (18), it is inferred that an increase of the charge in the insulator will lead to a negative shift of the qs-CV curve. Therefore, changes in the band bending in the a-Si:H layer with the bias-anneal voltage will be less important than in the case where no hole trapping is involved. This means that the

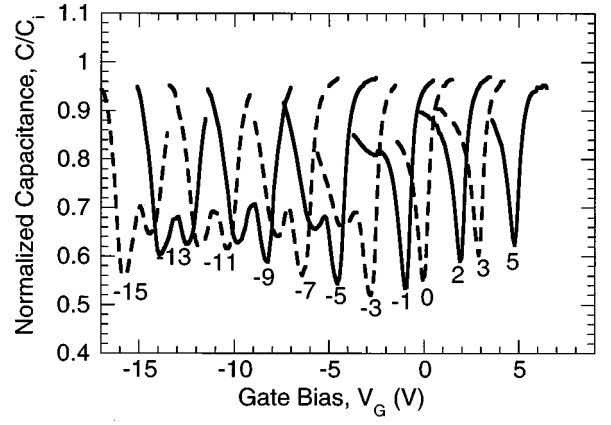

FIG. 14. Experimental normalized quasistatic capacitance C/C_i measured at $T=353$ K on the second silicon nitride bottom gate structure (BG2-SiN$_x$) as a function of the gate bias V_G after bias annealing at $T=473$ K under different bias-anneal voltages. The curves are labeled according to the bias-anneal voltage. They are shown, alternately, by plain and dashed lines, and only parts of the whole curves are shown for the sake of clarity.

modification of the DOS in the a-Si:H layer, and thus the changes of the shape of the qs-CV curves, are slowed down by the hole injection and trapping into the silicon nitride.

IV. DISCUSSION OF THE RESULTS USING THE SIMULATION OF THE qs-CV CURVES: DETERMINATION OF THE DEFECT-POOL PARAMETERS AND INFLUENCE OF THE *I*/*S* INTERFACE

From the above results the following qualitative conclusions can be drawn.

(i) The evolution of the qs-CV curves due to positive bias annealing is quite independent of the nature of the insulator and of the insulator/a-Si:H interface. Therefore, this evolution can be attributed to changes occurring in the defect density of the a-Si:H layer.

(ii) The evolution of the qs-CV curves due to negative bias annealing depends on the nature of the structure. This means that interface trap levels and hole injection and trapping into the insulator play a role. Hole injection is obvious in the BG-SiN$_x$ structures. Indeed, by increasing the negative bias-anneal voltage, we observe a shift of the whole qs-CV curve towards negative bias voltages. This overall shift is not observed on the top gate structures.

Since the a-Si:H layer was the same for the TG-SiN$_x$ and TG-SiO$_2$ structures, the qs-CV curves obtained on these structures were used to separate the contribution of the bulk a-Si:H from that of interface states. Concerning the TG-SiO$_2$ structure, we already showed that a good fit to the experimental qs-CV data could be obtained using the value of the defect-pool parameters called ''standard'' in Table I.[25] The choice of the defect-pool parameters can be fairly understood from the study of the influence of these parameters on the overall behavior of the qs-CV curves after positive bias annealing, as presented in Sec. II B. Indeed, one prominent feature of the qs-CV curves obtained on the top gate structures (see Figs. 11 and 12) is that the variation of the position of the minimum capacitance corresponds approximately to that of the bias-anneal voltage, i.e., the value of the mean slope s_V defined in Sec. II B is close to 1. According to Fig. 9, it can thus be deduced that the value of the characteristic parameter Δ_i should be less than 0.1 for $E_{v0}=0.056$ eV, this last value being typical of device grade a-Si:H. In the same time, Figs. 11 and 12 show that the increase of the minimum capacitance value with increasing bias-anneal voltage for $V_{\mathrm{ba}}>3$ V is such that s_C is of the order of 8×10^{-3} V^{-1}. Therefore, Fig. 9 indicates that the best choice for Δ_i is around 0.1 eV, where the theoretical values for s_V and s_C are 0.92 and 6×10^{-3} V^{-1}, respectively. Actually, the standard values of the defect-pool parameters, given in Table I yield $\Delta_i=0.093$ eV. Given the value of E_{v0}, the values U, σ, and E_p-E_v are found by matching the absolute value of the theoretical capacitance minimum to that observed experimentally. Indeed, these parameters mainly control the density of dangling-bond states, that in turn control the minimum capacitance values. Although the standard defect-pool parameters, together with a gap energy of 1.9 eV, reproduce quite well the overall behavior of the experimental qs-CV curves measured on the TG-SiO$_2$ structure,[25] we found that a better fit was obtained with a slightly lower gap value (1.8 eV), and consequently slightly modified defect-pool param-

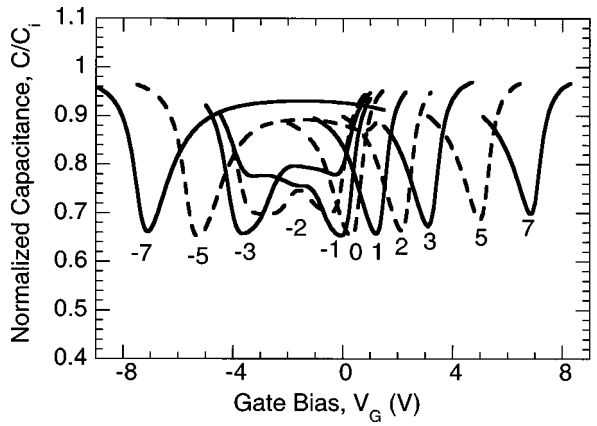

FIG. 15. Theoretical qs-CV curves simulating the results obtained on the silicon dioxide top gate structure (TG-SiO_2), using the parameters of Table I, and the density of interface trap levels presented in Fig. 19. No charge trapping into the insulator has been used.

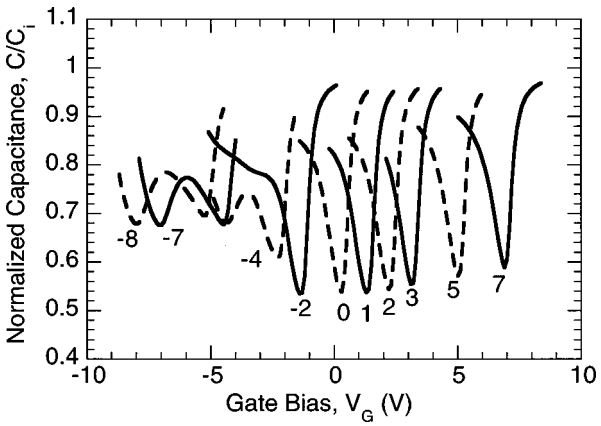

FIG. 17. Theoretical qs-CV curves simulating the results obtained on the first silicon nitride bottom gate structure (BG1-SiN_x), using the parameters of Table I, the density of interface trap levels presented in Fig. 19, and charge trapping into the insulator as shown in Fig. 20.

eters. The values giving the best fits are reported in Table I for all structures. The theoretical qs-CV curves obtained with these values are shown in Figs. 15, 16, 17, and 18 for the TG-SiO_2, TG-SiN_x, BG1-SiN_x, and BG2-SiN_x structures, respectively. Clearly, these theoretical curves reproduce fairly well the experimental curves of Figs. 11, 12, 13, and 14, respectively, in the whole range of bias-anneal voltages. Of course, the defect-pool parameters used to fit the qs-CV curves of the TG-SiO_2 and TG-SiN_x structures are exactly the same since these structures have the same *a*-Si:H layer. However, we note that, even for the BG-SiN_x structures that were fabricated in different laboratories, our good fits were obtained with almost the same defect-pool parameters, namely, $E_{v0} \approx 0.05$ eV, $\sigma \approx 0.157$ eV, $E_p - E_v \approx 1.16$ eV, and $U \approx 0.15$ eV. The fact that these parameters only weakly depend on the different structures strongly supports the defect-pool model. The density of dangling-bond states corresponding to these parameters is relatively flat, with a mean value of the order of 2×10^{16} cm^{-3} eV^{-1}, and a slight predominance of charged defects compared to neutral ones.

In addition to the bulk defects calculated from the defect-pool parameters, structure-dependent interface trap level densities were used to calculate the theoretical curves of Figs. 15–18. These interface trap level densities are shown in Fig. 19. They were constructed using two exponential band tails and two Gaussian distributions of deep states. It is worth emphasizing that these interface trap level densities were kept independent of the bias-anneal voltage, all the changes in the shape of the qs-CV curves being accounted for by the changes in the defect-pool DOS in the *a*-Si:H layer. It is interesting to compare the different structures in terms of their interface trap level densities. Indeed, we observe that the TG-SiN_x structure has the highest interface trap level density both for shallow and deep states. Note that for the TG-SiO_2 and BG-SiN_x structures the weight of the interface conduction-band tail states is negligible compared to that of bulk *a*-Si:H states, which is not the case for the TG-SiN_x structure. This point can be addressed together with the comparison of the field-effect mobility in TFT's fabricated using silicon nitride in the top and bottom gate configurations. In-

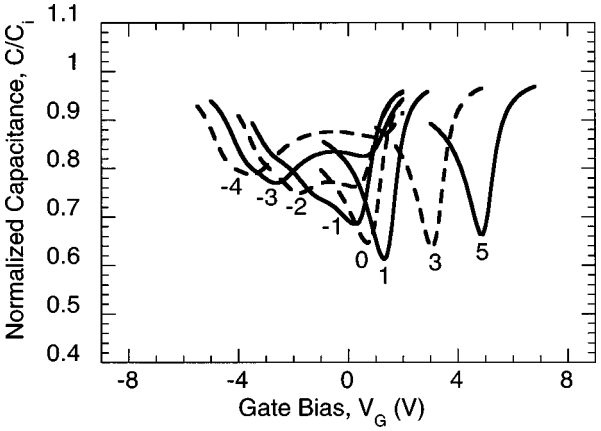

FIG. 16. Theoretical qs-CV curves simulating the results obtained on the silicon nitride top gate structure (TG-SiN_x), using the parameters of Table I, and the density of interface trap levels presented in Fig. 19. No charge trapping into the insulator has been used.

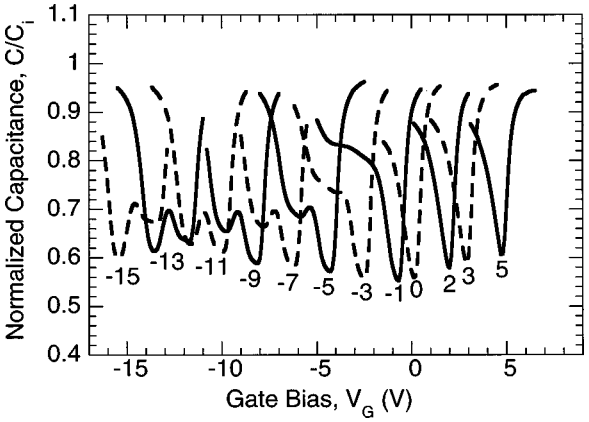

FIG. 18. Theoretical qs-CV curves simulating the results obtained on the second silicon nitride bottom gate structure (BG2-SiN_x), using the parameters of Table I, the density of interface trap levels presented in Fig. 19, and charge trapping into the insulator as shown in Fig. 20.

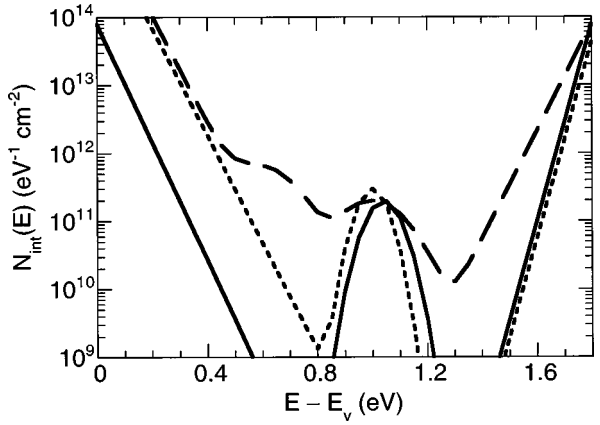

FIG. 19. Density of interface trap levels introduced in the simulation to reproduce the behavior of the experimental qs-CV curves. The solid, dashed, and dotted lines stand for the silicon dioxide top gate (TG-SiO_2), silicon nitride top gate (TG-SIN_x), and silicon nitride bottom gate (BG2-SiN_x) structures, respectively.

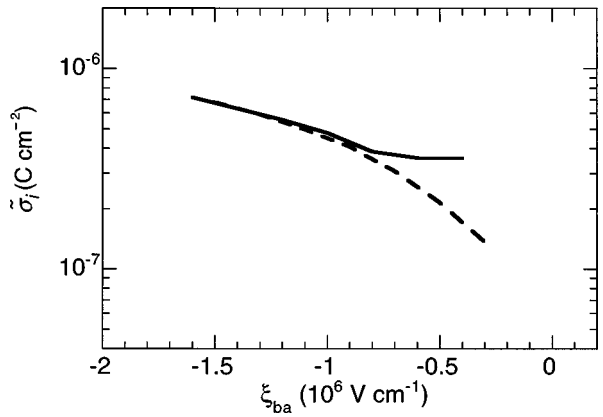

FIG. 20. Variation of the effective charge per unit area in the insulator as a function of the mean electric field during annealing for the silicon nitride bottom gate structures. The solid and dashed lines stand for the BG1 and BG2 structures, respectively.

deed, it is well known that top gate TFT's have a lower apparent mobility than bottom gate ones. It was shown that part of this difference could be attributed to the different source and drain contact and access resistances in the two configurations.[33] However, even after correction for these resistance effects, the field-effect mobility still remains somewhat higher in the bottom gate TFT's. According to our quasistatic capacitance results, this higher value should be related to a lower density of interface trap levels in the conduction-band tail.

Finally we address the problem of fixed charges and charge trapping in the insulator. The fixed charge is related to the true flatband voltage that can be deduced from each set of qs-CV curves. The values are reported in Table I. We observe that all structures have a positive charge in the insulator, the highest values being obtained for the bottom gate silicon nitride structures. As stressed in Sec. III, hole injection into the silicon nitride is observed for these structures under negative bias annealing. This hole injection is accounted for by the variation of the apparent charge density $\tilde{\sigma}_i = \tilde{Q}_i / A$, as shown in Fig. 20. Since the insulator thickness was different for the BG1 and BG2 structures, the evolution of $\tilde{\sigma}_i$ has been plotted as a function of the mean apparent field during bias annealing, $\xi_{ba} = V_{ba} / L_i$, rather than V_{ba}. Although the nitride layer may be different in the two structures since they were fabricated in two different laboratories, we observe in Fig. 20 the same kind of increase of $\tilde{\sigma}_i$ when the bias-anneal voltage becomes more negative. Although our results were obtained under bias annealing at 200 °C, hole trapping into the insulator can still be a problem in bottom gate nitride thin-film transistors at lower temperatures. From this point of view, we can note that our top gate structure using DECR-PECVD silicon dioxide as the insulator does not exhibit such charge trapping. It also has a low interface trap level density, that should make it a very interesting candidate in TFT applications.

V. CONCLUSIONS

The dependence upon gate bias of the quasistatic capacitance of *a*-Si:H-based MIS structures is very powerful to characterize the properties of both the *a*-Si:H layer and the *I*/*S* interface. The evolution of the qs-CV curves after annealing under different bias-anneal voltages can be related to changes in the defect density and to charge trapping into the insulator.

Our theoretical study of qs-CV curves and the comparison with experimental results obtained on different kinds of *a*-Si:H-based MIS structures strongly support the defect-pool model. Indeed, the evolution of the qs-CV curves after positive bias annealing is almost the same independently of the nature of the insulator (silicon nitride or silicon oxide) and of the interface (top or bottom gate silicon nitride). This evolution is due to changes in the density of dangling bonds in the *a*-Si:H close to the interface. Increasing the positive bias-anneal voltage leads to the increase of the dangling-bond density, the maximum of the distribution being located below midgap. Due to this below midgap location, these dangling bonds are negatively charged when the structure is biased for electron accumulation, which explains the positive shift of the CBT minimum in the qs-CV curves, and the concomitant positive shift of the threshold voltage generally observed on TFT's. The evolution of the qs-CV curves after negative bias annealing is also well reproduced by the defect pool model. In particular, we observe that the main capacitance minimum flips from the CBT to VBT one when the bias-anneal voltage is decreased below the flatband voltage. The creation of dangling-bond states in the upper part of the gap is clearly detected when the bias-anneal voltage becomes more negative. Although the overall changes of the qs-CV curves due to changes of the bias-anneal voltage are very well accounted for by changes in the defect-pool dangling-bond density of the *a*-Si:H layer, the details of these curves depend on interface trap levels and charge injection in the insulator. We find that the structures using silicon dioxide obtained by distributed electron cyclotron resonance plasma-enhanced chemical-vapor deposition have a low interface trap level density, and do not exhibit charge trapping into the insulator in the explored range of bias-anneal voltages. For the top gate nitride structure, changes of the shape of qs-CV curves are a little less pronounced than for the top gate oxide structure, due to the presence of a higher density of interface

trap levels. Top gate nitride structures also have the highest density of interface trap states in the conduction-band tail, and their weight is not negligible compared to that of the bulk *a*-Si:H conduction band-tail states. This supports the commonly observed results, namely, that the field-effect mobility measured on top gate nitride TFT's is lower than that of bottom gate nitride TFT's. The bottom gate nitride structures exhibit hole trapping in the insulator under high negative bias annealing (where hole accumulation occurs in the *a*-Si:H close to the interface). This hole injection induces a shift to more negative voltages of the whole qs-CV curves, and slows down the occurrence of the changes in defect density and thus in the shape of the qs-CV curves.

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