Effect of island length on the Coulomb modulation in single-electron transistors

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We have studied single-electron transistors with island lengths of 2, 10, 20, 30, and 40 μm and with high-resistance tunnel junctions to minimize the effects of cotunneling and electron self-heating. With longer islands, there is a marked reduction of the gate modulation of the Coulomb blockade width. According to orthodox theory, the width of the Coulomb blockade at $T=0$ is equal to e/C_Σ, and it falls approximately exponentially with k_BT/E_c, where $E_c=e^2/2C_\Sigma$, and C_Σ is the total capacitance. Based on numerical calculations and analytic estimates, we conclude that the modulation reduction is mainly due to the large increase in stray capacitance between the island and the leads as the island length is increased, and not to some more subtle nonequilibrium effect. When the increased capacitance is combined with the effect of electron heating, the Coulomb modulation is rapidly reduced. This work also demonstrates the need to take stray capacitance into account in addition to intrinsic junction capacitance even in structures that are only a few μm long.
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I. INTRODUCTION

The development of single-electron tunneling devices has been guided by simulations based on the "orthodox theory." [1–3] This theory is based on calculating the rates of single-electron tunneling transfers from one electrode to another, the electrodes being treated as zero-dimensional metal islands in internal equilibrium, characterized only by macroscopic parameters: capacitance and tunnel resistance. As the islands get larger, their capacitances increase, charging energies decrease relative to the thermal energy k_BT, control of electron number with unit precision becomes impossible, and characteristic features of single-electron tunneling, such as the Coulomb blockade, disappear. This scenario leaves open the possibility that other physical effects, not included in the zero-dimensional orthodox theory, might need to be taken into account in analyzing the Coulomb blockade when the physical dimension of an island becomes larger than some characteristic length scale. Examples of such possible length scales are the inelastic diffusion length (typically $\sim 10\ \mu$m), which limits the range of quantum phase coherence of the electrons, and the relativistic event-horizon length (typically $>100\ \mu$m) set by the speed of light and characteristic energies.

To explore experimentally the possible existence of a breakdown of orthodox theory due to such interesting nonequilibrium effects, we have fabricated and characterized the width of the Coulomb blockade in the tunneling characteristics of a series of single-electron tunneling transistors with island lengths of 2, 10, 20, 30, and 40 μm. In such transistors, a small superconducting (A1) island is weakly coupled to a bias circuit through two small-capacitance tunnel junctions and a capacitive gate as shown in Fig. 1.[4] A voltage V_g applied to the gate electrode modulates the equilibrium number of electrons on the island by an amount $C_gV_g/e=Q_0/e$. When Q_0 is an integer multiple of e, overcoming the Coulomb blockade requires an excess voltage of e/C_Σ, i.e., $2E_c/e$ (where $E_c=e^2/2C_\Sigma$ is the charging energy of the island with total capacitance C_Σ to its environment). On the other hand, if Q_0 is a half-integer multiple of e, there is no blockade since one pair of successive integer numbers of electrons has the same energy. When we vary the gate voltage V_g rapidly while slowly taking the I-V measurements, we can obtain an envelope of I-V curves. We refer to this as an $I(V,V_g)$ characteristic, and to the visible modulation within the envelope as the gate modulation of the Coulomb blockade. We have observed that, with longer islands, there is a marked reduction of the modulation width of the Coulomb blockade with variation of gate charge Q_0, even at our lowest available temperatures. As stated above, according to orthodox theory, the voltage width of the Coulomb blockade modulation at $T=0$ is equal to e/C_Σ, whether the island is in the superconducting or the normal state. For $T>0$, simulations show that the normalized Coulomb width, i.e., width/(e/C_Σ) falls approximately exponentially with k_BT/E_c as shown in Fig. 2. This plot contains information on the modulation width as it depends on both temperature and length since length is contained in the estimate of E_c. However, the observed width was found to decrease much faster than we had expected on the basis of our original estimated values of C_Σ versus island length. A main point of this paper is to show that the reason for this discrepancy is that our original estimate of C_Σ was flawed because we shared the

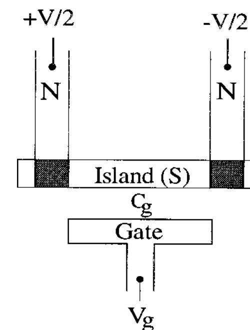

FIG. 1. Configuration of the NSN single-electron transistor, with normal-metal leads (Au) and superconducting island (Al).

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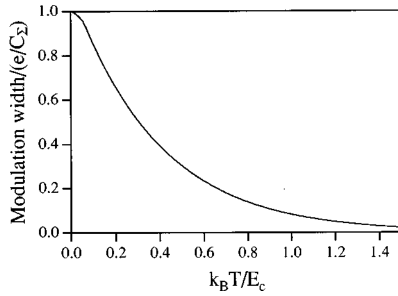

FIG. 2. Normalized modulation width versus k_BT/E_c based on orthodox theory.

general lack of appreciation of the large magnitude of stray capacitances in such systems.

These samples are fabricated with high-resistance tunnel junctions to minimize cotunneling[5] and electron self-heating, both of which reduce the visible Coulomb blockade. In the process of explaining these data, we have eliminated the possibility that the effect is due to electron heating alone, since that would require an unrealistic temperature of over 400 mK in order to fit the observed modulation reduction with a simulation based on our original estimates of C_Σ. In addition, the global rule to local rule transition described in the ''even-horizon'' model[6] does not appear to explain this length dependence either since it predicts a much longer crossover length of $>200\ \mu$m. Furthermore, thermally enhanced inelastic cotunneling alone does not seem to cause sufficiently rapid modulation reduction. With extensive FASTCAP (Ref. 7) calculations, we have found that the reduction of the Coulomb modulation is, in fact, mainly a classical effect caused by the large increase in the stray capacitances between the leads and the island as its length increases. These FASTCAP results can be semiquantitatively understood by simple analytic methods. Including also the effect of electron heating, this capacitance increase appears to provide a reasonably quantitative explanation for the rapid reduction in the Coulomb modulation with increasing island length, which was observed in our experiment. This result serves as a warning that, unless the island length is very short, stray capacitance *must* be included in the analysis to avoid errors in interpretation of data. We also explore the broader implications of this analysis for other experimental configurations.

II. OBSERVATION OF A LENGTH EFFECT IN SINGLE-ELECTRON TUNNELING

In this section we present systematic experimental data on the effect of island length on the observed Coulomb blockade of single-electron tunneling transistors. Figure 3 shows the $I(V,V_g)$ characteristics for five different NSN samples (see Fig. 1) with island lengths ranging from 2 to 40 μm. From these plots, we see that the width of the Coulomb blockade right above the superconducting energy gap decreases rapidly as the length is increased. For the 40 μm sample, the gate modulation is barely observable.

As further evidence for the significant reduction of modulation in our $I(V,V_g)$ curves, we have also taken data with

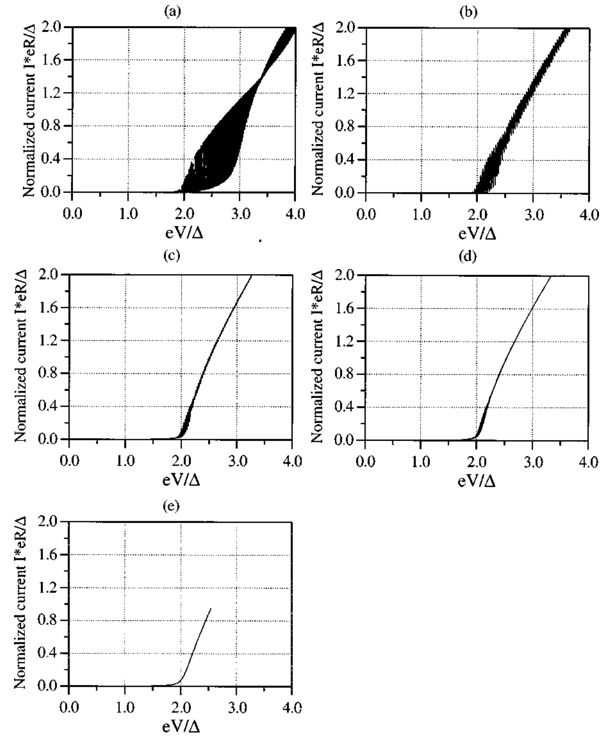

FIG. 3. Measured $I(V,V_g)$ characteristics for five different NSN samples with island lengths of (a) 2, (b) 10, (c) 20, (d) 30, and (e) 40 μm. The plots are scaled with the energy gap Δ and the total normal resistance (R_1+R_2) of the two junctions in the device.

the island made normal by applying a 2 T magnetic field. This eliminates the 2Δ gap of the superconductor that adds to the Coulomb blockade in Fig. 3. Figure 4 illustrates the normal state $I(V,V_g)$ characteristics (normalized with the junction resistances) for four samples of lengths 2, 10, 30, and 40 μm, respectively. These curves are superimposed on top of each other to demonstrate how the Coulomb gap shrinks as the island length increases. We observe that as the length increases, the modulation decreases and collapses toward the inner edge of the 2 μm curve, which corresponds to $Q_0=e/2$, that is, to no Coulomb blockade. Since the modulation reduction is similar to that in the superconducting

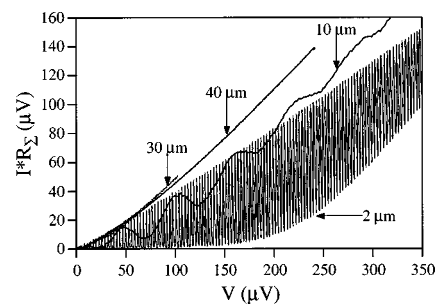

FIG. 4. Measured $I(V,V_g)$ characteristics of four samples with islands held in normal state by a 2 T magnetic field. (Although the gate voltage was swept more slowly for the 10 μm sample than for the 2 μm sample, the reduction in gate modulation amplitude is still clear.)

case, this shows that the length dependence does not involve superconductivity in any essential way.

III. STRAY CAPACITANCE ANALYSIS

From orthodox theory at $T=0$, the Coulomb blockade width is equal to e/C_Σ. When the island length is increased, the total capacitance C_Σ of the system will be increased. Unfortunately, the accurate independent measurement of C_Σ has been difficult in our experiments. A common method is to extrapolate the asymptotic I-V curve back to the horizontal (voltage) axis. The intercept value V_{offset} in principle yields the Coulomb blockade result e/C_Σ. However, this method fails since V_{offset} is a function of V so that the intersection value depends on the voltage range we use to extrapolate the I-V curve. Another method is to plot V_{offset} as a function of V.[6] By extrapolating V_{offset} back to zero-bias voltage, we should get a voltage corresponding to the charging energy in the global rule, i.e., e/C_Σ. However, the nonlinearity in our I-V data at high bias voltages due to barrier bending[8] gives us an unreliable result. For example, we have extrapolated a charging energy of about 150 μeV for a 20 μm sample. This clearly cannot be correct since it implies a C_Σ of 530 aF, while the measured C_g value alone (560 aF) already exceeds this value. In principle, one should be able to extract the junction capacitances from the V-V_g contour plot,[9] but this was not available in our experiment.

A. Capacitance calculations using FASTCAP

The crucial parameter C_Σ is the sum of the two intrinsic junction capacitances $2C_i$, the stray capacitance C_s between the island and the two leads, the gate capacitance C_g, and the capacitance C_∞ between the island and "infinity." It is important to realize that each of these capacitances depends on the presence of the other electrodes (except for the intrinsic junction capacitance, where the electric field is well localized between the two electrodes), and in general cannot be computed simply pairwise. Rather, we have used FASTCAP to compute the capacitance *matrix* of the *whole* array, again apart from C_i.[10] We then identify the various capacitances named above with off-diagonal elements of the matrix.

Figure 5(a) illustrates the geometry of the large-scale lead (10 and 100 μm wide) patterns of a 10-μm-long island sample. The six large rectangular pads at the end of the leads model the indium dots that are used to bond the leads to the external circuit wires for measurements. The large plane underneath the sample represents a metal plane that is electrically connected to the gate electrode. Figure 5(b) zooms into the center region and shows the small-scale (100 nm, 400 nm, and 1 μm wide) leads in the vicinity of the island. Table I gives the complete capacitance matrix for a 20 μm-long island sample calculated by FASTCAP.

Let us consider the third row of this matrix to illustrate its meaning. The absolute value of the capacitance matrix element C_{31} represents the mutual capacitance between the island and the left lead and $|C_{32}|$ is that between the island and the right lead. $|C_{34}|$ represents the capacitance between the island and the lithographic gate and $|C_{35}|$ that between the island and the metal gate plane. Thus, the stray capacitance C_S is $(|C_{31}|+|C_{32}|)$ and the gate capacitance C_g is $(|C_{34}|+|C_{35}|)$. The capacitance C_{36} from the island to "infinity" is small since the field lines from the island bend back into the large metal plane situated below, rather than going to "infinity," and hence are included in the capacitance between island and gate. In the following, we will neglect C_{36}, since it makes only a $\sim 1\%$ contribution to C_Σ, although the capacitance between the other, more extended, elements and "infinity" is quite significant, as can be seen from the tabulated matrix elements. C_{33} corresponds to the total capacitance of the island to its environment (apart from the intrinsic capacitance of the tunnel junctions); it is equal to the sum of $|C_{31}|$, $|C_{32}|$, $|C_{34}|$, $|C_{35}|$, and $|C_{36}|$, consistent with the fact that the sum of all the elements in any row or column must be zero. Because of our limited computer power, all of these capacitances were first calculated in free space ($\varepsilon_{\text{eff}}=1$) and then scaled up by the estimated effective dielectric constant $\varepsilon_{\text{eff}}\sim 6.45$, an arithmetic average between the dielectric constant of free space ($\varepsilon=1$) and of Si ($\varepsilon_{\text{Si}}=11.9$). (This approximation is supported by a formal application of the method of images in an idealized geometry similar to ours, as well as by the results of rather simple but specific FASTCAP calculations that included a silicon substrate of the appropriate geometry.) The matrix is calculated for the actual geometry of the sample, which is not even left-right symmetric with respect to the island.

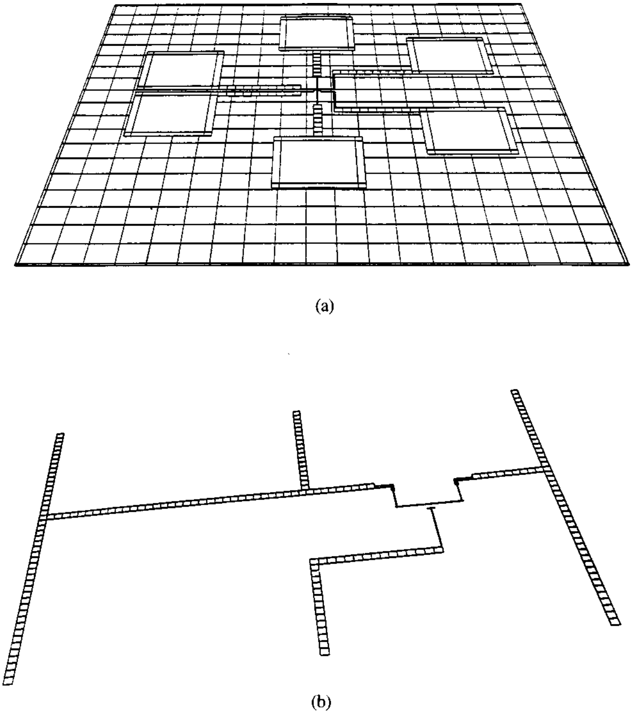

FIG. 5. (a) Large-scale lead patterns of a typical device. The six large rectangular pads at the end of the leads model the indium dots. The plane underneath the device represents the metal plane connected with the gate electrode; (b) Small-scale lead (100 nm, 400 nm, and 1 μm wide) patterns in the vicinity of the island.

The gate capacitance can be accurately measured from the periodicity in the I-Q_0 curve. We have found that the gate capacitance increases roughly linearly with the island length, with a slope of about 25 aF/μm. To complete our best estimate of C_Σ, we combine the results of the FASTCAP calculation for the stray capacitance C_s with the measured value

TABLE I. Capacitance matrix of a 20 μm-long island sample (in fF). These values include the effective dielectric constant ϵ_{eff} (see text), but do not include the estimated intrinsic capacitance of the tunnel junctions.

	Left lead (1)	Right lead (2)	Island (3)	Litho-graphic gate (4)	Gate plane (5)	''Infinity'' (6)
Left lead (1)	1528.00	−44.83	−0.37	−23.54	−1378.37	−80.89
Right lead (2)	−44.83	1182.93	−0.42	−30.38	−1045.54	−61.76
Island (3)	−0.37	−0.42	1.24	−0.34	−0.10	−0.01
Lithographic gate (4)	−23.54	−30.38	−0.34	555.47	−474.08	−27.13
Gate plane (5)	−1378.37	−1045.54	−0.10	−474.08	4311.83	−1413.74
''Infinity'' (6)	−80.89	−61.76	−0.01	−27.13	−1413.74	1583.53

of C_g and our estimate of the intrinsic parallel plate capacitances of the junctions from their known area.

The intrinsic capacitance C_i of the junction can be estimated theoretically based on the parallel-plate capacitor model. Taking the oxide barrier thickness of our junction to be 15 Å (estimated from its conductance[11]), and a dielectric constant for AlO_x of eight, the capacitance/area would be 47 fF/μm^2. This is very close to the nominal value of 45 fF/μm^2 determined from large area junctions of similar nature.[12] Typical junction areas are estimated to be $(80 \pm 20\ \mathrm{nm})^2$, which would yield capacitance estimates of 300 ± 150 aF. In view of this uncertainty, the value of C_i must be considered a somewhat adjustable parameter, although the uncertainty is swamped by the increasing values of C_g and C_s in the longer islands. From three previously studied 2-μm-long island samples of the same geometry and fabrication procedure, we extracted single junction capacitances C_1 and C_2 from the V-V_g contour plot,[9,13,14] and they are $C_1 = 430$ aF and $C_2 = 310$ aF, $C_1 = 540$ aF and $C_2 = 450$ aF, $C_1 = 470$ aF and $C_2 = 510$ aF. The average of these junction capacitances yield a single junction capacitance of about 450 aF that includes the stray capacitance (≈ 70 aF to each lead as shown in Table II). After subtracting out this stray capacitance, the intrinsic capacitance is then about 380 aF, which is consistent with the estimated range from the parallel-plate capacitance model. Since the capacitance should actually vary inversely with the barrier thickness and hence with the logarithm of the tunnel resistance (for fixed area), the junctions will not all have exactly the same C_i, but this effect is too small to account for the measured range of capacitance values. In view of these uncertainties, in our calculations we have adopted a single value $C_i = 300$ aF, which lies in the middle of the range theoretically estimated from the junction dimensions.

The stray capacitance C_s between the island and all the surrounding leads is found to be quite large and to increase linearly with island length, so that it soon dominates the junction capacitance C_i. Since both C_s and C_g increase linearly with island length L, the total capacitance C_Σ will increase approximately linearly with island length, leading to a rapidly decreasing E_c. The values determined from the FASTCAP calculations are listed in Table II. We see that the calculated C_g values are 10–20 % smaller than the actual measured ones. This discrepancy probably arises because we have modeled our conductors as having zero thickness in our FASTCAP calculations. In addition, a finer discretization $(n>3)$ would also increase the C_g value, but would require more computer power than was available. The total capacitance C_Σ is taken to be $2C_i + C_s + C_g$ (with measured C_g values). Figure 6 plots the calculated stray capacitance C_s, the calculated and measured gate capacitance C_g, and the total capacitance of the island C_Σ as a function of the island length. Since each of the five samples has slightly different geometry in terms of the lengths of the island and the lithographic gate, the capacitances do not, and are not expected to, agree completely to a linear fit.

To test these results, we simulate the $I(V,V_g)$ curves based on orthodox theory for each sample with different is-

TABLE II. Measured resistances and gate capacitances, calculated gate and stray capacitances, and estimated total capacitances.

Length (μm)	Resistance R_Σ (kΩ)	Measured C_g (aF)	Calculated C_g (aF)	Calculated C_s (aF)	Estimated total capacitance $C_\Sigma = 2C_i + C_S + C_g$ (aF)
2	240	70	63	144	814
10	1430	254	230	468	1322
20	584	560	441	792	1952
30	168	788	647	1100	2488
40	1850	1000	793	1520	3120

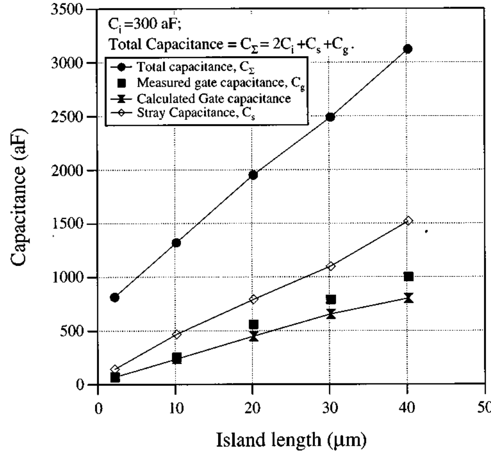

FIG. 6. Plot of the calculated stray capacitance C_s, the measured and calculated gate capacitance C_g, and the estimated total capacitance C_Σ as a function of the island length. The calculated values correspond to the actual geometries of the devices.

land length. Even though the operating temperature of the mixing chamber of our dilution refrigerator $T_m \approx 15$ mK, the electron bath can still be at a higher temperature due to the poor coupling between the electrons and phonons at low temperatures. This implies that the effective temperature can be high enough to cause thermal rounding, and as a result to further reduce gate modulation. The electron-phonon coupling model gives the electron bath temperature:[15]

$$T_e = \sqrt[5]{\alpha IV/\Sigma V_I}. \tag{1}$$

Here α is the fraction of the total Joule power IV dissipated by electron-phonon coupling in the island; it is chosen to be ~25% in our simulation. V_I is the volume of the island and the material constant Σ is taken to be 0.2 nW/(K^5 μm^3).[15] We have assumed that the phonons in the island are well coupled to the mixing chamber whose temperature is such that $T_m^5 \ll T_e^5$.

With the C_Σ values from Table II, we simulate the $I(V,V_g)$ curves for each sample based on the orthodox model with power-dependent temperatures. The program algorithm is as follows: at each fixed bias voltage, we first start at a high temperature, obtain the current based on the orthodox theory,[13] then calculate a new temperature according to Eq. (1). With this new temperature, we then iterate back to recalculate the current until self-consistency is achieved, i.e., until the new temperature converges with the previous one.

The simulated I-V curves obtained in this way for each sample are shown in Fig. 7. They outline the envelope of the $I(V,V_g)$ curves, corresponding to $Q_0=0$ and $Q_0=e/2$, in the case of symmetric tunnel junctions. These simulation curves match well with the experimentally measured $I(V,V_g)$ curves shown in Fig. 3. For the 2 μm sample as shown in Fig. 7(a), the modulation is well developed and shows nearly the full width one would expect in the typical case in which C_Σ is dominated by the intrinsic junction capacitances. As the island length is increased, we see that the gate modulation decreases quickly. When the length is 40 μm as plotted in Fig. 7(e), the two curves at $Q_0=0$ and $e/2$ nearly overlap each other and lead to minimal, but nonzero, modulation, whereas modulation is hardly visible in the corresponding

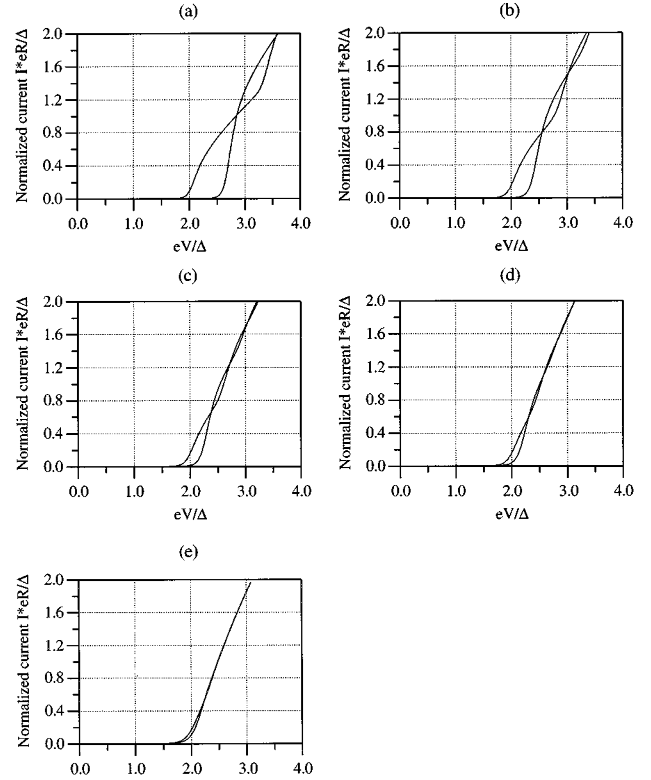

FIG. 7. Simulated I-V curves based on orthodox model at $Q_0=0$ and $e/2$ using FASTCAP results and power-dependent temperatures for samples with the same island lengths and scaling as in the corresponding panels in Fig. 3.

experimental curve in Fig. 3(e). This is the only significant discrepancy between the simulated and experimental curves.

Because of the direct relation between the maximum modulation width at $T\approx 0$ and $1/C_\Sigma$, it is of interest to make a systematic quantitative comparison between the *measured* maximum widths and the maximum widths found in finite temperature *simulations* using our estimated values of C_Σ. The latter were found from the simulated curves by determining the voltage modulation widths at various constant current levels, and taking the maximum value. The electron bath temperatures T_e at these maximum modulation widths are calculated according to Eq. (1) to be 275, 153, 154, 182, and 116 mK for the 2-, 10-, 20-, 30-, and 40-μm samples, respectively. These values are not monotonic because they depend on R_Σ as well as V_I. The modulation widths determined from simulation are plotted as closed circles in Fig. 8. For comparison, the measured maximum Coulomb modulation widths at each island length are plotted as triangles. From this figure, we see that the voltage modulation widths as determined from the simulations generally agree quite well with the ones measured. The discrepancy of the two at longer island lengths suggests that the total capacitances C_Σ determined with FASTCAP are smaller than the actual ones. This is consistent with the deviation of the measured and calculated gate capacitance C_g, noted earlier. In fact, if one assumes the same deviation, i.e., that the FASTCAP values underestimate the true values by approximately 20%, this would lead to a further 30% reduction in the simulated modulation for the longest island. Although substantial, such a correction is too small to account for the entire discrepancy

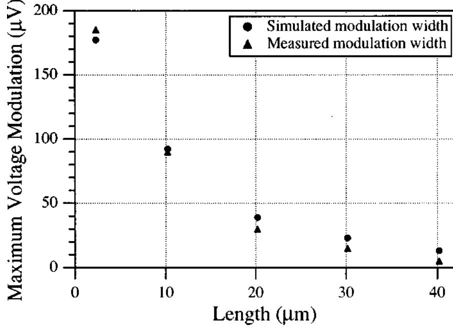

FIG. 8. Comparison of the measured (Fig. 3) and simulated (Fig. 7) maximum voltage modulation width vs island length.

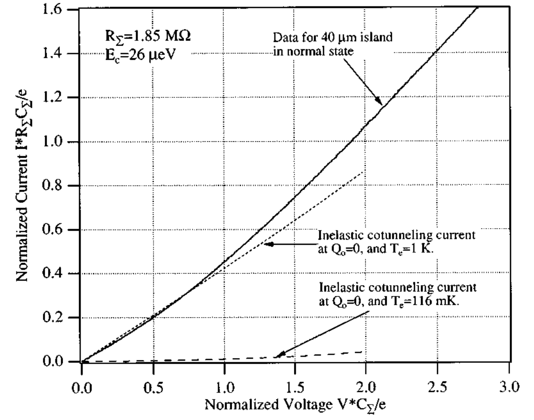

FIG. 9. Comparison of the I-V data for a 40 μm normal island with the inelastic cotunneling current calculated at $T_e \approx 1$ K and $T_e \approx 116$ mK for $Q_0=0$.

between the experiment and simulation for this sample. Possibly the remaining discrepancy results from an underestimate of the electronic heating by Eq. (1). This formula is based on the assumption of a spatially uniform heating of the electron gas. This should be appropriate for a short island, but in long islands the finite electronic thermal diffusivity will lead to higher electronic temperatures near the tunnel junctions, where the heating is injected, and where the local temperature determines the rounding of the tunnel curves and the amount of modulation reduction. This effect would be expected to become significant for lengths above the inelastic diffusion length for electrons, typically ~ 10 μm, and we speculate that it might account for the increasingly significant discrepancies between data and simulations for the 20-, 30-, and 40-μm samples.

In these simulations, we have neglected any contribution from the inelastic cotunneling current. This is a process in which two electrons tunnel simultaneously through the junctions and an electron-hole excitation is left on the island. Since this process provides a way around the Coulomb blockade, it can contribute to the current in the blockade region where the sequential-tunneling current is very small.[16] Since for low temperatures, the inelastic cotunneling current varies as the third power of the voltage V, it makes the I-V curve appear to be rounded near the voltage onset of the single-electron tunneling. Because of the fact that the current is inversely proportional to the square of the junction resistances, we have fabricated high-resistance junctions to minimize this process. However, since the electron bath is at a higher temperature due to the poor electron-phonon coupling, this process is enhanced and gives rise to a larger current than at $T \approx 0$. This would further reduce the modulation width. However, we find that the contribution from thermally enhanced inelastic cotunneling is not significant enough to cause major modulation reduction, even with significantly reduced E_c's due to the large stray capacitances. Figure 9 shows the data in the normal state of the 40-μm sample as compared with the calculated current based on the inelastic cotunneling process.[17] In order to fit the cotunneling current with the measured current, it requires an electron bath temperature of $T_e \approx 1$ K, which is unrealistic for the small voltage range we are considering. At the electron bath temperature corresponding to the maximum modulation width for this sample, i.e., $T_e \approx 116$ mK, the inelastic cotunneling current is negligible as seen in this figure. Thus we believe that the correction of the modulation reduction due to the inelastic cotunneling process is not significant in our observations.

B. Analytic approximations to C_{ij}

In retrospect, we recognize that the results of the computer-intensive FASTCAP calculations could have been anticipated in a semiquantitative way by simple analytic approximations. The essential observation is that the electrodes in this geometry are essentially one-dimensional ''wires'' of length L and width w. The self-capacitance of such a conductor (in vacuum) is well known to have the general form

$$C_{ii}=\frac{L/2}{\ln(L/w)+1}, \tag{2}$$

where the ''1'' in the denominator represents a number of order unity which depends on the exact geometry. Clearly, this C_{ii} is proportional to the length L, apart from a logarithmic correction. (For typical values of L/w, this converts the local dependence on L from linear to L^p, with $p \approx 0.75$.) The mutual capacitance between such an element and another of the same type is essentially half this value, i.e., the series combination of such ''spreading capacitances'' from each element, with the length being that of the shorter element in case of asymmetry. Thus, we estimate that

$$C_{ij}=\frac{L/4}{\ln(L/w)+1}. \tag{3}$$

If we include an effective dielectric constant

$$\varepsilon_{\rm eff}=\frac{1+\varepsilon_{\rm Si}}{2}\approx 6.5, \tag{4}$$

and convert to SI units, we obtain the approximation

$$C_{ij}(\mathrm{aF})=\frac{182L(\mu\mathrm{m})}{\ln(L/w)+1}. \tag{5}$$

Finally, if we take the typical values $L \approx 20$ μm and $w \approx 100$ nm in the denominator, we obtain $C_{ij} \approx 29$ aF/μm, which is about 30% higher than the FASTCAP values. The sense of this discrepancy is that which one expects between

elements of a full capacitance matrix and capacitances between two isolated elements, because the presence of other elements has a ''shielding'' effect which tends to reduce the capacitive coupling quite substantially when C_{ij} is not much less than C_{ii}, as is the case here. Moreover, we noted above that there is experimental evidence that our FASTCAP calculations may be *underestimating* the actual capacitances by $\sim 20\%$, which would significantly reduce the discrepancy between the analytic estimates and the actual values.

C. Broader implications

The large size of these estimated stray capacitance values implies that the traditional approximation of modeling the capacitances in single-electron tunneling circuits as arising solely from the intrinsic capacitance of the tunnel junctions needs to be re-examined. For example, even for a typical short island length of 2 μm, the stray capacitance to each lead is calculated to be approximately 70 aF, which is not negligible compared to an intrinsic capacitance of 300 aF. When junction capacitances are determined by fitting features in the Coulomb staircase, what is actually determined is the combination of the intrinsic and the stray capacitance. If this combined number is treated as reflecting only the intrinsic capacitance, it provides an overestimate of the specific capacitance. This observation may explain the lack of consistency of various estimates of this specific capacitance found in the literature, and suggests that the low end value of 45 fF/μm^2 (Ref. 12) may be the most appropriate for the intrinsic value, so long as corrections are made for the stray capacitance as well.

IV. CONCLUSION

We have made a systematic investigation of the effect of island length on the Coulomb blockade in single-electron transistors, and observed a rapid reduction of the Coulomb modulation with increasing island length. Although we have considered various possible origins for this length effect, we have concluded that the rapid increase in the stray capacitances between island and leads, causing them to dominate the intrinsic junction capacitance, is, in fact, the dominant factor producing the rapid reduction of Coulomb blockade modulation. This conclusion is supported by extensive FASTCAP calculations and analytic approximations, which indicate a stray capacitance of ≈ 25 aF/μm between two long and narrow conductors on a Si substrate. Simulations based on orthodox theory using these capacitance values together with electron heating (estimated to reach temperatures of $\sim 100-200$ mK in these experiments) appear to give a satisfactory account of our experimental data. As a byproduct of this analysis, we conclude that the values of individual capacitances inferred from detailed fitting to $I(V,V_g)$ characteristics of single-electron tunneling transistors include significant contributions from stray capacitance to the leads, and that the specific capacitance of the junctions themselves is probably only ≈ 45 fF/μm^2, as had been estimated from measurements on large-area junctions.

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