Defect creation and removal in hydrogenated amorphous silicon predicted by the defect-pool model and revealed by the quasistatic capacitance of metal-insulator-semiconductor structures

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The quasistatic capacitance of metal-insulator-semiconductor structures is shown to be a powerful tool to study the defect formation in hydrogenated amorphous silicon (a-Si:H), and it is used to test the defect-pool model. Numerical calculations demonstrate that, in the framework of this model, the changes in the density of dangling bond states induced by thermal bias annealing are reflected in the shape of the capacitance versus the gate bias (C-V) curve. Though some details of experimental C-V curves obtained on aluminum/silicon dioxide/a-Si:H structures are not explained by this model, the major model characteristics are clearly observed. In particular, it is confirmed that a bump of dangling bond states is created below or above midgap, depending on whether the Fermi level is moved towards the conduction or the valence band during thermal bias annealing. [S0163-1829(97)52416-7]

The electronic properties of hydrogenated amorphous silicon (a-Si:H) devices such as thin film transistors (TFT) are mainly controlled by the electronic density of states (DOS) in the gap of the a-Si:H layer. It is now well established that two kinds of states prevail in a-Si:H: band-tail states related to weak Si-Si bonds, and deep defects due to silicon dangling bonds (DB), which can be positively charged (D^+), neutral (D^0), or negatively charged (D^-) depending on whether they are occupied by zero, one, or two electrons. A great effort has been made to understand the origin and formation of these dangling bonds, and there is now strong evidence that the density of dangling bonds results from a chemical equilibrium process that describes the breaking and reconstruction of weak Si-Si and Si-H bonds.[1–3] These ideas, together with the assumption that dangling bonds can form at different energies due to the inherent disorder, are the basis of the defect-pool model that has been considerably improved in the past few years.[4–9] From an experimental point of view, it could account for optical subgap absorption measurements,[10,11] and it was used by Deane and Powell to fit the transfer characteristics of TFT's after thermal bias-annealing treatments.[12] The use of field-effect devices is very attractive to test the defect-pool model. Indeed, in such devices, the position of the Fermi level can be changed within the gap near the insulator interface by applying a gate bias. Since the defect-pool model predicts that the DB states density depends on the Fermi-level position, one can expect to change the DOS by changing the gate voltage, if this is applied at a temperature above the equilibration temperature in order for the defect density to equilibrate in a reasonable time (such a gate voltage applied at high temperature is defined as the bias-anneal voltage V_{ba}). We suggest to use the quasistatic capacitance of metal-insulator-semiconductor (MIS) structures to detect these DOS changes. The advantage of using MIS structures rather than TFT's is that the semiconductor layer can be made thick enough (much thicker than the intrinsic Debye length of a-Si:H), so that band bending near the insulator/semiconductor (I/S) interface becomes insensitive to the rear interface states that can affect the transfer characteristics of TFT's.[13] Moreover, in a recent paper, it has been shown that the shape of the quasistatic capacitance curve of MIS structures as a function of the gate voltage (which will be simply denoted C-V curve in the following) is very sensitive to the shape of the DOS in a *homogeneous* amorphous semiconductor MIS structure, where the density of defects is homogeneous across the semiconductor.[14] In this paper, we show that quasistatic C-V curves are still sensitive to details of the DOS in the framework of the defect-pool model, wherein the distribution of defects across the semiconductor layer can be highly *non-homogeneous*, depending on the bias-anneal voltage. We present the theoretical quasistatic C-V curves expected for a set of bias-anneal voltages ranging from electron accumulation to hole accumulation. Finally, we present experimental bias-annealing data obtained on aluminum/silicon dioxide/a-Si:H structures and discuss the ability of the defect-pool model to account for the changes in defect densities observed in these a-Si:H based field-effect devices.

Our theoretical C-V curves were obtained in two steps. In the first step, for a given bias-anneal voltage, we calculated the equilibrated DB states distribution in the whole semiconductor layer. Several recent calculations can be found in the literature for the density of DB states in the framework of the defect-pool model.[5,9] These differ in the details of the microscopic reactions and in some assumptions, but the orders of magnitude and the main tendencies of the defect densities resulting from these different calculations are quite the same. In the following, we shall use the defect-pool formulas given by Powell and Deane in Ref. 6, with the values of the defect parameters listed in Table I, which are standard values for a-Si:H. The major characteristic of the defect-pool model is that the density of DB states strongly depends on the Fermi-level position. This is illustrated in Fig. 1, where we show the defect-pool DOS $D(E)$ and the one electron DOS defined by $g(E)=D[E+kT\ln(2)]+D[E-U-kT\ln(2)]$,[6] for three values of the Fermi-level position. It can be seen that

TABLE I. Defect-pool parameters used to calculate the densities of states of Fig. 1 and the theoretical quasistatic capacitance of Figs. 2 and 3. VB and CB are used for valence band and conduction band, respectively.

Bias-annealing temperature T_{ba} (K)	473
Characteristic temperature of the VB-tail T_v (K)	600
Characteristic temperature of the CB-tail T_c (K)	300
DOS at the VB-edge $N(E_v)$ (cm^{-3} eV^{-1})	2×10^{21}
DOS at the CB-edge $N(E_c)$ (cm^{-3} eV^{-1})	1×10^{21}
Hydrogen Concentration $[H]$ (cm^{-3})	5×10^{21}
Defect-pool characteristic width σ (eV)	0.178
Position of the pool maximum E_p-E_v (eV)	1.27
Gap energy E_G (eV)	1.9
Correlation energy of the DB states U (eV)	0.2
Measurement temperature T_m (K)	353

the DOS is quite flat if the Fermi level is in its intrinsic position (curve b). Shifting the Fermi level towards the conduction band leads to an exponential increase of negatively charged DB states that form in the lower part of the gap (curve a), the position of the maximum being defined by the energy position of the pool maximum E_p, the pool width σ, and the characteristic width of the valence band tail kT_v. Similarly, shifting the Fermi level towards the valence band leads to an exponential increase of positively charged DB states that form in the upper part of the gap (curve c), the maximum being located at E_p. Since the density of DB states depends on the position of the Fermi level within the gap, the distribution of DB states across the semiconductor layer was obtained by solving self-consistently Poisson's equation using a finite difference method, taking all the contributions to the charge density into account: free electrons and holes, and band-tail states and dangling bonds. The equilibrium temperature was chosen equal to 200 °C, as suggested by thermal quenching experiments.[15–17]

In the second step, this DB states distribution was frozen in at the measurement temperature ($T_m=80$ °C). Then, for any value of the gate voltage V_G, we solved Poisson's equation in order to get the band bending and to deduce the

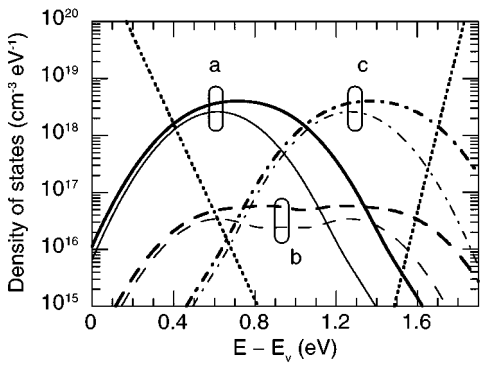

FIG. 1. Density of dangling bond states $D(E)$ (thin lines) and one-electron density of states $g(E)$ (bold lines) as a function of the energy E referred to the valence-band edge E_v, as predicted by the defect-pool model with the parameters listed in Table I for three values of the Fermi-level position: (a) $E_F-E_v=1.46$ eV, (b) $E_F-E_v=1.04$ eV, and (c) $E_F-E_v=1.62$ eV. Also shown in dotted lines are the two exponential band-tail states distributions.

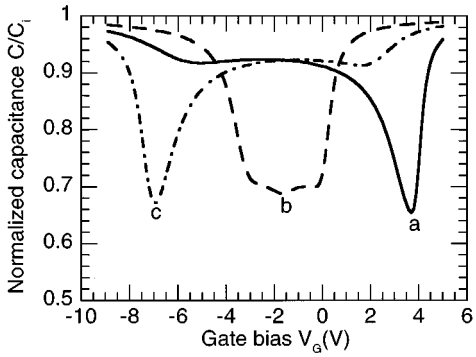

FIG. 2. Theoretical quasistatic capacitance curves as a function of the gate bias (C-V curves) for three dangling bond states distributions calculated from the defect-pool model using the parameters listed in Table I. These three curves labeled (a), (b), and (c) correspond to dangling bond states distributions such that the densities of states at the insulator/semiconductor interface are those labeled (a), (b), and (c), respectively, in Fig. 1.

corresponding charge induced on the metal gate Q_M. The C-V curve was then obtained by differentiating Q_M with respect to V_G. To account for our experimental insulator characteristics, we took values of the dielectric permittivity and thickness equal to $\varepsilon_i=0.33\times10^{-12}$ F cm^{-1} and $x_i=840$ Å, respectively, and we also introduced a fixed positive charge Q_i equivalent to a surface density of 2.5×10^{11} cm^{-2}. Concerning the semiconductor, the band-tail states were taken as monovalent states, being of donor and acceptor type in the valence-band and conduction-band tail, respectively. Their density was chosen to be distributed exponentially in energy as can be seen in Fig. 1. The values of the characteristic temperatures T_v and T_c, as well as that of the DOS at the conduction-band and valence-band edge can be found in Table I.

All the C-V curves presented in the following are normalized to the value of the insulator capacitance C_i. Figure 2 shows the quasistatic C-V curves calculated for the three values of the bias-anneal voltage that yield the density of DB states at the I/S interface shown in Fig. 1. Thus, during bias annealing, the Fermi level at the I/S interface was at 1.46 eV, 1.04 eV, and 0.62 eV above the valence-band edge E_v for curves labeled (a), (b), and (c), respectively, and the corresponding values of the bias-anneal voltage V_{ba} were equal to $+3.5V$, $-1.7V$, and $-6.9V$, respectively.

Looking at curve (a) in Fig. 2, we observe that there is a sharp capacitance minimum ($C/C_i\approx0.65$) at $V_G\approx3.7V$. This sharp capacitance minimum reflects the sharp DOS minimum observed in Fig. 1 at the intercept between the one-electron density of DB states and the conduction-band tail ($E-E_v\approx1.5$ eV); in the following, this capacitance minimum will be called the CBT minimum. The capacitance strongly increases at higher gate biases, because the Fermi level near the I/S interface is swept into the exponentially increasing band-tail states. The capacitance also strongly increases at lower gate biases, because the Fermi level near the I/S interface is pushed into the DB states, whose density strongly increases towards midgap. The huge bump of defects thus leads to the broad capacitance bump extending down to $V_G\approx-5V$, where a secondary capacitance minimum is observed. This corresponds to the local minimum in

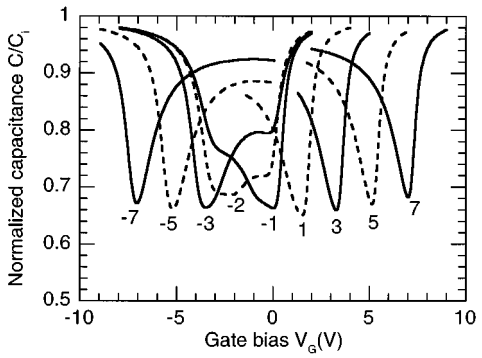

FIG. 3. Theoretical quasistatic C-V curves calculated at $T_m = 80\,^{\circ}\mathrm{C}$ using the parameters listed in Table I, after thermal bias annealing at $T_{\mathrm{ba}} = 200\,^{\circ}\mathrm{C}$ under different bias-anneal voltages. The value (in volts) of the bias-anneal voltage is indicated below each curve. For clarity, the curves are alternatively in plain and dashed lines, and some parts have been hidden.

the DOS at the intercept between the DB states distribution and the valence-band tail ($E - E_v \approx 0.4$ eV); in the following, this capacitance minimum will be called the VBT minimum. For curve (a) in Fig. 2, the VBT minimum is much less well defined than the CBT one, and its value is much higher ($C/C_i \approx 0.92$), because of the much higher DOS values in the corresponding energy range.

For the curves labeled (b), we observed that the quite flat density of DB states of Fig. 1 leads to a C-V curve exhibiting a quite flat minimum plateau in Fig. 2. This was already expected from our previous analysis of the C-V curves of MIS structures with a homogeneous defect density in the semiconductor layer.[14] Indeed, it is worth noticing that the Fermi level at the I/S interface was in its intrinsic position for curve (b) during bias annealing, meaning that the semiconductor has been bias annealed under flat-band conditions. This implies that the density of DB states is homogeneous across the whole semiconductor layer, as already pointed out by Powell and Deane,[9] so that the results of the analysis of Ref. 14 are expected.

For curve (c) in Fig. 2, we again observe two capacitance minima as for curve (a), but the main sharp one (at $V_G \approx -7V$) is now the VBT minimum, while the secondary one (at $V_G \approx 1.5V$) is the CBT minimum. Finally, from Figs. 1 and 2, we can conclude that in the framework of the defect-pool model that can give a strongly nonhomogeneous DOS, the shape of the C-V curve follows that of the one-electron DOS close to the I/S interface.

In Fig. 3 we show the theoretical quasistatic C-V curves that are calculated for a whole set of bias-anneal voltages using the defect-pool parameters listed in Table I, for which we know from the discussion above that the flat-band voltage V_{fb} is equal to $-1.7V$ (curves b in Figs. 1 and 2). Figure 3 emphasizes the changes that occur in the shape of the C-V curve if one changes the bias-anneal voltage.

For $V_{\mathrm{ba}} > -1V$, parts of the curves including the VBT minimum have been hidden for clarity reasons, and the sharp minimum exhibited by the C-V curves is the CBT minimum. We observe that the position of this capacitance minimum shifts to higher gate voltages as V_{ba} is increased. This can be explained as follows. During acquisition of the C-V curve, as the Fermi level near the I/S interface probes the minimum of the DOS at the intercept of the *conduction*-band tail with the DB states ($E_F - E_v \approx 1.5$ eV), practically all dangling bonds are *negatively* charged, because the peak of DB states is well *below* midgap (see Fig. 1). As V_{ba} is increased, the density of DB states increases so that there is an increasing negative charge in the semiconductor as one probes the CBT minimum. This results in a shift of the CBT minimum towards higher gate voltages. We also observe that, from $V_{\mathrm{ba}} = -1V$ to $V_{\mathrm{ba}} = +1V$, the CBT minimum slightly decreases, while for $V_{\mathrm{ba}} > +1V$, it slightly increases with V_{ba}. This reflects the fact that during bias annealing under moderate electron accumulation ($V_{\mathrm{ba}} < +1V$), in addition to the defect creation in the lower part of the gap, there is a defect removal in the upper part of the gap leading to a decrease of the density of DB states at the intercept with the conduction-band tail. During bias annealing under higher electron accumulation ($V_{\mathrm{ba}} > +1V$), the density of DB states increases whatever the energy, so that the DOS minimum also increases, leading to the observed increase of the minimum capacitance.

For $V_{\mathrm{ba}} < V_{\mathrm{fb}}$, the sharp minimum exhibited by the C-V curve is the VBT minimum, and we observe that its position shifts to lower gate voltages as V_{ba} becomes more negative. This can be explained in the same manner as the evolution of the minimum capacitance for $V_{\mathrm{ba}} > V_{\mathrm{fb}}$ discussed above. Indeed, during acquisition of the C-V curve, as the Fermi level probes the minimum of the DOS at the intercept of the *valence*-band tail with the DB states near the I/S interface, practically all the dangling bonds are *positively* charged, because the peak of DB states is well *above* midgap (see Fig. 1). This positive charge increases if V_{ba} becomes more negative, leading to the negative shift of the capacitance minimum. In addition, we also observe a slight decrease of the minimum capacitance from $V_{\mathrm{ba}} = -2V$ to $V_{\mathrm{ba}} = -3V$, followed by a slight increase as V_{ba} becomes more negative. This is because, during annealing, the density of DB states below midgap under hole accumulation behaves in the same manner as the density of DB states above midgap under electron accumulation. If the Fermi level during annealing is moved from the intrinsic position towards the valence band, the defect-pool model predicts first the removal and then the creation of DB states below midgap (in addition to the creation of DB states above midgap). This explains the evolution of the VBT minimum with V_{ba}.

We now turn to experimental results obtained on aluminum/silicon dioxide (SiO_2)/a-Si:H top gate structures. The SiO_2 layer was obtained by distributed electron cyclotron resonance plasma enhanced chemical vapor deposition, and earlier measurements have proved its high electrical quality.[18] More details on the fabrication of the devices and on the quasistatic C-V measurements are given elsewhere.[19]

The experimental quasistatic C-V curves are presented in Fig. 4. There is a striking resemblance between these experimental curves and those predicted by the defect-pool theory. Indeed, comparing Fig. 4 with Fig. 3, we observe that the main features of the C-V curves and the dependence of these curves upon V_{ba} are quite the same. We can consider three ranges of bias-anneal voltages. In the intermediate range, $-3V < V_{\mathrm{ba}} < -1V$, we clearly observe two capacitance minima. According to the results of Fig. 3 and to the discussion above, we can identify these minima with the VBT and CBT minima, and attribute them to the minima in the density

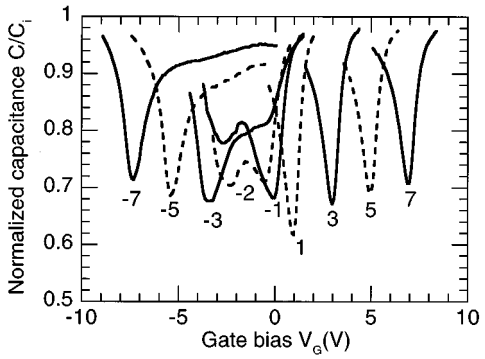

FIG. 4. Experimental quasistatic C-V curves obtained on our Al/SiO_2/a-Si:H structures, labeled according to the value (in volts) of the bias-anneal voltage.

of states occurring at the intercept of the DB states distribution with the valence-band and conduction-band tail states, respectively. We observe that the main minimum flips from the VBT minimum to the CBT minimum when the bias-anneal voltage changes from $-3V$ to $-1V$, suggesting that the flat-band voltage V_{fb} is approximately at $-2V$. In the range of bias-anneal voltages such that $V_{ba}>-1V$, we essentially observe that the sharp minimum, which we identify as the CBT minimum, is shifted to higher gate voltages when V_{ba} is increased, as predicted in Fig. 3. We also note that the minimum capacitance value first decreases, and then increases with V_{ba}, which is also predicted by the defect-pool model. In the range of bias-anneal voltages such that $V_{ba}<-3V$, the sharp minimum is identified as the VBT minimum, which also depends on V_{ba} just as predicted by the defect-pool model.

The origin of metastabilities in a-Si:H TFT's has been much debated in the past. Indeed, threshold voltage shifts can be explained either by defect creation in the semiconductor or by charge trapping in the insulator. It should be emphasized that charge trapping in the insulator would only produce a rigid shift of the C-V curve along the bias axis without any change in the shape of the curve. Since we observe strong changes in the shape of our C-V curves, it is clear that our results cannot be ascribed to charge trapping. Moreover, our numerical modeling indicates that these results can be well explained by changes in the defect densities as predicted by the defect-pool model without any charge trapping in the insulator. Thus, our quasistatic capacitance measurements provide a quantitative experimental evidence to the defect-pool theory.

Examining the details of the experimental C-V curves, we can, however, find two slight discrepancies with the model predictions. First, the value of the minimum capacitance seems to depend more strongly on the bias-anneal voltage than predicted by the defect-pool model. In particular, the decrease from $V_{ba}=-1V$ to $V_{ba}=+1V$ as well as the increase from $V_{ba}=+1V$ to $V_{ba}=+7V$ are stronger in Fig. 4 than in Fig. 3. At first sight, this could be attributed to the choice of the defect-pool parameters in Fig. 3. However, we believe that this is not the case, because we could not achieve a stronger dependence of the minimum capacitance value with V_{ba} in the theoretical C-V curves, whatever the values for these parameters. Work is still under way to precise the effect on the C-V curves of all defect-pool parameters, and the results, which are beyond the scope of this paper, will be published in the future. Second, for $V_{ba}=-1V$ and $V_{ba}=-2V$, we observe a bump in the C-V curves revealing the presence of a bump of midgap states that is not predicted by the defect-pool model. Two explanations can be suggested. The first one is the possible existence of a bump of interface states at the silicon dioxide/amorphous silicon interface. Indeed, the quasistatic capacitance is sensitive not only to the defects in the a-Si:H layer but also to interface states.[14] The second explanation is that there might be additional features in the density of the bulk states that are not included in the current modeling of defect formation in a-Si:H, and this deserves further theoretical investigation.

In summary, we have shown that the quasistatic capacitance of MIS structures is a powerful tool to study the changes in the defect density of a-Si:H that are induced by thermal bias annealing. The shape of our experimental C-V curves strongly depends on the bias-anneal voltage that proves that bias annealing induces strong changes in the density of states in a-Si:H. Our experimental data are in good agreement with the predictions of the defect-pool model and provide a conclusive support to this defect formation model. In particular, the quasistatic capacitance measurements reveal a broad bump of dangling bond states that is created either in the lower part of the gap or in the upper part of the gap, depending on whether bias annealing is carried out under electron or hole accumulation.

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