Single-electron transport in small resonant-tunneling diodes with various barrier-thickness asymmetries

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We fabricated submicrometer-diameter double-barrier diodes from four wafers with different barrier-thickness asymmetry. All samples exhibit staircaselike features in the current-voltage characteristic at the current threshold due to single-electron tunneling. Our study focuses on the properties of the first current step which arises from tunneling through the energetically lowest discrete electron state within the double-barrier region. The analysis of the bias position of the step allows a spatial spectroscopy of the vertical position of the lowest discrete level in the double-barrier region. The magnitude of the step is in excellent agreement with theory for all barrier-thickness asymmetries whereas the broadening of the step edge exceeds the lifetime-related width of the discrete state by one order of magnitude. [S0163-1829(96)07743-0]

I. INTRODUCTION

Single-electron tunneling through zero-dimensional (0D) states in double-barrier diodes attracted considerable experimental and theoretical interest in recent years.[1–26] Experimentally, two different methods were employed to investigate discrete states by tunneling: On one hand, quantum dots with 0D states were generated by adding a lateral confinement to the vertical double-barrier confinement by etching submicrometer-diameter pillars,[1–10] focused ion-beam writing,[11,12] or hydrogen-plasma-induced depletion.[13] On the other hand, tunneling through discrete impurity-related states in the quantum well of large-area devices was studied.[14–21] In both cases, staircaselike features are observed at the onset of the current in the current-voltage characteristic. These steps are known to arise from consecutive tunneling events of single electrons through discrete electron levels.

The purpose of this work is a detailed analysis of single-electron tunneling through small double-barrier structures as a function of the barrier-thickness asymmetry. This parameter determines the occupation probability of discrete electron states in the quantum well.[25] Our study is based on four wafers with different barrier-thickness asymmetry. In order to fabricate laterally-confined devices with discrete states, we etched submicrometer-diameter pillars from these wafers. All devices exhibit staircaselike features in the low-temperature current-voltage characteristics due to single-electron tunneling. Particular emphasis is put on the properties of the first current step in the current-voltage characteristics which is the consequence of tunneling through the energetically lowest discrete level within the double-barrier region. Our paper is organized as follows: The fabrication of submicrometer-diameter devices is described in Sec. II. Section III is devoted to a general discussion of staircaselike features exhibited by the current-voltage characteristics. In Sec. IV we focus on the first current step. This step is analyzed with respect to its position in bias, to its magnitude in current, and to the broadening of its edge. The experimental results for these three parameters are compared with theoretical predictions as a function of the barrier-thickness asymmetry. In Sec. V, we give a brief summary of our results.

II. SAMPLE PREPARATION

In order to cover a wide range of barrier-thickness asymmetries systematically, four double-barrier heterostructures were grown by molecular beam epitaxy on an n^+-type GaAs substrate as follows[27]: A 10 nm wide GaAs well is embedded between two $Al_{0.3}Ga_{0.7}As$ barriers. The thickness of the bottom barrier b_b varies in steps of 1 nm from 6 nm to 9 nm while the top-barrier thickness is fixed at 5 nm (i.e., structures 5/6, 5/7, 5/8, and 5/9). Contact layers of 300 nm GaAs, n-doped with Si to 4×10^{17} cm^{-3} and separated from the intrinsic double-barrier region by undoped 7 nm wide spacer layers, complete the heterostructures.

Following the technique developed in Refs. 1 and 2, we fabricated devices with submicrometer diameter from the wafers. By employing electron-beam lithography and lift-off techniques, we deposited AuGe/Ni disks on the frontside of the wafer. These metallizations serve first as etch masks for the following reactive-ion etching step and second as Ohmic top contacts of the devices. AuGe/Ni was evaporated on the backside of the wafer as well in order to provide the bottom contact of the resonant-tunneling diodes. Using $SiCl_4$ for reactive-ion etching, we fabricated free-standing pillars with a diameter of several hundred nm and a typical height of 500 nm. The structures were planarized with a polyimide layer which was then partially etched back in oxygen plasma to reexpose the top contacts. The polyimide serves as an insulating base for large-area Cr/Ag/Au bond pads which were finally evaporated on top of individual devices by employing standard photolithography. Figure 1 shows both a sketch and a scanning-electron-microscope image of a typical sample before planarization.

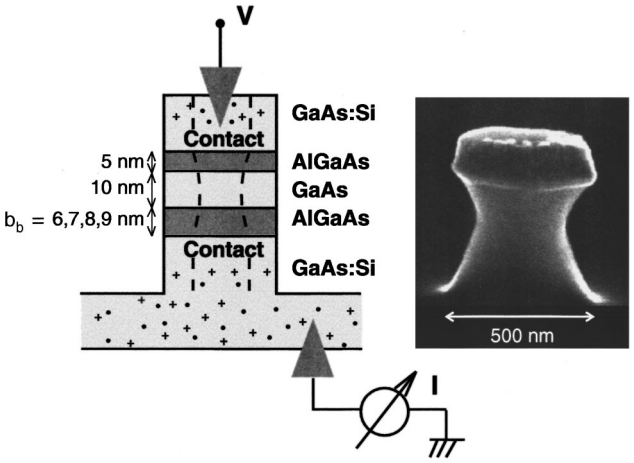

FIG. 1. Sketch and scanning-electron-microscope image of a submicrometer-diameter resonant-tunneling diode supplied with a metallic disk which serves as top contact. The dashed lines in the sketch illustrate the depletion layer at the pillar surface, which confines the electrons to the central core of the pillar.

III. CHARACTERIZATION

The dc current-voltage characteristics $I(V)$ of the samples were recorded in a dilution refrigerator operating at its base temperature of $T=23$ mK. The bias voltage was applied to the top contact with respect to the substrate. Figure 2 shows the threshold region of the $I(V)$ curves of four devices fabricated from the heterostructures 5/6, 5/7, 5/8, and 5/9 with

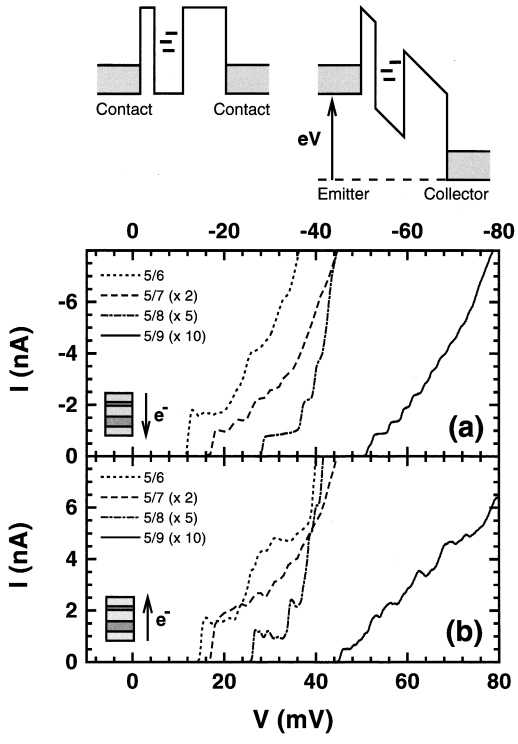

FIG. 2. Low-bias current-voltage staircases of four submicrometer diameter samples fabricated from the heterostructures 5/6, 5/7, 5/8, and 5/9 for negative (a) and positive bias polarity (b) ($T=23$ mK). The sketch above shows the energy diagrams of a resonant-tunneling diode with discrete states in the quantum well for zero and finite bias voltage.

TABLE I. Nominal pillar diameters d_p and current thresholds $V_s^{\pm}$ of the four devices considered in Fig. 2 as well as the calculated voltage-to-energy conversion coefficients $\alpha^{\pm}$ and occupation probabilities $n_s^{\pm}$ of the lowest discrete level S for both negative and positive bias. The values for $\alpha^{\pm}$ are valid if S is located at the center of the quantum well.

	d_p (nm)	V_s^-, V_s^+ (mV)	α^-, α^+	n_s^-, n_s^+
5/6	350	12.2,15.0	0.48,0.51	0.87,0.28
5/7	350	17.3,17.3	0.47,0.53	0.97,0.08
5/8	500	28.4,26.3	0.45,0.54	0.99,0.02
5/9	350	51.3,45.5	0.44,0.55	1.00,0.00

pillar diameters of $d_p=350-500$ nm, see Table I. Staircase-like features are observed in the current for both bias polarities as a consequence of single-electron tunneling from the emitter contact through discrete 0D states in the double-barrier region. The underlying physics is illustrated in the sketch of Fig. 2: At zero bias, all discrete levels in the quantum well lie above the Fermi level in the contacts, which prohibits resonant tunneling. Current steps occur whenever one of these levels becomes energetically available for transport by being pulled below the Fermi level in the emitter contact due to the applied bias voltage. The emitter states are of three-dimensional (3D) nature since the lateral quantization in the contacts is destroyed by doping-induced disorder.

The shape of the staircase depends strongly on the ratio Γ_E/Γ_C of the emitter- and collector-barrier tunneling rates. This ratio determines the occupation probability of the discrete levels in the quantum well. For $\Gamma_E \gg \Gamma_C$, electrons enter the quantum well rapidly but leave slowly, which leads to strong electron accumulation in the well. In the opposite case, $\Gamma_E \ll \Gamma_C$, electrons enter the quantum well slowly but escape rapidly. Hence, the accumulation of electrons in the well, or charging, is negligible. We distinguish the cases of *strong*, *intermediate*, and *weak* charging of the discrete levels which correspond to $\Gamma_E \gg \Gamma_C$, $\Gamma_E \approx \Gamma_C$, and $\Gamma_E \ll \Gamma_C$. For $\Gamma_E \gg \Gamma_C$ (heterostructures 5/7, 5/8, and 5/9 with negative bias), $I(V)$ staircases with smooth plateaus and steps of roughly equal height are observed. In ideal quantum dots with a soft lateral confinement potential, every step corresponds to an additional electron which is dynamically accumulated in the quantum dot by overcoming the electron-electron Coulomb repulsion, the so called Coulomb blockade.[4,8,25] Magnetotunneling measurements reveal that in our samples the staircases arise from an intricate combination of Coulomb blockade within the whole double-barrier region and fairly independent tunneling through several local potential minima in the double-barrier region. Such minima originate from single impurities inside the quantum well,[14] from potential fluctuations due to the heavily doped contacts,[15] or from well-width fluctuations.[28] It is interesting to note that the staircase of the device from wafer 5/7 starts with a step whose magnitude is roughly twice as large as that of the other steps. This is probably the consequence of tunneling through two independent local potential minima with almost equal energy. For $\Gamma_E \approx \Gamma_C$ (heterostructure 5/6 for both bias polarities), a complicated sequence of small steps

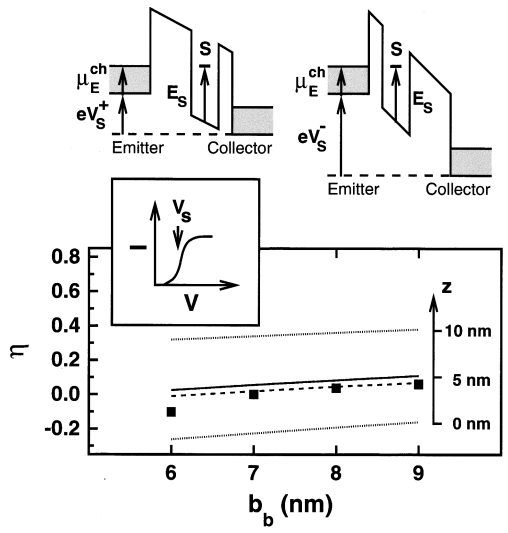

FIG. 3. Energy diagrams of an asymmetric double-barrier device which illustrate that the bias position of the first current step V_s is for negative bias larger than for positive bias. The plot below shows the relative difference $\eta=(V_s^- - V_s^+)/(V_s^- + V_s^+)$ as a function of the thickness of the bottom barrier. The experimental values (■) are compared with numerical results (connected by solid, dashed, and dotted lines, as explained in the text). The vertical position of the lowest 0D states in the 10 nm wide quantum wells is measured by the z axis from the lower dotted line, which corresponds to the interface between the thick barrier and the quantum well.

and wiggles is superimposed on the plateaus as a consequence of tunneling through excited states[4,10,25] and fluctuations of the density of states in the emitter.[10] These phenomena are concealed in case of $\Gamma_E \gg \Gamma_C$ but become even more pronounced for $\Gamma_E \ll \Gamma_C$ (heterostructures 5/7, 5/8, and 5/9 with positive bias).

IV. CURRENT STEP ANALYSIS

A. Step position

In the following, we focus on the first single-electron-tunneling current step which is due to tunneling through the energetically lowest discrete state S with energy E_s. The condition for the observation of the first current step is given by

$$V_s=(E_s-\mu_E^{ch})/e\alpha \tag{1}$$

with μ_E^{ch} the chemical potential in the emitter (see the sketch in Fig. 3). Here, E_s and μ_E^{ch} are evaluated from the conduction-band edge in the quantum well and emitter, respectively. The voltage-to-energy conversion coefficient $\alpha \approx 0.5$ is proportional to the part of the bias voltage which drops between the emitter contact and the discrete level S in the quantum well. Table I shows that V_s is for the devices fabricated from wafers 5/6, 5/7, and 5/8 about $20-30$ mV smaller than for the device made from heterostructure 5/9. We want to emphasize that this effect is not correlated with the pillar diameter of the devices, since all devices are far from pinch-off, i.e., all pillar diameters are larger than twice the width of the depletion layer at the pillar sidewall measured to be 50–100 nm in our double-barrier structures.[27] According to Eq. (1), the difference corresponds to a 10–15 meV smaller energy E_s which is close to the binding energy of a donor in the center of a 10 nm wide quantum well.[29] Hence, our interpretation is that S is provided in the samples from wafers 5/6, 5/7, and 5/8 by an unintentional donor in the quantum well (in contrast to the device from heterostructure 5/9). This conclusion is supported by an estimate of the lateral extension of the wave functions of S in the four samples from the magnetic-field dependence of E_s (in analogy to Ref. 8).

For a given device, we expect the first current step to occur for negative bias at higher absolute voltage than for positive bias, $V_s^- > V_s^+$, since for positive bias a larger part of the applied voltage drops accross the emitter barrier than for negative bias due to the barrier-thickness asymmetry, i.e., $\alpha^+ > \alpha^-$. This effect is shown by the sketch in Fig. 3. For the more asymmetric devices (wafers 5/8 and 5/9) we observe indeed $V_s^- > V_s^+$ whereas the sample fabricated from heterostructure 5/6 shows the opposite behavior.

For a quantitative treatment, we define the relative difference of V_s^- and V_s^+ as test parameter η. From to Eq. (1), we derive

$$\eta=\frac{V_s^- - V_s^+}{V_s^+ + V_s^-}=\frac{\alpha^+ - \alpha^-}{\alpha^+ + \alpha^-}. \tag{2}$$

Figure 3 compares the measured relative differences of V_s^- and V_s^+ with values obtained by calculating α^+ and α^-. The conduction-band profile required the calculation was computed with a one-dimensional Poisson solver in Thomas-Fermi approximation, in order to take the voltage drops in the contacts due to electron accumulation at the emitter barrier and electron depletion at the collector barrier into account. Since $\alpha^{\pm}$ depends weakly on the applied bias voltage, each sample was biased at $V_s^{\pm}$ in the calculation. Moreover, it was assumed that S is located at the center of the quantum well, i.e., at a distance of 5 nm from each barrier. Table I gives $\alpha^{\pm}$, as evaluated using the nominal layer parameters. The solid line in Fig. 3 connects the corresponding values for η, which exceed the experimental results.

In order to reveal the origin of this discrepancy, we discuss first the influence of the spacer thicknesses on η: As a consequence of growth-induced donor segregation from the bottom contact, the bottom spacer layer is expected to be thinner than the nominally grown 7 nm. The top spacer layer is expected to be wider than 7 nm for the same reason. Therefore, the part of the bias voltage that drops in the bottom spacer is reduced while the voltage drop across the top spacer is increased. This reduces α^+ and increases α^-, i.e., η is reduced. In order to get an upper limit for this effect, we assume a vanishing bottom spacer and a top spacer thickness of 14 nm. Although good agreement between the computed values (dashed line in Fig. 3) and experiment is obtained for the devices from wafers 5/7, 5/8, and 5/9, a striking deviation remains for the sample from wafer 5/6. This calculation demonstrates that the influence of the spacer thicknesses on η is small, in particular if more realistic thicknesses than above are considered.

Second, we study the influence of the vertical position of S in the quantum well on η: The upper dotted line in Fig. 3 was calculated for S located exactly at the interface between

the quantum well and the thin top barrier, the lower dotted line results for S located at the interface between the thick bottom barrier and the quantum well. Here, we used the nominal layer parameters for the calculation. In principle, all values between the two dotted lines are possible, depending on the vertical position of S in the quantum well. Note, however, that the vertical position of S is determined by the center of mass of the probability density of its wave function. Thus, the vertical positions of S and of the corresponding potential minimum are typically close but in general not identical due to the repulsive influence of the barriers on the wave function. If S is related to a donor located at one of the interfaces between the quantum well and the barriers, for example, its wave function is pushed by the barrier into the quantum well, i.e., the vertical position of S is within the quantum well though close to the interface.

Summarizing all numerical results, we conclude that η is only weakly dependent on the spacer thicknesses but very sensitive to the vertical position of S in the quantum well. The comparison of the experimental value of η with theory allows us thus to determine the vertical position of discrete states in double-barrier heterostructures. We estimate the accuracy of this spatial spectroscopy to 1 nm, limited by possible deviations of the actual heterostructure parameters from the nominal ones.

The method is exemplified by the z axis in Fig. 3. It measures the position of S in the quantum well from the lower dotted line, which corresponds to the interface between bottom barrier and quantum well. For the device from wafer 5/6, for example, we find that S is located at a distance of 3 nm from the bottom barrier. This conclusion complies with detailed $I(V)$ measurements in magnetic field,[10] where we deduced from the separation between the ground state and the first excited levels of the local potential minimum that it is provided by an off-center donor close to one of the barriers.

Note that S is in all samples considered in Fig. 3 located closer to the bottom barrier than to the top one. In order to check the relevance of this common feature, we analyzed a large number of single-electron-tunneling steps in many different devices processed from all four wafers. The corresponding 0D states are typically located at a distance of $2-5$ nm from the bottom barrier which was grown first during epitaxy. This provides strong evidence that the majority of the discrete states arises from growth-induced segregation of Si donors from the bottom contact into the nominally undoped double-barrier region.

B. Step magnitude

Figure 4 shows that the magnitude ΔI of the first step decreases fairly exponentially with increasing bottom-barrier thickness for both bias polarities (values are corrected according to the number of independent contributing 0D levels). The current-step height is related to the emitter- and collector-tunneling rates $\Gamma_E \approx T_E \mu_E^{ch}/\hbar$ and $\Gamma_C \approx T_C E_0/\hbar$ through

$$\Delta I = 2e\Gamma_E\Gamma_C/(2\Gamma_E+\Gamma_C) \tag{3}$$

(with T_E and T_C the emitter- and collector-barrier transmission coefficients and E_0 the energy of the quasi-two-dimensional subband in the quantum well).[24] This formula is based on sequential tunneling and holds for arbitrary charging conditions. The current-step height is dominantly controlled by the thicker barrier: In the strong charging limit ($\Gamma_E \gg \Gamma_C$), the current-step height is determined by the collector-barrier tunneling process, $\Delta I \approx e\Gamma_C$. In the weak-charging limit ($\Gamma_E \ll \Gamma_C$) results $\Delta I \approx 2e\Gamma_E$, i.e., the magnitude of the current step is determined by the emitter-barrier tunneling process. The factor 2 stems from the possibility for electrons of either spin to tunnel independently through an empty spin-degenerate level. In the strong charging case, the level is always occupied with one electron, and Coulomb repulsion prevents a second electron of opposite spin from tunneling.

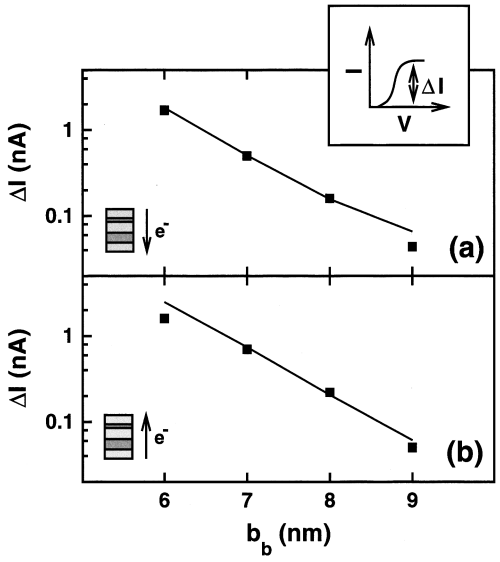

FIG. 4. Dependence of the height of the first current step (inset) on the thickness of the bottom barrier for negative (a) and positive bias polarity (b). The experimental step heights (■) are compared with numerical results which are connected by a solid line.

The current on the plateau which follows the first step increases with bias in the strong charging limit whereas it decreases in the weak charging limit. This phenomenon is in Fig. 2 most clearly exhibited by the devices fabricated from heterostructures 5/8 and 5/9. In the strong charging case, the current $\Delta I \approx e\Gamma_C$ increases with bias because the effective collector-barrier height is reduced (with respect to the energy of S) and the density of final 3D collector states is increased (at the energy of S). In the weak charging limit, in contrast, the current $\Delta I \approx 2e\Gamma_E$ decreases with bias since the effective emitter-barrier height increases (with respect to the energy of S) and the density of initial 3D emitter states decreases (at the energy of S).

Using Eq. (3), we calculated the current-step height after computing the tunneling rates based on the self-consistently obtained conduction-band profile of the devices. Figure 4 reveals good agreement of numerical results and experimental data independent of the barrier-thickness asymmetry. This agreement confirms not only that the staircases arise indeed from single-electron tunneling but it shows, moreover, that the actual barrier thicknesses of the heterostructures match the intended values very well.

The calculation demonstrates also that our experiment

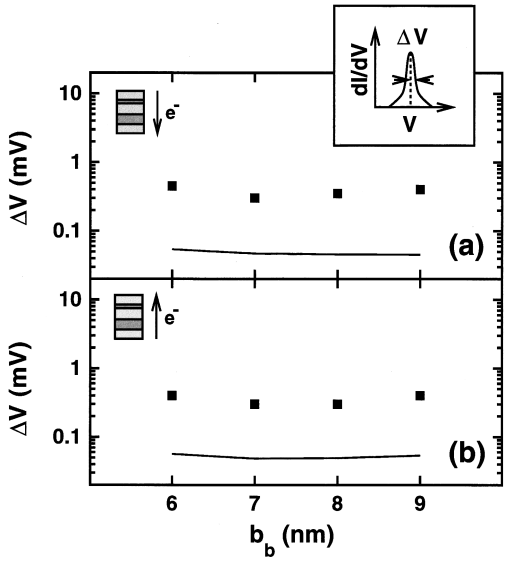

FIG. 5. Dependence of the broadening of the step edges on the thickness of the bottom barrier for negative (a) and positive bias polarity (b). The broadening was deduced as half width at half maximum of the corresponding peak in the differential conductance (inset). The experimental results (■) are compared with calculated values of the lifetime broadening of the resonant level (connected by a solid line).

covers for negative bias the time scale of $\Gamma_C^{-1}\sim 10^{-10}-10^{-9}$ s with $\Gamma_E^{-1}\sim 10^{-11}$ s and for positive bias the regime of $\Gamma_E^{-1}\sim 10^{-10}-10^{-8}$ s with $\Gamma_C^{-1}\sim 10^{-11}$ s. The ratio of the tunneling rates varies over five orders of magnitude, $\Gamma_E/\Gamma_C\sim 10^{-3}-10^{2}$, while the occupation probability of the discrete level[24]

$$n_s=\Delta I/e\Gamma_C=2\Gamma_E/(2\Gamma_E+\Gamma_C) \tag{4}$$

varies from zero to one, see Table I.

C. Step edge

The current steps exhibit a finite broadening at the edge. This broadening can be measured as half width at half maximum of the corresponding peaks in the differential conductance. Figure 5 shows that the experimental result is of the order of $\Delta V\approx 0.4$ mV with no significant dependence on either the barrier-thickness asymmetry or the bias polarity. For comparison we calculated the lifetime broadening of the quasibound states

$$\Delta V=\Delta E/e\alpha=\hbar(\Gamma_E+\Gamma_C)/2e\alpha \tag{5}$$

from the natural linewidth $\Delta E=\hbar/2\tau$ with $\tau=1/(\Gamma_E+\Gamma_C)$ denoting the intrawell lifetime.[30] It is similarly independent of both the barrier-thickness asymmetry and bias polarity since the lifetime is dominantly determined by the decay through the thin barrier whose thickness remains unchanged.

The calculated values are, however, more than one order of magnitude smaller than the experimental results. Thermal broadening does not explain this discrepancy since k_BT is at $T=23$ mK even smaller than the natural linewidth. Scattering processes, current-induced Joule heating of the electron bath in the contacts as well as electromagnetic ac pickup of the measurement circuit were previously invoked as explanations for similar experimentally observed extra broadenings.[2,4] In our case, we estimate the ac pickup signal in the measurement circuit to be much smaller than the observed width of $\Delta V\approx 0.4$ mV.[31] Joule heating of the electron bath in the emitter contact and the voltage drop at Ohmic contact resistances do not account for the observed phenomenon as well: Both effects increase the width but, in contrast to our experimental results, they become more pronounced with increasing current-step height, i.e., with decreasing thickness of the bottom barrier. Scattering processes in the double-barrier region can be also ruled out: Interface-roughness and impurities in the double-barrier region are no source for elastic scattering but contribute to the potential landscape which defines the lowest 0D state. Inelastic LO phonon emission during tunneling may lead to a replica of the first current step at a bias voltage of $V_s+\hbar\omega_{\mathrm{LO}}/e\alpha$, but does not cause any extra broadening of the step edge (with $\hbar\omega_{\mathrm{LO}}/e\alpha\approx 70$ mV using $\hbar\omega_{\mathrm{LO}}=36$ meV as LO-phonon energy of GaAs).

Recently, Imam *et al.*[32] suggested that the interaction of tunneling electrons with charged donors in the depletion layer of the collector contact can generate an anomalously large broadening. This mechanism depends, however, on the ratio of the tunneling rates Γ_E/Γ_C, i.e., on the barrier-thickness asymmetry and bias polarity, which contradicts the observed independence of the extra broadening of this parameter.

Now, we discuss the influence of scattering processes in the contacts. Inelastic scattering in the collector contact is irrelevant for the width of the current-step edge: the tunneling electrons which form the edge have an excess energy of eV_s in the collector measured from the Fermi level. The energy relaxation which follows tunneling is in the device fabricated from heterostructure 5/9 much faster than in all others, since the excess energy is solely in this sample higher than the LO-phonon energy $\hbar\omega_{\mathrm{LO}}$. Therefore, if inelastic scattering in the collector were the origin of the extra broadening, the width of the step edge would be in the device from wafer 5/9 much larger than in the others, in contrast to experiment.

Scattering processes in the emitter contact are, however, a possible source for the observed extra broadening: The relaxation of the holes generated by tunneling electrons in the emitter due to inelastic scattering leads to a broadening reflected in the width of the edge of the current steps. Even elastic electron-impurity scattering processes were reported to broaden the energy distribution function at the Fermi edge.[33] Extra broadening due to scattering processes in the emitter should be independent of the barrier-thickness asymmetry in agreement with our experiment.

Very recently, extremely sharp current-step edges of the order of $\Delta V\sim 0.05$ mV were observed in two experiments on symmetric resonant-tunneling diodes.[17,20] The employed double-barrier structures had, however, very low transparency barriers with a several orders of magnitude longer natural lifetime compared with our devices, i.e., not only the measured broadening of the step edge but also the theoretical lifetime broadening were far smaller than in our case. Moreover, both experiments were performed on large-area samples whereas we report on submicrometer-diameter de-

vices. The size difference appears to be crucial: We observed a current-step edge of $\Delta V \approx 0.15$ mV width in a larger device with 2 μm diameter from wafer 5/8. Although this value is still larger than the calculated lifetime broadening, it is considerably smaller than $\Delta V \approx 0.4$ mV obtained for the submicrometer-diameter devices.

According to above discussion, scattering processes in the emitter contact are a plausible reason for the extra width of the current-step edge in our devices, although the detailed mechanism is not clear at the moment.

V. SUMMARY

We studied resonant transport in small double-barrier heterostructures as a function of the barrier-thickness asymmetry. Staircaselike features were observed in the current-voltage curves due to single-electron tunneling through discrete energy levels. The barrier-thickness asymmetry controls the occupation probability of these states. From the dependence of the position of the first current step on the bias polarity, we are able to estimate the vertical position of the lowest discrete state in the quantum well. In most of the samples it is located close to the bottom barrier, which provides strong evidence for growth-related donor segregation from the heavily doped bottom contact into the nominally undoped double-barrier region. The height of the first current step is in good agreement with theory independent of the barrier-thickness asymmetry. In contrast, the broadening of the step edge exceeds the calculated natural linewidth of the discrete levels by one order of magnitude. Scattering processes in the emitter contact are a possible source for this extra broadening.

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