Weak localization in back-gated $Si/Si_{0.7}Ge_{0.3}$ quantum-well wires fabricated by reactive ion etching

S. J. Koester, K. Ismail, K. Y. Lee, and J. O. Chu
IBM Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598
(Received 20 May 1996)

The electronic properties of $Si/Si_{0.7}Ge_{0.3}$ quantum-well wires fabricated by reactive ion etching are investigated. The width of the nonconducting layer produced by the dry-etch damage and surface depletion is determined by plotting the conductance vs wire width for wires with lithographic widths ranging from 0.10 to 1.0 μm. The combined width of the so-called ''dead layers'' on each edge of the wire is determined to be as small as 0.13 ± 0.01 μm. Quantum interference effects are studied in wires with lithographic widths of $W=0.23$ μm. One-dimensional (1D) weak localization is evident in these wires at $T=1.3$ K in the form of a pronounced negative magnetoresistance for $|B|\leqslant 0.3$ T. A back-gate contact is used to study the electron-transport properties in the wires, as a function of the electron sheet concentration, n_s. The data have been fitted to the 1D theory of weak localization, and indicate that the inelastic mean free path L_ϕ increases from 0.2 to 1.2 μm as n_s is increased from 4.2×10^{11} to 5.9×10^{11} cm^{-2} at $T=1.3$ K. [S0163-1829(96)01239-8]

Recent improvements in the quality of $Si/Si_{1-x}Ge_x$ strained-layer heterostructures have produced two-dimensional (2D) systems with very high electron (and hole) mobilities.[1–4] Electron mobilities $>5\times10^5$ cm^2/V s (Ref. 3) (and hole mobilities $>5\times10^4$ cm^2/V s) (Ref. 2) have been obtained at low temperatures ($T\leqslant 4.2$ K) in modulation-doped $Si/Si_{1-x}Ge_x$ quantum wells. These values are an order of magnitude greater than the best mobilities achieved in Si/SiO_2 MOS structures. Such results offer promise for the observation of several quantum-mechanical phenomena in Si, and potentially the operation of various quantum devices. However, before such devices can be implemented, it is important to understand the nature of quantum transport in mesoscopic geometries.

The weak-localization effect is a powerful tool for extracting relevant parameters such as the phase-coherence length L_ϕ and the dephasing time τ_ϕ in 2D and 1D systems.[5] Weak localization is caused by the constructive interference between time-reversed electron paths, which leads to a decreased conductivity compared to the classical value. Application of a magnetic field causes a phase shift between the time-reversed paths and a suppression of the weak localization.[6] Several studies of this phenomenon have been performed in both n- and p-type $Si/Si_{1-x}Ge_x$ heterostructures.[7–9] However, these analyses have been restricted to 2D samples. Though fitting the magnetoresistance data to theory is perhaps more accurate in 2D systems,[5] it is important to study transport in lower-dimensional structures, because such systems are more relevant to potential quantum device applications. In this paper, we describe our study of weak localization in narrow $Si/Si_{0.7}Ge_{0.3}$ quantum-well wires fabricated by reactive ion etching. We utilize the unique back-gating properties of this material system[10] to describe the phase-coherent electron transport as a function of electron concentration in the wires.

The heterostructure layers used in this work are grown on a $\rho=11-25$ Ω cm p-type Si substrate using ultrahigh-vacuum chemical vapor deposition (UHV-CVD) in the temperature range of 500–550 °C. A 1-μm-thick $Si_{1-x}Ge_x$ buffer layer graded from $x=0$ to 0.30 is first grown to provide a virtual substrate for the ensuing layer structure. Following a 1-μm-thick layer of $Si_{0.7}Ge_{0.3}$, a 10-nm tensilely strained Si quantum well is grown. An 8-nm-thick

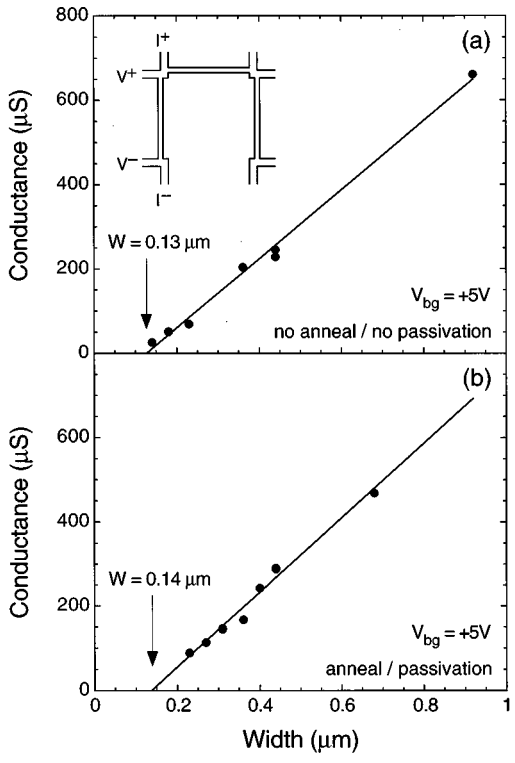

FIG. 1. Plot of conductance vs lithographic wire width for 10-μm-long wires (a) with no post-processing treatment ($S1$), and (b) passivated with 50 nm of SiO_2, and annealed at 575 °C for 1 h after etching ($S2$). In both plots, the solid circles are the experimental points, and the line is a least-squares best-fit straight line to the experimental points.

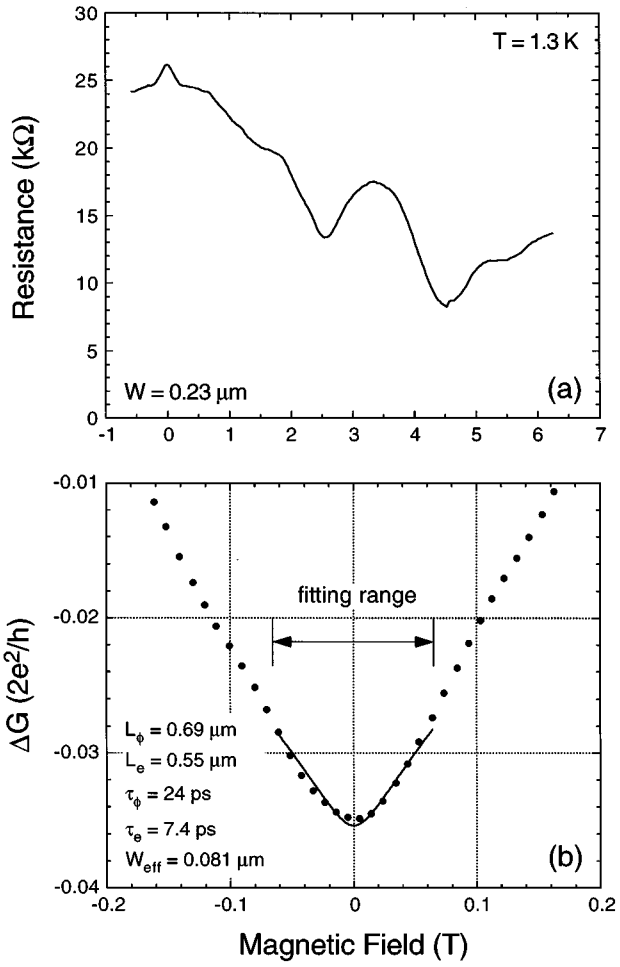

FIG. 2. (a) Typical magnetoresistance characteristic for a wire in set ($S2$) with lithographic width of 0.23 μm, at $T=1.3$ K. Shubnikov–de Haas oscillation are observed at high fields, and a negative magnetoresistance due to weak localization is apparent at low fields. (b) Weak-localization correction to the conductance ΔG, plotted vs magnetic field. The solid points are the experimental data, and the solid curve is a fit of the BvH 1D weak-localization theory (clean limit, specular boundary scattering) using the adjustable parameters L_ϕ and $W_{\rm eff}$. These values are listed in the plot along with other relevant device parameters. The back-gate bias for both plots is $V_{\rm bg}=+1.0$ V.

$Si_{0.7}Ge_{0.3}$spacer layer is next grown, followed by a 10-nm $Si_{0.7}Ge_{0.3}$ supply layer with a doping concentration of $N_D=2$–3×10^{18} cm^{-3}. Finally, the layers are capped with 5 nm of Si to provide a stable surface for subsequent processing; all layers other than the supply layer are unintentionally doped. Shubnikov–de Haas (SdH) measurements using a van der Pauw geometry at $T=2$ K reveal an electron sheet concentration and electron mobility of $n_s=6.9\times10^{11}$ cm^{-2} and $\mu_e=1.3\times10^5$ cm^2/V s, respectively. Though we have grown layers with higher mobilities, this particular layer structure was chosen because its high electron concentration makes it suitable for fabrication of structures with very small lateral dimensions. Wires with lengths of 10 μm, and widths varying from 0.04 to 1.0 μm have been fabricated by electron-beam lithography using an IBM proprietary negative resist, and then using the resist as a mask for CF_4 reactive ion etching (RIE). The etch conditions are as follows: the applied rf power is 10 W, the gas flow rate is 10 sccm, the pressure is 10 mTorr, the dc bias is -60 V, and the etch time is 6.1 min. A laser reflectance system is used during the RIE step to enable termination of the etch in the Si quantum well, corresponding to an etch depth of 23–33 nm. Both the etch depth and the wire widths have been confirmed by inspection of the samples in a scanning electron microscope. Two sets of wires are examined: one with no post-etching treatment ($S1$); and the other ($S2$) passivated with 50 nm of SiO_2, deposited by low-temperature CVD, and then annealed in a furnace for 1 h at $T=575$ °C. The back-gate contact is created by blanket evaporation of Ag onto the back side of the Si substrate, followed by annealing for 1 min at $T=400$ °C.

In order to determine the effect of process damage on the wire characteristics, the dc four-point conductance of wires with widths varying from $W=0.10$ to 1.0 μm has been measured at $T=4.2$ K. Figure 1 shows a plot of the conductance G, vs lithographic width W for wire sets $S1$ and $S2$. The measurement configuration of the wires is shown in the inset. In both cases, a bias of $V_{\rm bg}=+5$ V is applied to the back-gate contact. The results show similar behaviors for $S1$ and $S2$, where G decreases linearly with decreasing W. Wires with lithographic widths as small as $W=0.14$ μm are found to be conducting. A least-squares best-fit straight line to the data points (indicated by the solid line) shows a positive-x intercept, the value of which corresponds to the width of the nonconducting regions at the edges of the wire, the so-called ''dead layers.'' The *combined* dead-layer widths determined by this method are 0.13 ± 0.01 and 0.14 ± 0.01 μm for $S1$ and $S2$, respectively. The relatively small dead-layer widths given above suggest that the fabrication procedure induces little damage to the high-mobility samples used in this work. The depletion caused by pinning of the Fermi level at the surface is thus the main reason for the dead layer.

The magnetoresistance behavior of both sets of wires has been studied at $T=1.3$ K. For these measurements, the resistance is measured as a function of perpendicular magnetic field. Once again the configuration shown in the inset of Fig. 1 is utilized, except that the resistance is measured using ac lock-in techniques. A driving current typically $\lesssim5$ nA is used to avoid heating effects. A typical plot of the magnetoresistance characteristic for a wire with a lithographic width of $W=0.23$ μm is shown in Fig. 2(a). SdH oscillations are observed at high fields ($|B|\gtrsim1$ T), and a pronounced negative magnetoresistance is observed in the low-field region ($|B|\lesssim0.3$ T). The latter behavior is attributed to the suppression of weak localization by a magnetic field.

Figure 2(b) shows a plot of ΔG vs B, where ΔG is the weak-localization correction to the wire conductance. The magnetoconductance data have been fitted to theory in order to extract material parameters such as L_ϕ and τ_ϕ. We have used the 1D theory of weak localization, originally developed by Al'tshuler and Aronov,[11] and later modified by Beenakker and van Houten (BvH).[12] In this formulation,

which is valid for $L_\phi \gg W_{\text{eff}}$, the change in the classical conductance due to weak localization is given by

$$\Delta G(B) = -N_\nu \alpha \frac{2e^2}{h} \frac{\sqrt{D}}{L} \left[\frac{1}{\sqrt{\tau_\phi^{-1} + \tau_B^{-1}}} - \frac{1}{\sqrt{\tau_\phi^{-1} + \tau_e^{-1} + \tau_B^{-1}}} \right], \quad (1)$$

where $N_\nu = 2$ is the valley degeneracy, α is an intervalley scattering parameter, D is the diffusion coefficient, L is the wire length, τ_ϕ and τ_B are the phase relaxation times due to inelastic collisions and the magnetic field, respectively, and τ_e is the elastic scattering time. W_{eff} is the width of the conducting channel in the wire. The so-called ''dirty'' limit described by Al'tshuler and Aronov occurs when $L_e \ll W_{\text{eff}}$, where $L_e = \nu_F \tau_e$ is the elastic mean free path, and ν_F is the Fermi velocity. In this case, $\tau_B = 3L_m^2/DW_{\text{eff}}$, where $D = \frac{1}{2}\nu_F L_e$ and $L_m \equiv \sqrt{\hbar/eB}$. Using $L_\phi = \sqrt{D\tau_\phi}$ and W_{eff} as adjustable parameters, Eq. (1) can be fitted to the magnetoconductance characteristic, such as the one shown in Fig. 2(b). W_{eff} enters through the elastic scattering time since $\tau_e = (m^*/Rn_s e^2)\,(L/W_{\text{eff}})$, where R is the classical value of the wire resistance. However, fitting Eq. (1) for the dirty limit of our data produces clearly unrealistic values of $L_\phi > 10$ μm and $W_{\text{eff}} < 1$ nm.

The ''clean'' limit, achieved when $L_e \gg W_{\text{eff}}$, is a more representative situation for our wires, since $L_e = 1.3$ μm in the as-grown 2D material. In this case, the magnetic dephasing time can be expressed as

$$\tau_B = \frac{C_1 L_m^4}{W_{\text{eff}}^3 \nu_F} + \frac{C_2 L_m^2 \tau_e}{W_{\text{eff}}^2}, \quad (2)$$

where (2) is an interpolation formula between the asymptotic expressions for the high- and low-field limits.[12] In the clean limit, the constants C_1 and C_2, as well as the diffusion coefficient D, depend on the type of boundary scattering. For purely specular boundary scattering, $C_1 = 9.5$ and $C_2 = 4.8$, and $D = \frac{1}{2}\nu_F L_e$. In the diffuse limit, $C_1 = 4\pi$ and $C_2 = 3$, and $D \approx (\nu_F W_{\text{eff}}/\pi)\ln(L_e/W_{\text{eff}})$. We find that using the diffuse boundary scattering values produces a poor fit to our data, and unrealistic values of L_ϕ and W_{eff}. However, all of our data can be fitted using the parameters for specular boundary scattering. The solid line in Fig. 2(b) shows the quality of this fit and the values of the some of the device parameters extracted from the data.

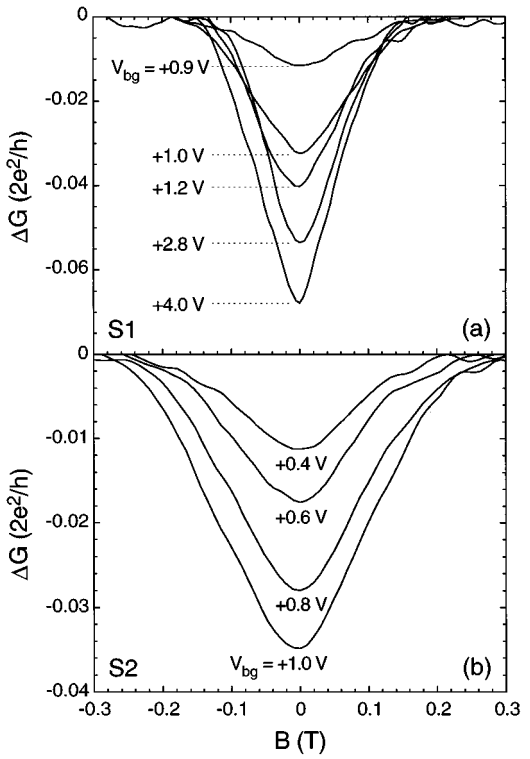

FIG. 3. Plot of the weak-localization correction to the conductance ΔG, vs magnetic field at various values of V_{bg} for (a) no anneal and no passivation ($S1$), and (b) anneal and passivation ($S2$). The temperature is $T = 1.3$ K.

We have studied the weak-localization characteristics of both wire sets $S1$ and $S2$ as a function of V_{bg}. The magnetoconductance results are shown in Figs. 3(a) and 3(b). In general, the weak-localization correction to the conductance increases with more positive values of V_{bg}, particularly for low values of V_{bg}. However, in $S2$, for values of $V_{\text{bg}} \gtrsim 2$ V, the weak localization disappears, while in $S1$ ΔG is seen to increase up to the highest back-gate voltage. (The suppression of the weak localization for large values of V_{bg} has been observed in other wires for both sets $S1$ and $S2$.) The data in Fig. 3 have been fitted to Eqs. (1) and (2) for specular bound-

TABLE I. Device parameters extracted from fitting the BvH 1D theory of weak localization to magnetoresistance data on wire set $S1$ (no anneal and no passivation).

V_{bg} (V)	W_{eff} (μm)	L_ϕ (μm)	L_e (μm)	n_s (10^{11} cm^{-2})	μ_e (10^4 cm^2/V s)	τ_ϕ (ps)	τ_e (ps)
0.6	0.104	0.21	0.17	4.20	2.2	7.6	2.4
0.7	0.108	0.20	0.20	4.20	2.7	5.6	2.9
0.8	0.115	0.24	0.23	4.40	3.0	7.1	3.2
0.9	0.137	0.28	0.25	4.55	3.2	8.6	3.5
1.0	0.109	0.64	0.48	4.84	5.9	23	6.4
1.1	0.127	0.67	0.47	4.96	5.8	25	6.2
1.2	0.112	0.76	0.56	5.02	6.8	27	7.4
1.6	0.100	1.01	0.70	5.45	8.1	36	8.8
1.8	0.107	1.03	0.67	5.61	7.7	39	8.3
2.2	0.111	0.91	0.67	5.61	7.7	31	8.3
2.8	0.114	1.00	0.69	5.69	7.8	36	8.4
4.0	0.106	1.19	0.82	5.86	9.2	42	9.9

TABLE II. Device parameters extracted from fitting the magnetoresistance data on wire set $S2$ (anneal and passivation) to theory. The value of W_{eff} for $V_{\text{bg}}=+2$ V is the average of the previous six values of W_{eff} obtained from the fitting procedure.

V_{bg} (V)	W_{eff} (μm)	L_ϕ (μm)	L_e (μm)	n_s (10^{11} cm^{-2})	μ_e (10^4 cm^2/V s)	τ_ϕ (ps)	τ_e (ps)
0.2	0.108	0.17	0.13	4.15	1.7	6.6	1.8
0.4	0.115	0.23	0.19	4.22	2.5	8.2	2.7
0.6	0.105	0.32	0.24	4.41	3.2	12	3.4
0.8	0.087	0.52	0.38	4.49	4.9	19	5.3
1.0	0.082	0.67	0.54	4.68	6.7	23	7.3
1.2	0.087	0.69	0.62	4.85	7.6	20	8.2
2.0	0.097*		0.73	5.18	9.0		9.7

ary scattering, once again using W_{eff} and L_ϕ as adjustable parameters. The results of these fits for $S1$ and $S2$ are tabulated in Tables I and II, respectively.

In interpreting the results listed in Tables I and II, the significance of our assumption that the intervalley scattering factor $\alpha=0.5$ should be noted. Theory predicts a value of α ranging from 0.375 (strong intervalley scattering) to 1 (independent valleys).[13] Performing a three-parameter fit to our data, using α, W_{eff} and L_ϕ as adjustable parameters, is not feasible, due to the limited field range available. Previous studies on Si metal-oxide-semiconductor field effect transistors[14,15] and more recently $Si/Si_{1-x}Ge_x$ heterostructures,[8] have produced values of α in the range 0.27–0.36, indicating strong intervalley scattering. Since decreasing α leads to larger values of L_ϕ extracted from the fitting procedure, our choice of $\alpha=0.5$ can be considered to be a conservative estimate. We also mention that the values of n_s used for all the fits have been obtained from the high-field SdH characteristics, such as the one in Fig. 2(a). However, we have observed certain anomalies that make it difficult to determine the sheet concentration using the standard formula $n_s=4/\Delta(1/B)h$, where $\Delta(1/B)$ is the spacing of minima in the SdH characteristic when one plots resistance vs $1/B$. Such anomalies may be due to a lifting of the valley degeneracy due to the lateral confinement potential in the narrow wires. Instead we simply determine n_s from the magnetic field corresponding to the position of the $\nu=8$ minima: $n_s=8B_{n=8}/h$. Even if there is a certain degree of error in the determination of n_s, Eqs. (1) and (2) only depend upon n_s through the Fermi velocity $\nu_F=(\hbar/m^*)\sqrt{\pi n_s}$, and slight deviations in n_s do not greatly affect the calculation results for L_ϕ.

Tables I and II show an increasing phase-coherence length with increasing electron concentration, as expected. Both samples show a very similar quantitative dependence of L_ϕ on n_s, suggesting that the passivation and annealing steps do not greatly affect the electron transport. This also confirms that the etch process has induced very little damage to the devices. In both samples, L_ϕ is of the same order as L_e, and the ratio τ_ϕ/τ_e is sometimes less than 2.5. In addition, for large sheet concentrations, τ_ϕ/τ_e is seen to decrease with increasing n_s for $S2$, while, in $S1$, τ_ϕ/τ_e generally tends to continue increasing. These results may explain why the negative magnetoresistance is suppressed in some samples for large n_s. If $\tau_e\sim\tau_\phi$, then electrons will lose phase memory before they have a chance to be scattered, eliminating the weak-localization effect even at zero field. This is a reasonable assertion since phase-breaking mechanisms such as electron-electron scattering are known to be n_s dependent. Further investigations into the mechanisms by which the weak localization is suppressed are ongoing. The values of L_ϕ obtained in this study are encouraging for device applications, particularly given the relatively small lithographic dimensions of the wires used in this study. For instance, for a wire with a lithographic width of 0.20 μm, and an inner diameter of 0.15 μm, and Aharonov-Bohm ring with arm lengths of 0.55 μm could readily be fabricated. It should also be pointed out that L_ϕ in $S2$ may still become larger for $V_{\text{bg}}>2$ V; however, because no magnetoresistance effect is observable, the value of L_ϕ cannot be determined by weak-localization fitting. The conducting channel widths extracted from the fits agree quite well with the values obtained from the G vs W characteristics in Fig. 1. In fact, the subtle increase in the value of W_{eff} for $S1$ compared to $S2$ is in agreement with a slightly smaller dead-layer width for the samples with no post-processing treatments. Finally, we note that the μ_e vs n_s values obtained for both wires sets are consistent with those expected for the as-grown 2D material. These results show that our fabrication procedure does not degrade the electrical properties of the wires.

In conclusion, we have presented a study of the phase-coherent electron transport in strained $Si/Si_{0.7}Ge_{0.3}$ quantum wires fabricated by reactive ion etching. The dead-layer widths have been determined by extrapolation of the G vs W characteristics, and by fitting the low-field magnetoresistance data to theory. Very little damage is induced by the dry-etching process, and no significant difference is observed between wires with and without post-processing passivation and annealing treatments. The low-field magnetoresistance is found to fit best to the BvH theory of 1D weak localization in the clean limit, and the nature of the boundary scattering is found to be specular. The phase coherence length L_ϕ and the conducting channel width W_{eff} are extracted from the fits for various values of the back-gate bias voltage. The results show that the wires approach a regime where $\tau_\phi\sim\tau_e$ for large n_s, which could explain why the weak localization is often suppressed for large values of positive back-gate voltage. Further work is needed to understand this mechanism in more detail. These studies are important for understanding electron transport in low-dimensional systems, and will help in the design and analysis of devices based upon quantum interference effects.

The authors would like to acknowledge J. Nocera for assistance with the low-temperature measurements.

[1] F. Schäffler, D. Többen, H.-J. Herzog, G. Abstreiter, and B. Holländer, Semicond. Sci. Technol. **7**, 260 (1992).
[2] Y. H. Xie, E. A. Fitzgerald, D. Monroe, P. J. Silverman, and G. P. Watson, J. Appl. Phys. **73**, 8364 (1993).
[3] K. Ismail, M. Arafa, K. L. Saenger, J. O. Chu, and B. S. Meyerson, Appl. Phys. Lett. **66**, 1077 (1995).
[4] J. F. Nützel, C. M. Engelhardt, R. Wiesner, D. Többen, M. Holzmann, and G. Abstreiter, J. Cryst. Growth **150**, 1011 (1995).
[5] C. W. J. Beenakker and H. van Houten, in *Solid State Physics*, edited by H. Ehrenreich and D. Turnbull (Academic, San Diego, 1991), pp. 38–51.
[6] G. Bergmann, Phys. Rep. **107**, 1 (1984).
[7] G. Stöger, G. Brunthaler, G. Bauer, K. Ismail, B. S. Meyerson, J. Lutz, and F. Kuchar, Semicond. Sci. Technol. **9**, 765 (1994).
[8] R. S. Prasad, T. J. Thornton, A. Matsumura, J. M. Fernandez, and D. Williams, Semicond. Sci. Technol. **10**, 1084 (1995).
[9] R. Cheung, T. Zijlstra, E. van der Drift, L. J. Geerligs, A. H. Verbruggen, K. Werner, and S. Radelaar, J. Vac. Sci. Technol. B **11**, 2224 (1993).
[10] K. Ismail, M. Arafa, F. Stern, J. O. Chu, and B. S. Meyerson, Appl. Phys. Lett. **66**, 842 (1995).
[11] B. L. Al'tshuler and A. G. Aronov, Pis'ma Zh. Eksp. Teor. Fiz. **33**, 515 (1981) [JETP Lett. **33**, 499 (1981)].
[12] C. W. J. Beenakker and H. van Houten, Phys. Rev. B **38**, 3232 (1988).
[13] H. Fukuyama, in *Electron-Electron Interaction in Disordered Systems*, edited by A. L. Efros and M. Pollak (North-Holland, Amsterdam, 1985), pp. 155–230.
[14] N. Paquin, M. Pepper, A. Gundlach, and A. Ruthven, Phys. Rev. B **38**, 1593 (1988).
[15] R. T. Syme and M. Pepper, J. Phys. Condens. Matter **1**, 2747 (1989).