Extending the high-frequency limit of a single-electron transistor by on-chip impedance transformation

J. Pettersson, P. Wahlgren, P. Delsing, D. B. Haviland, and T. Claeson
Department of Physics, Chalmers University of Technology and Göteborg University, S-412 96 Göteborg, Sweden

N. Rorsman and H. Zirath
Department of Microwave Technology, Chalmers University of Technology, S-412 96 Göteborg, Sweden

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We have fabricated an aluminum single-electron transistor (SET) and characterized it at frequencies up to 700 kHz. The relatively high frequency was achieved by reducing the capacitance at the SET output. The SET was bonded to an InP high-electron-mobility transistor (HEMT), and biased through a small (<100 μm) on-chip resistor made of 150 tunnel junctions in series. The output-voltage swing of the SET decreases with increasing HEMT current because of heating. Thus, the gain of the HEMT was limited and therefore the noise performance of the system was limited to $3\times10^{-4}e/\sqrt{\mathrm{Hz}}$ at 10 kHz. [S0163-1829(96)00120-8]

A single-electron transistor[1,2] (SET) is a device that is based on the Coulomb blockade.[3,4] It consists of a small metallic island that is connected through two very small tunnel junctions to the source and drain terminals and capacitively coupled to a gate terminal. The SET can measure very small changes of charge on the gate capacitance. Sensitivities as high as $7\times10^{-5}e/\sqrt{\mathrm{Hz}}$ have been reported[5] at 10 Hz. SET transistors have been successfully used to study single-electron tunneling events at low frequency.[6] A drawback of the SET is its low operation frequency, which is set by the *RC* time constant of the output resistance of the SET, and the capacitance loading the SET output. The output resistance of a SET must necessarily be higher than the quantum resistance $R_K\approx26$ kΩ and is typically of order 100 kΩ. The electrical lead that brings the signal up to room temperature loads the SET output with a capacitance to ground of order 300 pF. This results in an *RC* cutoff frequency of order 5 kHz.

In this paper we report results with a circuit where both a high impedance bias resistor and an active output impedance transformer are integrated on chip to reduce the load capacitance. The bias resistor is fabricated using a large number of tunnel junctions, each having a tunnel resistance $\sim R_K/2$. The impedance transformation of the SET output signal is achieved by connecting a high-electron-mobility transistor (HEMT) close to the SET output; see Fig. 1. This configuration reduces the load capacitance C_{L1} by a factor of 1000 and results in a device which can operate at frequencies up to 700 kHz. The cutoff frequency is then set by the *RC* time constant at the output of the HEMT circuit. A similar experiment, which used a HEMT but no on-chip resistor, was recently performed in Delft.[7] A theoretical upper limit for the speed of the SET itself is given by the tunneling rate in the SET which is roughly $1/RC$, where R and C are the resistance and the capacitance, respectively, of the tunnel junctions in the SET. The theoretical limit is of the order of 10 GHz for our SET.

The coupled SET-HEMT device can be used for looking at real-time single-electron tunneling events at high frequencies, such as single-electron tunneling oscillations from a current biased tunnel junction. It can, for instance, be used in a current standard where the tunneling events are *monitored* on the single-electron level rather than *controlled,* as is the case in the turnstile[8] and pump[9] concepts.

The sample was measured in a dilution refrigerator at temperatures between 15 and 50 mK. A magnetic field of 0.25 T was applied to quench superconductivity in the aluminum films. The bias currents and output signal were fed between the SET-HEMT hybrid and room temperature via 0.5-m Thermocoax filters[10] at 50 mK (25-Ω series resistance and 220-pF capacitance to ground), and 1.5 m of thin copper wires. Each lead passed through a 100-pF feedthrough ca-

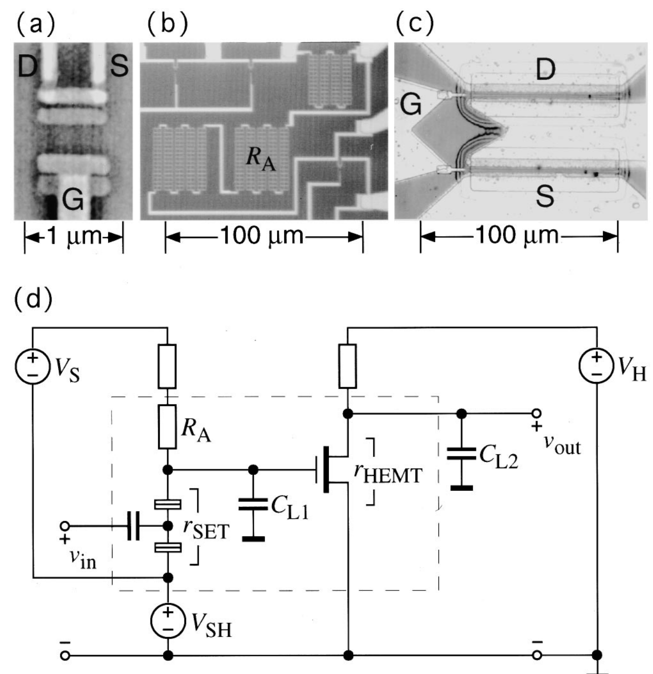

FIG. 1. (a) SEM and (b) and (c) optical images of the SET transistor, the integrated resistor, and the HEMT, respectively. (d) Circuit diagram. The cold part is within the dashed box.

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pacitor at room temperature. To avoid cross talk, the input signal was fed to the SET gate via a 2-m stainless-steel coaxial cable and a 0.5-m Thermocoax filter.

The SET tunnel junctions [Fig. 1(a)] were made of aluminum on an unoxidized silicon substrate, using an angle evaporation technique.[11,12] Each of the two junctions had an area of approximately 80×80 nm^2, which gives a capacitance of order 300 aF. The resistance per junction was 50 kΩ. The SET showed typical periodic response as a function of gate voltage[6] with 175-μV maximum voltage swing. The gate voltage period was $\Delta V_g = 9.4$ mV corresponding to a gate capacitance $C_g = e/\Delta V_g = 16$ aF. The on-chip drain resistor R_A for the SET [Fig. 1(b)] was made of 150 larger junctions in series, each having a resistance close to the quantum resistance. The junctions were sufficiently large so that the charging energy $e^2/2C$ was not much larger than $k_B T$. Therefore, there was practically no Coulomb blockade in the array and its current voltage characteristic was almost linear even at very low temperatures.[13] The total resistance of the array was 2 MΩ. This array resistor cuts off the stray capacitance of the SET biasing lead. We have used an array of 150 junctions rather than a single or double junction, since a single or a double junction would give one or two additional island(s) whose charge would be affected by the gate potential. In that case, the output signal would be a function not only of the SET but also of a gate-voltage-dependent ''resistor.'' Furthermore, the array makes the transistor more current biased than voltage biased, which should increase the voltage swing of the SET.

The HEMT was made on an InP substrate with a modulation-doped lattice-matched $Al_xIn_{1-x}As/Ga_xIn_{1-x}As$ heterostructure. The double gate design [Fig. 1(c)] was originally optimized for a wide-bandwidth low-noise amplifier in millimeter-wave applications.[14] As such it has a small input capacitance (50–300 fF) and acceptable dc characteristics with low noise at low power. It has gate length 0.15 μm, gate width 2×75 μm, and the distance from the gate to the two-dimensional electron gas (2DEG) was thinned down to 30 nm through selective wet etching. The leakage resistance through the gate was 2 MΩ at room temperature but exceeded 50 GΩ at low temperature. In this measurement, we used one of the two sources as a drain. This choice increased the voltage gain, but at the same time decreased the cutoff frequency, each by a factor of 4 as compared with using the center drain. With this series connection, the minimum drain-source resistance was 80 Ω. The HEMT chip was glued onto the silicon substrate with epoxy. A 2-mm-long and 25-μm-thick gold bonding wire connected the drain of the SET and the gate of the HEMT.

There were three parameters to optimize during operation of the circuit: the SET current, the HEMT current, and the gate-source potential of the HEMT. Referring to Fig. 1(d), the SET was biased from a battery V_S, through a 10-MΩ bias resistor at room temperature and the 2-MΩ on-chip resistor R_A. The HEMT was biased through 10 kΩ at room temperature and a 150-Ω unintentional contact resistance on the chip. The HEMT bias voltage, V_H, and the offset voltage between the sources of the SET and the HEMT, V_{SH}, were supplied by low-pass-filtered power-line-operated voltage sources. V_{SH} together with V_H define the HEMT working point and the small signal impedance r_{HEMT}. Typically $V_{SH} = -0.3$ V and $r_{HEMT} \approx 200$ Ω. The source of the HEMT was chosen as the ground point.

The total capacitance loading the SET output ($C_{L1} \sim 0.23$ pF) was the sum of several contributions. The dominating contributions were the self-capacitance of the bonding pad on the SET chip, ~100 fF, the bonding wire, ~30 fF, and the capacitance between the gate and the two-dimensional electron gas (2DEG), ~100 fF. Thus the cutoff frequency of the first stage of the circuit was approximately $(2\pi r_{SET} C_{L1})^{-1} \sim 5$ MHz, where r_{SET} (~150 kΩ) is the differential resistance at the bias point.

The capacitance loading the HEMT output is $C_{L2} \approx 1.5$ nF, coming from the bias and output leads plus an unused coaxial lead. The cutoff frequency in the second stage is then approximately $(2\pi r_{HEMT} C_{L2})^{-1}$, which for $r_{HEMT} = 200$ Ω gives 0.5 MHz.

When the SET is used as an electrometer, the dc gate voltage level is adjusted such that the average charge on the island is an integer plus or minus $\frac{1}{4}e$, where the SET has maximum sensitivity. In Fig. 2(a), a 10-kHz triangular wave with a 9.4-mV peak-to-peak amplitude was added to show the gate-voltage dependence and frequency doubling as one electron charge is added and subtracted in each period. In Fig. 2(b), a 0.2e step response is plotted for three different V_{SH} settings. Here the leads at the HEMT output were loaded by two additional 1.5-nF filters which increased the settling time (i.e., decreased the RC cutoff frequency). The signal level of the lowest trace of Fig. 2(b), was lower than the rms noise level, and the wave form was only distinguishable after averaging a large number of traces.

At temperatures below 50 mK, the maximum output voltage swing in the SET transistor is 175 μV. However, when the HEMT was biased with a current corresponding to a

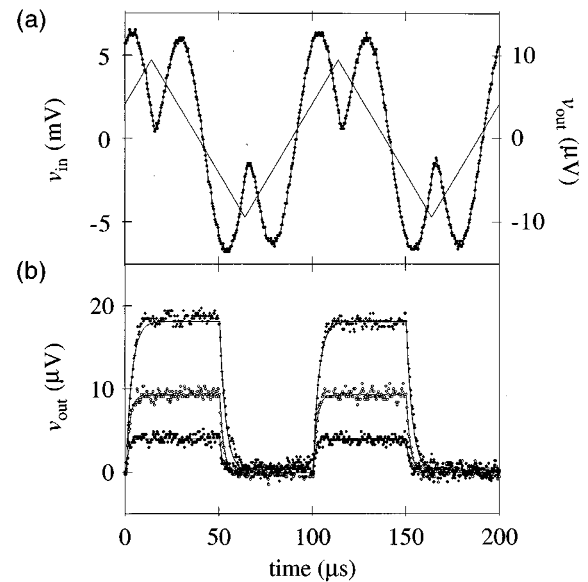

FIG. 2. Electrometer signal at 10 kHz. $B = 0.25$ T, $T < 50$ mK, $C_{L2} \approx 4$ nF. (a) Triangle wave response with an amplitude 9.4 mV$_{pp}$ corresponding to one electron peak to peak: $I_{SET} = -1$ nA; $I_{HEMT} = 100$ μA; $r_{HEMT} \approx 400$ Ω. (b) Step response corresponding to 0.2e: $I_{SET} = -2$ nA; $I_{HEMT} = 100$ μA; $r_{HEMT} \approx 140$, 180, 400 Ω (bottom to top). The full lines represent fits to exponential decays. Noise reduction was performed by averaging approximately 500 traces for each curve.

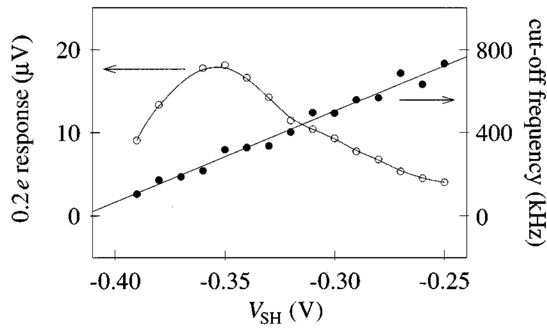

FIG. 3. The 0.2 electron step response and the cutoff frequency as a function of V_{SH}. The step response was calculated in the same way as in Fig. 2(b).

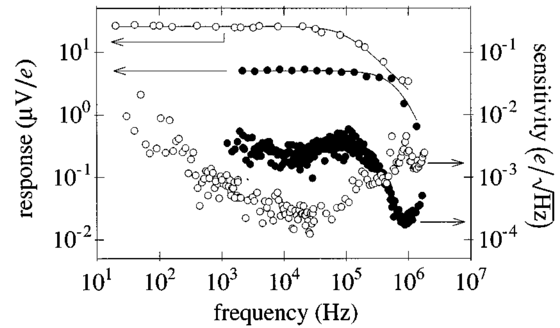

FIG. 4. Frequency response and noise of the SET-HEMT circuit at two working points. $B=0.25$ T; $T<50$ mK; $C_{L2}\approx 1.5$ nF. Parameters for open circles: $I_{SET}=-0.2$ nA, $I_{HEMT}=20$ μA, $r_{HEMT}\approx 1$ kΩ; filled circles: $I_{SET}=-1$ nA, $I_{HEMT}=-300$ μA, $r_{HEMT}\approx 130$ Ω.

power of 10 μW, the output voltage swing of the SET decreased by more than a factor of 2, corresponding to an electron temperature of the SET above 200 mK. We can therefore only bias the HEMT with a very small drain current, which limits its voltage gain. There is an obvious tradeoff between signal amplitude and cutoff frequency as can be seen in Fig. 3. The cutoff frequency decreases with decreasing V_{SH} due to the increasing r_{HEMT}. On the other hand, the output amplitude has a maximum around $V_{SH}\approx -0.35$ V. For lower V_{SH}, the power dissipation in the HEMT heats the SET and thus decreases the amplitude (left side in Fig. 3). For higher V_{SH} the gain in the HEMT decreases due to a lower sensitivity of the HEMT.

The output signal amplitude and charge noise are plotted versus frequency in Fig. 4 for two different HEMT working points. To be certain that we only measured the SET output signal and not cross talk, these amplitudes were obtained by sweeping the gate voltage corresponding to the addition of $n=2-20$ electrons to the gate capacitance, at different sweep frequencies. The HEMT output signal was captured by a digitizing oscilloscope and then the nth frequency component was Fourier analyzed to find the amplitude. The noise was determined by Fourier analysis of traces with no input signal.

The charge sensitivity in the measurements presented is not outstanding due to low gain and fluctuations in the offset voltage, V_{SH}. The 0.3-V offset voltage had to be stable on the μV level. This problem can be avoided using a HEMT designed for high gain at zero gate voltage, or by replacing the external voltage source V_{SH} with an appropriate resistor. The gain can be improved significantly if the gate capacitance of the SET is increased, and if the tunnel junctions in the SET transistor are made smaller so that the HEMT can be operated at a higher power. The capacitive load at the HEMT output can be reduced by cryogenic amplification close to the HEMT. For frequencies above 5 MHz, it will be necessary to further reduce the capacitive load also at the SET output. This may be achieved by patterning the SET and its bias resistor directly on the HEMT substrate.[7]

In conclusion, we have succeeded in constructing and characterizing a single-electron transistor with an InP high-electron-mobility transistor as an active impedance transformer within millimeters from the SET. The total load capacitance at the SET output was reduced from 1 nF to less than 1 pF by incorporating the HEMT and an on-chip biasing resistor for the SET. A cutoff frequency of 700 kHz was obtained, and the minimum input noise was $3\times 10^{-4}e/\sqrt{\text{Hz}}$ at 10 kHz. The limiting factor was no longer the load on the SET output, but rather the capacitive load on the HEMT output, and heating of the SET by power dissipated in the HEMT.

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