Electron interference in a T-shaped quantum transistor based on Schottky-gate technology

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We have observed quantum interference in the electronic transport in a T-shaped $Al_{0.3}Ga_{0.7}As/GaAs$ heterostructure. The geometry is defined by four independent Schottky gates on top of the layer system. By changing the split-gate voltages, the dimensions of the T-shaped two-dimensional electron gas could be varied continuously. Especially, the stub length of the transistor can be controlled in order to switch between constructive and destructive interference. An additional advantage of using gates instead of etching methods to define the geometry is the smooth form of the boundary potential which implies specular boundary scattering. At low temperatures the transport in the high mobility two-dimensional electron gas (2DEG) is ballistic. Thus weak-localization effects and conductance fluctuations are suppressed, whereas the intended interference pattern is reproducible and nearly identical for different samples. We attribute the observed resistance oscillations to the change in transmissivity in the device when the geometry is altered. Other explanations are discussed as well but could be excluded by experiment.

I. INTRODUCTION

In 1989, inspired by advances in nanometer-scale technology, Sols *et al.*[1,2] have proposed a transistor principle based on electron interference in a T-shaped $Al_xGa_{1-x}As/GaAs$ heterostructure. Independently Datta[3] has suggested an analogous device only differing from the aforementioned by the position of the gate that controls the interference pattern. The realization of both devices seemed to be possible using material systems where the electron preserves its phase coherence over distances larger than the sample size. In that case, electron interference can significantly change the classical sample resistance and can be used as basis for new devices. Besides, the performance of an interference device strongly depends on the number of eigenmodes propagating in it. Idealized only one mode should be present to prevent averaging effects. This is true for both, either if an electrical field is used to control the interference pattern (e.g., Ref. 4) or the change of sample geometry is responsible for the variation in the resistance, as in our case. Both requirements, large phase coherence length and electron wavelength comparable to sample size, can be fulfilled using an electron waveguide in a two-dimensional electron gas (2DEG).

The principle of operation of a T-interference device acting as a transistor is explained in Fig. 1(a). The T-transistor switches between high transmissivity and low transmissivity between source (emitter e) and drain (collector c) by change of sample geometry via a gate (g). In a simple model, the interference pattern only depends on the length difference between the two paths (a) and (b) indicated in Fig. 1(a).

Variation of the stub depth S changes the path difference between (a) and (b), which is $2S$ by $2\Delta S$. Thus, the same interference pattern should appear each time the stub length is changed by ΔS equal to half the electron wavelength (in the direction of the electron propagation). The result of varying the stub length continuously is a periodic alternating signal as long as all electrons in the channel have the same velocity. Measuring the sample resistance or voltage drop between source and drain should yield $R=h/2e^2$ for the constructive case, if transmissivity is one and zero conductance for destructive interference assuming infinite phase coherence length L_Φ, only one one-dimensional mode in the channel and adiabatic transport conditions.[5]

First, experiments on electron waveguides with T geometry were reported by Miller *et al.*[6] Using a two-dimensional electron gas in an $Al_xGa_{1-x}As/GaAs$ heterostructure, they have prepared T geometries by wet chemical etching. Thus,

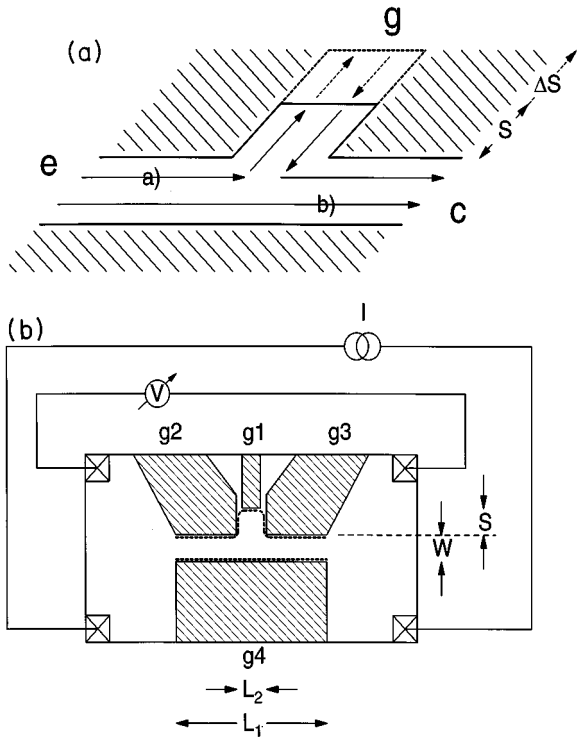

FIG. 1. (a) Schematic picture for the appearance of electron interference in a T geometry. S denotes the stub length and ΔS the change of S with the gate voltage. (b) Measurement configuration and relevant length scales.

the geometry of the sample is fixed excluding the stub length, which can be controlled by a Schottky gate. They found some hints for the presence of the expected interference pattern, but in addition they always observe universal conductance fluctuations. Due to the fact that their T structure was etched, a variation of geometrical dimensions using the same sample was not possible.

Besides, the transport in their case was not ballistic over the entire distance between emitter and collector. Remember the fact that $L_{\mathrm{el}}=6\ \mu$m determined from nonlocal transport measurements is not the true distance L_{bal} between impurities, which dominate the transport properties for low temperatures in $\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{As/GaAs}$ heterostructures. Typically, L_{bal} and L_{el} differ by a factor of 4 or 5.[7] Using μ and n_s from the Hall effect and Shubnikov–de Haas measurements in order to determine L_{el} implies a weighted averaging over the scattering angle, thus, L_{bal} is always significantly smaller than L_{el}.

As will be shown in the following sections, our device is indeed smaller than L_{bal} and geometrical dimensions can be controlled continuously using the same sample. The advantages of combining ballistic transport properties with controllable interference have already been demonstrated by Yacoby *et al.*[8] They have observed a clear periodic interference signal in a point contact experiment. In contrast to our experiment, they did not change the geometry of the device, but have varied the electron concentration over a well defined distance.

II. DEVICE FABRICATION

A modulation doped $\mathrm{Al}_{0.3}\mathrm{Ga}_{0.7}\mathrm{As/GaAs}$ heterostructure, with a sheet carrier concentration of $n_s\approx 2.1\times 10^{15}\ \mathrm{m}^{-2}$ and a mobility of $\mu\approx 110\ \mathrm{m}^2/\mathrm{V\,s}$ at 4.2 K, was used in the present investigation. Both values have been determined without illumination using a Hall bar geometry. The heterostructure was grown by molecular beam epitaxy and consists of a GaAs buffer followed by a 40 nm thick $\mathrm{Al}_{0.3}\mathrm{Ga}_{0.7}\mathrm{As}$ spacer layer, a δ doping of $N_D=4\times 10^{12}\ \mathrm{cm}^{-2}$, and a 100 nm thick $\mathrm{Al}_{0.3}\mathrm{Ga}_{0.7}\mathrm{As}$ layer, which is finally capped with a 10 nm thick GaAs top layer.

From ballistic measurements with a number of adjacent point contacts performed by Müller,[7] we deduced a value of $L_{\mathrm{bal}}\approx 1.7\ \mu$m for our heterostructure. In comparison, the wire length of our T structure is approximately 1 μm and thus ballistic transport over the entire distance from emitter e to collector c is possible. Transport phenomena like weak localization or conductance fluctuations, which depend on the existence of impurities in the conducting channel, do not contribute to the sample resistance and the intended interference pattern is not masked by them.

Figure 2 shows a scanning electron micrograph of the T transistor. Brighter areas are metal gates on top of the semiconductor. These are fabricated using electron beam lithography and consist of a 5 nm chromium and a 40 nm gold layer.

Applying a sufficiently negative voltage to all four gates [$g1$, $g2$, $g3$, and $g4$ in Fig. 1(b)] depletes the electron gas below the metallization and defines the electrically active area of the device. The limits of this area are plotted as dotted lines in Fig. 1(b). The applied voltages have to be small enough in order to prevent any electron transport between $g1$ and $g2$ or $g1$ and $g3$. After the definition of the T-transistor geometry, the interference conditions (which means the length S) can be changed by applying a variable negative voltage to gate one [$g1$ in Fig. 1(b)]. This is the small fingerlike structure on the right side of the photograph.

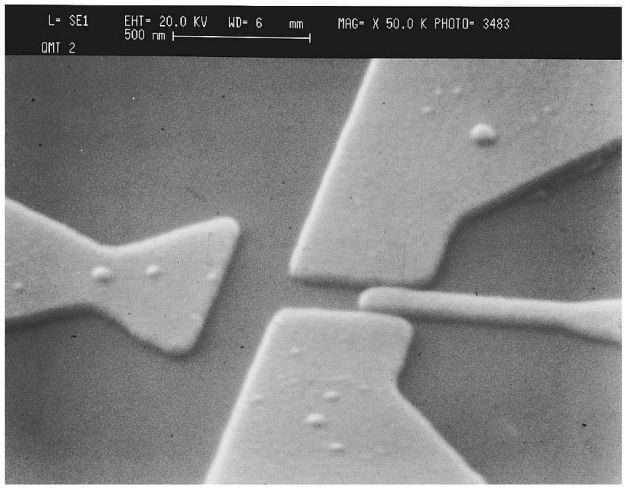

FIG. 2. Scanning electron micrograph of the T transistor.

Comparing Fig. 1(b) with Fig. 2, we obtain $L_1=1\ \mu$m, $L_2=250$ nm, $W=250$ nm, and $S=280$ nm for threshold voltages V_{th} just totally depleting the electron gas underneath the metal gates. For a separation of 150 nm between gates and 2DEG as in our case, we assume nearly ideal transcription of gate geometry to the electron gas for $V=V_{\mathrm{th}}$. These are the maximum values of the T dimensions. Lowering (making more negative) the voltages V_{g2}, V_{g3}, and V_{g4} reduces the wire widths by a field effect and changes the carrier concentration in the conducting channel. For a wire width of 250 nm and a carrier concentration as given above, there are nine eigenmodes in the T transistor if we assume a hard wall square potential. Applying a more negative voltage at V_{g4} in Fig. 1(b) reduces the number of modes in the wire by reducing W as is well known from split-gate point contacts.[9] On the other hand, lowering the voltages at V_{g2} or V_{g3} has a twofold effect. Both values, L_2 and W are reduced simultaneously, whereas we assume the stub length S to stay nearly unchanged.

III. RESULTS AND DISCUSSION

In our experiment, $g2$, $g3$, and $g4$ were typically kept at fixed voltages and $g1$ was changed continuously measuring the voltage drop across the sample for a small ac current, as indicated in Fig. 1(b). All samples were measured in a four-terminal configuration, using standard lock-in techniques. In order to reach temperatures down to 0.3 K, we used a ^{3}He-evaporation cryostat.

In Fig. 3(a), the sample resistance (R_{xx}) versus gate voltage (V_{g1}) is plotted at $T=0.3$ K for a current of 10 nA. The voltages at $g2$, $g3$, and $g4$ were -0.42 V. This is the value for which the T geometry is just defined by depleting the electron gas underneath $g2$, $g3$, and $g4$.

For $V_{g1}>-0.5$ V, the resistance of the wire is nearly

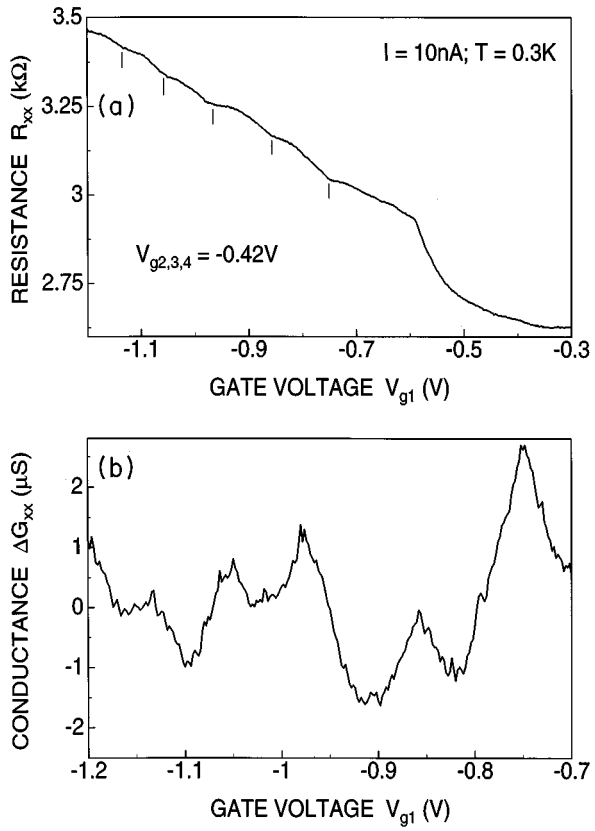

FIG. 3. (a) Sample resistance R_{xx} as a function of applied voltage to gate one $(g1)$. (b) Change of conductance ΔG_{xx} as function of V_{g1}. The linear background resistance has been subtracted.

unchanged and defined by the three gates mentioned before. Decreasing the voltage at gate one $(g1)$ below -0.5 V changes the sample resistance drastically by depleting the electron gas below $g1$ totally. Further reduction of V_{g1} yields a monotonous nearly linear increase of R_{xx}, with superimposed oscillations having minima in resistance marked in Fig. 3(a).

The background resistance can be understood as classical resistance of electrons, which do not contribute to the interference pattern, because their phase memory has been lost by inelastic scattering events. A reduction of S with decreasing V_{g1} increases the sample resistance by a classical reduction of the inner wire area.

In contrast to this, we attribute the oscillations superimposed on this background to controlled electron interference in our T geometry. For a quantitative analysis, it is necessary to translate the gate voltage into the length S. This can be done by the following assumptions: First, $S(V_{g1}=-0.59\ \mathrm{V}) = 280$ nm, which is the aforementioned maximum value of S. Second, $S(V_{g1}=-1.6\ \mathrm{V}) = 0$ nm. For this gate voltage, which is not plotted in Fig. 3(a), a significant increase of sample resistance is observed. We attribute this effect to the increased probability of electron reflection between e and c when the potential of $g1$ reaches the wire. Third, there is a linear decrease of S with decreasing gate voltage. After having subtracted a linear background resistance, we calculate under the assumptions above an oscillation period of 22 nm $<\lambda/2<$ 38 nm, using Fourier analysis. Figure 3(b) shows the interference related change in conductance ΔG_{xx}, without the background influence.

The electron wavelength in the direction of the stub is the only relevant parameter for the oscillation period of the resistance pattern, if we assume in a simple picture that the phase difference is produced in the stub of the T structure. As mentioned before, L_2 is 250 nm for $V_{g2,3,4}=-0.42$ V. For a hard wall square potential and a Fermi energy of $E_F \approx 7.5$ meV, there are nine eigenmodes in the wire. For the lowest seven modes, we calculate 55 nm $<\lambda<$ 85 nm. Whereas the wavelength of the eighth and ninth one-dimensional channel are 115 nm and 315 nm, respectively.

We interpret our measurement as a superposition of a number of different eigenmodes with very similar quantization energies. Averaging effects do not fully destroy the interference pattern in that case, although there is a damping effect. This can easily be verified by numerical superposition of sinusoidal modes with appropriate frequencies and identical amplitudes. In this picture, each sinus corresponds to the interference pattern of one eigenmode. Note that the choice of frequencies and amplitudes is not crucial for the statement above. Even under the assumption of a harmonic confinement potential, the situation is not significantly altered although the damping effect is more pronounced. In addition, the finite phase coherence length, in combination with the nonideal shape of the potential forming the T geometry, reduces the theoretically expected variation of resistance. For the latter reason, electrons in the modes with higher energies contribute even less, due to their small velocity in direction of the stub. The reduced velocity for the higher energy modes implies a reduced phase coherence length L_Φ and thus less contribution to interference pattern. Besides, for the largest wavelength, the measurement interval is too small to resolve any interference related resistance oscillations.

Nevertheless, the following questions arise: How can we be sure that our measurement is not related to the change of number of one-dimensional channels in the T structure and thus nothing else but a stepwise increase of resistance as in a point contact? Are we measuring conductance fluctuations although we assume our sample to work in the ballistic regime? There are a number of facts in contradiction to these explanations of our measurements.

If we divide our device in three point contact segments formed by the gates $g2/g4$, $g1/g4$, and $g3/g4$ [see Fig. 1(b)], variation of V_{g1} in the first order approximation only changes the resistance in the middle area of the T transistor. For Ohmic transport, we expect the measured device resistance to be approximately the sum of the resistances of the individual quantum point contacts (QPC), whereas for adiabatic transport conditions, R_{xx} is completely determined by the QPC with the lowest conductance (Kouwenhoven *et al.*[5]). Thus, for adiabatic transport, a change of V_{g1} should not yield any increase of R_{xx}, as long as the resistance of the point contact $(g1/g4)$ is smaller than the resistance of both, the emitter point contact $(g2/g4)$ and the collector point contact $(g3/g4)$. On the other hand, under Ohmic transport conditions, all resistance features of Fig. 3(a) should also be found for $V_{g4}=-0.42$ V and $V_{g2,3}=0$ V (dashed line) in Fig. 4. As can be seen easily from Fig. 4, both are not the case for our experiment. (Even for more negative values of V_{g1}, no conductance quantization could be observed for the

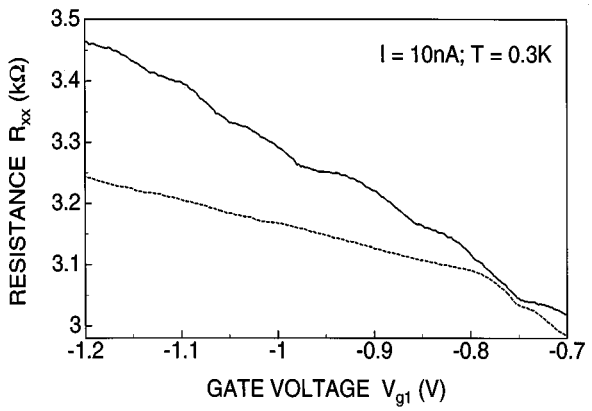

FIG. 4. Comparison of the influence of gate one ($g1$) on sample resistance for $V_{g2,3,4}=-0.42$ V (solid line), with $V_{g4}=-0.42$ V and $V_{g2,3}=0$ V (dashed line). The second curve is vertically offset by a value of 1.9 kΩ to higher resistance values.

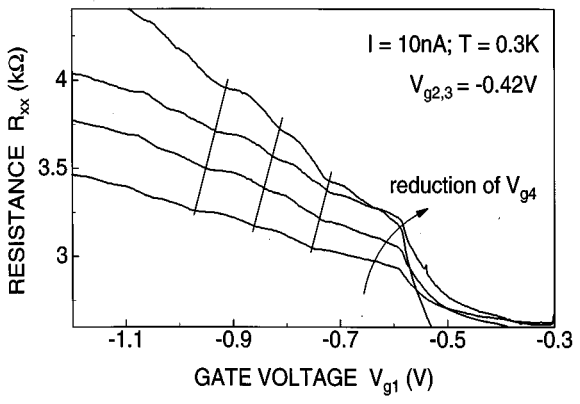

FIG. 6. Sample resistance for various values of V_{g4}, as a function of V_{g1}. From top to the bottom, we applied $V_{g4}=-0.6$ V, -0.52 V, -0.48 V, and -0.42 V. The curves are offset by -2 kΩ, -0.9 kΩ, and -0.6 kΩ to lower resistance values (from top to bottom).

dashed curve. The relatively large separation between gate one and gate four is responsible for the absence of pure one-dimensional modes in the transport area.)

Besides, the resistance steps in Fig. 3(a) or Fig. 4 (if we want to interpret the resistance modulation in that way) are not related to $h/2Ne^2$ (N is the number of one-dimensional channels in a point contact[9]), even after subtraction of a constant resistance contribution by $g2/g4$ and $g3/g4$. Especially the step height does not increase with decreasing gate voltage as it should for a stepwise depopulation of one-dimensional channels in a point contact geometry.

Another important feature in contradiction to the interpretation of the resistance modulation as conductance fluctuations is the reproducibility. Annealing of the sample up to room temperature and cooling back to $T=0.3$ K did not change the measurement as would be the case for conductance fluctuations.

To support our interpretation of intended electron interference, we have performed temperature dependent measurements (Fig. 5) and have investigated the influence of gate voltage V_{g4} on sample resistance (Fig. 6). All those measurements are in qualitative agreement with the expected behavior as will be discussed below.

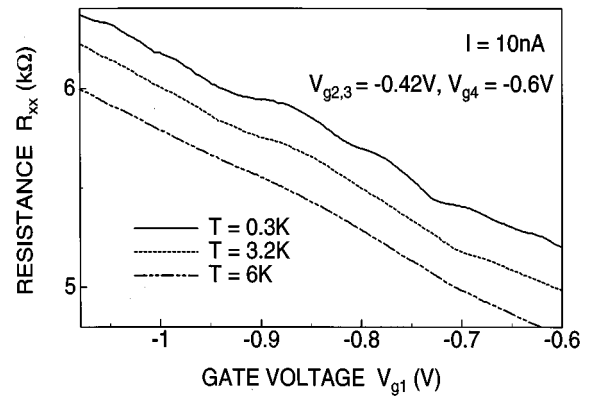

FIG. 5. Temperature dependence of R_{xx} for $T=0.3$ K, $T=3.2$ K, and $T=6$ K. No offset is present in the figure.

Increasing the temperature very quickly destroys the electron phase and thus the modulation of resistance. A temperature of $T=6$ K is already sufficient to fully suppress the interference pattern.

The phase coherence length in $Al_xGa_{1-x}As/GaAs$ for the temperature range that we have investigated is mainly determined by electron-electron scattering.[10,11] For temperatures below $T=10$ K, phonons do not play a significant role. The decrease of L_Φ with increasing temperature is due to enlarged phase space available for electron-electron scattering events for higher temperatures.[12,13] Thus, the number of electrons contributing to the interference pattern is decreased with increasing T and only the background resistance is observed. (For higher temperatures, R_{xx} decreases due to reduction of quantum mechanical corrections as electron-electron interaction in quasi-one-dimensional geometries, e.g., Ref. 14.)

Still more convincing than the temperature dependence of the oscillation amplitude is the influence of gate four ($g4$) on sample resistance. Reduction of V_{g4} yields a smaller W, whereas L_2 stays nearly unchanged. This implies that on one hand the absolute value of R_{xx} increases with decreasing V_{g4} and the slope of the background resistance is increased, but on the other hand, the oscillation period remains nearly unchanged. Remember that the phase difference between paths (a) and (b) in Fig. 1(a) as mentioned earlier only depends on the wavelength λ in the direction of gate one ($g1$). Indeed, all aforementioned aspects can be observed in Fig. 6. For clarity the curves are vertically offset. Minima in the resistance pattern are connected by lines as a guide to the eye. Again, the step height of none of the curves is related to $h/2Ne^2$.

We still have to discuss one feature, which is obvious in the measurement. The resistance minima are shifted towards higher values of V_{g1} for decreasing V_{g4}. We have observed that smaller values of V_{g4} do not only reduce W, but also increase the value of V_{g1} for which S becomes zero. This means that there is an influence of gate four ($g4$) on S, which shifts the interference pattern and slightly changes the oscillation period in the measurement. Besides, the interfer-

ence pattern always becomes less pronounced for smaller gate voltages.

We attribute all these effects to a reduced sheet carrier concentration n_s in the T geometry for $V_g < V_{\mathrm{th}}$. This implies on one hand that L_Φ is reduced for smaller gate voltages and on the other that the assumption of ideal transcription of gate geometry to the electron gas is no longer valid. In that case, we can no longer consider the gates to work independently and the influence of gate four ($g4$) on S for small values of V_{g1} becomes pronounced.

This is the reason why we did not find a better resolved interference pattern for smaller values of $V_{g2,3,4}$, which one would expect for transport conditions with less modes in the T structure. The monotone shift of oscillations with a nearly constant period in V_{g1} again cannot be explained by means of conductance fluctuations.

IV. CONCLUSIONS

In our experiments, a reproducible interference pattern could be observed for different devices, thus proving the absence of the sample specific fingerprint. We clearly have identified the variation in resistance as an interference related effect by the controlled change of sample geometry. Using gates instead of etching methods made it possible to check the validity of our interpretation. Quantitative agreement between theory and experiment could be found under the assumption that mainly electrons in the lowest transport modes contribute to the interference pattern.

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