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Crossover from global to local rule for the Coulomb blockade in small tunnel junctions

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We have investigated several single and double aluminum tunnel junctions in the nonsuperconducting state. Current-voltage (I-V) characteristics were measured up to voltages corresponding to several hundred times e/C, where C is the capacitance of each junction. The individual junctions had capacitances in the order of 0.5 fF and resistances of 50–150 kΩ. The offset voltage, defined as $V_{\rm off}=V-I/(dI/dV)$, is resistance independent for given junction capacitances, but depends on the bias voltage. For a single junction the offset voltage is very small for low voltages, but it approaches the local-rule value of $e/2C$ at high voltages. For a double junction the global rule applies at low voltages and the offset voltage equals $V_{\rm off}=e/C_\Sigma$, where $C_\Sigma=2C+C_0$. At large voltages the local rule applies and each junction contributes with a voltage of $e/2C$ to the offset voltage, so that $V_{\rm off}=e/C$. This paper shows that a careful analysis of the offset voltage has to be made to determine the values of the capacitances involved.

Metal/oxide/metal tunnel junctions usually display a linear current-voltage (I-V) characteristic where the slope defines the tunnel resistance R_N. However, if the capacitance of the junction, C, is extremely small, the I-V characteristic becomes nonlinear due to the Coulomb blockade. The effect of the Coulomb blockade has been studied extensively during the past decade in junctions with capacitances of the order 1 fF.[1,2] The Coulomb blockade manifests itself in the I-V characteristics as an increase in the differential resistance at low bias, when these tunnel junctions are measured at temperatures below E_C/k_B. Here $E_C\equiv e^2/2C$ is the characteristic charging energy. The shape of the I-V characteristic depends strongly on the impedance $Z(\omega)$ of the electromagnetic environment of the junction, as has been shown both theoretically[3–8] and experimentally[9–12] for superconducting as well as for nonsuperconducting samples. For a circuit of junctions with a high impedance environment $Z(\omega)\gg R_Q\equiv h/4e^2$, the so-called local rule[13] should apply, i.e., only the changes of the charge in the circuit itself have to be considered. On the other hand, for a circuit with a low impedance environment $Z(\omega)\ll R_Q$, the so-called global rule applies and the change of the environment as well as the change in the circuit have to be considered. Ingold *et al.*[8] pointed out that there should be a crossover between the two limits as the voltage is increased. This crossover is the subject of this paper.

For a perfect voltage biased [$Z(\omega)=0$] double junction system in the normal state, the differential resistance is enhanced at low bias voltage, due to the Coulomb blockade. As the bias voltage is increased the differential resistance gradually decreases to $\sim R_N$, so that the I-V curve is shifted by an offset voltage $V_{\rm off}\approx e/C_\Sigma$, where C_Σ is the sum of the junction capacitances and the self-capacitance C_0 of the island formed between the junctions. The offset voltage is often used to determine the characteristic capacitances.[14] A common method to determine the offset voltage is to extrapolate the high voltage ($V\gg e/C$) asymptotes of the I-V curve for both negative and positive voltages and measure the voltage shift, which should be $2V_{\rm off}$. This method is, however, ambiguous, because $V_{\rm off}$ depends on the bias voltage from which the extrapolation is done.

For a more precise analysis, we extrapolate the tangent at each point of the I-V curve back to zero current [see Fig. 1(a)]. The function $V_{\rm off}(V)$ can thus be calculated from the I-V curve and its derivative,

$$V_{\rm off}(V)=V-\frac{I}{dI/dV}. \tag{1}$$

The offset voltage $V_{\rm off}(V)$ can be regarded as a measure of the effective Coulomb energy barrier for a single electron to tunnel through the circuit. From analysis of $V_{\rm off}$ we can extract important information not only about the junction but also about the characteristics of the environment.

For a single small capacitance tunnel junction in a low impedance environment, the low bias resistance is only slightly increased compared to R_N, and the offset voltage grows gradually as the bias voltage is increased. The I-V characteristic of a single ultrasmall tunnel junction coupled to a voltage source via an external impedance can be determined with the help of a probability density function $P(E)$.[7] $P(E)dE$ is the probability that the tunneling electron can exchange an energy E with the environment. In terms of $P(E)$, Eq. (1) can be written (at $T=0$)

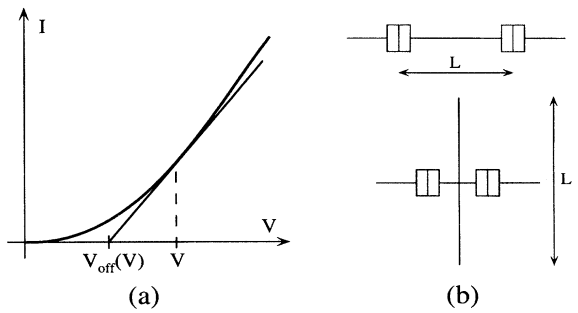

FIG. 1. (a) Definition of the offset voltage. (b) The two different geometries used to change the island capacitance.

$$eV_{\rm off}=\frac{\int_0^{eV} EP(E)dE}{\int_o^{eV} P(E)dE}. \quad (2)$$

The probability density $P(E)$ can be calculated numerically if the impedance of the environment is known. For a single junction connected between two transmission lines (the measurement leads) each with a real, frequency independent impedance $Z(\omega)=R_{\rm env}/2$, one can use the low energy asymptotic behavior of $P(E)$ to obtain the low voltage limit,[4,5]

$$I(V)=\text{const}\times V|V|^{1/2\alpha}, \quad (3)$$

where $\alpha\equiv R_Q/R_{\rm env}$. Combining this with Eq. (1) and normalizing all voltages to $e/2C$, we find

$$\nu_{\rm off}\equiv \frac{V_{\rm off}}{e/2C}=\frac{1}{2\alpha+1}\,\nu, \quad (4)$$

where $\nu\equiv V2C/e$. Thus we can determine $R_{\rm env}$ from the slope of $V_{\rm off}$ vs V at low bias. For large bias voltages the offset voltage should approach $e/2C$ as[15]

$$\nu_{\rm off}=1-\frac{8\alpha}{\pi^2\nu}. \quad (5)$$

For the double tunnel junction system one has to rely on approximate methods[8] and the analysis becomes more complex.

A more simple analysis of both single and double tunnel junctions in the low impedance case is to consider the length of the transmission line in the proximity with each junction over which an electromagnetic wave can travel during some characteristic time. This so-called horizon picture was introduced by Büttiker and Landauer,[16] who argued that the characteristic time should be the traversal time of tunneling. Nazarov[3] suggested that the relevant time should be the "uncertainty time" $\tau\approx\hbar/eV$, which was also supported by experiments.[9] From τ we get an event horizon (length)

$$l=\frac{c_0}{\sqrt{\epsilon_{\rm eff}}}\frac{\hbar}{eV}, \quad (6)$$

where c_0 is the speed of light in vacuum and $\epsilon_{\rm eff}$ is the effective dielectric constant. This event horizon defines a capacitance which is voltage dependent, $C_l(V)$. The capacitance of a strip of length l, width w, and distance to the ground plane h can be determined to be[17]

$$C=2\pi\epsilon_0\epsilon_{\rm eff}\frac{l}{\ln\left(\frac{8d}{w}\right)}, \quad d=\min(h,l). \quad (7)$$

For a single tunnel junction the effective capacitance seen by the tunneling electron is then $C_{\rm eff}=C+C_l/2$, giving an offset voltage $V_{\rm off}=e/2C_{\rm eff}$. Then $\nu_{\rm off}(\nu)$ can be written as

$$\nu_{\rm off}=\frac{1}{1+\frac{4\alpha}{\pi\nu}}. \quad (8)$$

This expression gives qualitatively the same shape for $V_{\rm off}(V)$ as the $P(E)$ theory, and has the same asymptotic form as Eqs. (4) and (5), but with slightly different prefactors.

Thin film Al/AlO_x/Al tunnel junctions were fabricated with a standard shadow evaporation technique.[18,19] The substrate (thickness $h=250\ \mu$m) was oxidized silicon, with an oxide layer grown in wet oxygen to a thickness of 1 μm. The pattern was defined with e-beam lithography in a two-layer copolymer, PMMA resist. The AlO_x barrier was grown *in situ* with dry oxygen. Single junctions were fabricated with various areas and resistances. The double junctions were defined with a shift perpendicular to the current path to avoid a third (much larger) tunnel junction in series. The self-capacitance of the island between the two junctions was altered in two different ways: either by increasing the length of the thin island between the two junctions, or by adding a strip of varying length perpendicular to the current path when the distance between the junctions was fixed at two micrometers [see Fig. 1(b)]. The former will be referred to as the straight geometry and the latter as the cross geometry. Four chips with several double tunnel junctions of different layouts were measured. Each junction has an approximate area of 80×80 nm^2. The resistances for the junctions varied from 50 to 150 kΩ. One chip had a strip width of the island of approximately 80 nm, while the others had a width of 300 nm.

Measurements were carried out in a dilution refrigerator at a temperature of about 20 mK. A large magnetic field (1 T) was applied to quench superconductivity. For large junctions and/or high temperatures we find the linear approximation[20] of the tunneling I-V to be valid up to approximately $V_{\rm lin}\sim20$ mV per junction. Above $V_{\rm lin}$, $V_{\rm off}$ can no longer be directly related to the charging energy. Due to the extrapolation method used, any nonlinearity in the I-V curve will show up in $V_{\rm off}$. This results in a sensitivity to mesoscopic conductance fluctuations with varying voltage.[21,22] These fluctuations in dI/dV, which we find to be reproducible and magnetic field dependent, result in large fluctuations of the offset voltage at high bias.

Typical offset voltages for single junctions are shown in Fig. 2 together with a fit of $V_{\rm off}$ from $P(E)$ calculations at zero temperature. $V_{\rm off}$ for a single junction of area approximately 180×80 nm^2 levels off to the local rule value of $e/2C=0.11$ mV, corresponding to a capacitance of 0.73 fF. In the low voltage limit (global rule) the impedance of the environment can be determined from the slope of $V_{\rm off}$ vs V, Eq. (4). From Fig. 2(a), we find $R_{\rm env}=300\ \Omega$ (150 Ω on each side of the junction). As can be seen in Fig. 2(b), the offset voltage for junctions of area approximately 80×80 nm^2 does not level off below $V_{\rm lin}\sim20$ mV, but fitting by adjusting the junction capacitance we find a good agreement with the $P(E)$ theory for $C=0.25$ fF. For both junctions sizes we get a capacitance per unit area in the range 40–45 fF/μm^2, in agreement with previous experience.[23]

Double tunnel junctions exhibit a very different $V_{\rm off}(V)$, as shown in Fig. 3, where data for three different island

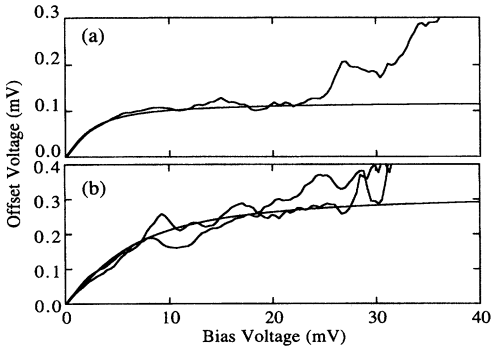

FIG. 2. Comparison of measurements and calculations of the offset voltage of single junctions. The measurements were done at $T=20$ mK and $B=1$ T. (a) The offset voltage for a large area junction, which levels off to $e/2C=0.11$ mV, compared to a $P(E)$ calculation with $R_{env}=300\ \Omega$. (b) The offset voltages for two smaller junctions. Using $R_{env}=300\ \Omega$, a good fit is obtained at $C=0.25$ fF.

capacitances C_0 are displayed. The curves can be characterized by four different regions: (i) At very low bias, $V\sim e/2C$, the offset grows rapidly as the bias voltage increases. (ii) Between ~ 3 and 20 mV, V_{off} grows almost linearly and there is a clear reduction of the offset voltage with increased island capacitance. (This is the only region where V_{off} depends on the geometry of the island, which will be discussed in a future paper.) (iii) Above ~ 20 mV (10 mV per junction) C_0 no longer plays a role. (iv) Above $V_{lin}\sim 40$ mV (20 mV per junction) nonlinearity, not associated with the Coulomb blockade, causes V_{off} to increase rapidly.

The voltage at which C_0 no longer plays a role (~ 10 mV per junction) corresponds to a length $l=9.4\ \mu$m, where $\epsilon_{eff}=4.4$ has been used in Eq. (6). Taking a capacitance per unit length of 30 aF/μm (see below) one obtains a capacitance of $C_l\sim 0.2$ fF. The individual junctions have capacitances of approximately $C\sim 0.35$ fF (see below); thus $C_l \lesssim C$ above 10 mV per junction, meaning that V_{off} is dominated by the individual junction capacitances. When the horizon becomes equal to the distance between the two junctions, the junctions effectively decouple from one another and the junctions act individually, each with an offset voltage determined by the junction capacitance and its local environment.

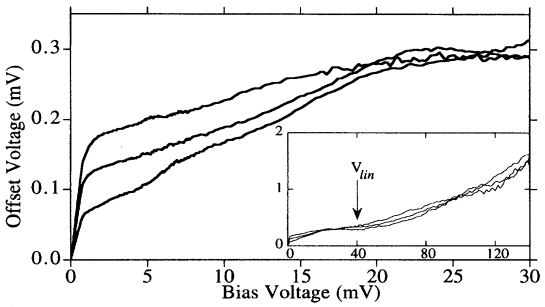

FIG. 3. The offset voltage for three samples from the same chip with island sizes 2 μm, 16 μm (straight geometry), and 64 μm (cross geometry) ($T=20$ mK and $B=1$ T). Larger island sizes gives a decrease in offset voltage at low bias. A linear extrapolation back to zero bias gives e/C_Σ. At high bias the offset voltages are similar in all three samples, independent of island size. The inset shows the same samples for bias up to 130 mV, far above V_{lin}, where the linear approximation breaks down.

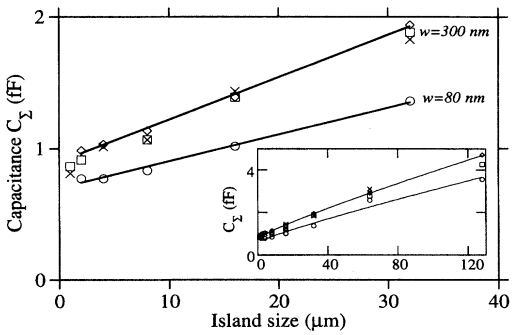

FIG. 4. C_Σ plotted vs island size for strip width 300 nm (three chips) and 80 nm (one chip). A linear fit for each strip width has a slope which gives the capacitance per unit length. The inset shows a fit to Eq. (7). The effective dielectric constant and junction capacitances can be determined.

All double junction systems have equal junction areas so that the differences in $V_{off}(V)$ can be attributed to the different C_0. In region (ii) V_{off} increases approximately linearly above 3 mV. We argue that by extrapolating V_{off} back to zero bias voltage, we achieve a voltage corresponding to the charging energy in the global rule, $V_{off}=e/C_\Sigma$. C_Σ as a function of island size is shown in Fig. 4. For small islands ($L<35\ \mu$m) a linear approximation ($C\propto L$) is very good and a capacitance per unit length is easily obtained. For the three chips with 300 nm linewidth the capacitance per unit length was $c_l=32$ aF/μm and for the chip with 80 nm linewidth $c_l=20$ aF/μm. Having determined both R_{env} and c_l we can also determine the inductance per unit length, $l_l=c_l R_{env}^2/4$, which gives values of the order 1 pH/μm.

For larger islands ($L>35\ \mu$m), the linear approximation for the island capacitance breaks down. The capacitance for a strip of length l and width w can be approximated with Eq. (7). We make a best fit with two free parameters: the capacitance of the junctions and the effective dielectric constant (see inset in Fig. 4). We find an ϵ_{eff} that varies from 4.0 to 4.8. An environment consisting of a semi-infinite silicon ($\epsilon_r=12$) substrate and vacuum ($\epsilon_r=1$) gives $\epsilon_{eff}\approx 6.5$. A substrate of silicon dioxide gives $\epsilon_{eff}\approx 2.5$. The fit gives a junction capacitance for the four samples between $C=0.30$ and 0.38 fF. This gives values (47–59 fF/μm^2) slightly larger than those of the single junctions with approximately the same size. This discrepancy can be attributed to inaccuracy in determination of the junction area. These capacitances corresponds to $e/2C$ between 0.21 and 0.26 mV, which indicates that in the local rule, V_{off} should approach ~ 0.46 mV. However, Fig. 3 shows that V_{off} is not fully developed at voltages below V_{lin}, which is consistent with the analysis of the single junctions of the same size [Fig. 2(b)].

In conclusion, we find that an analysis of the voltage dependence of V_{off} can give important information not only about the tunnel junctions but also about the electromagnetic

environment. The offset voltage is bias dependent as a result of a crossover from the global to the local rule. Single junctions, which have zero offset voltage in the global rule, develop a $V_{\rm off}$ that approaches $e/2C$ in the local rule. Our measurements agree well with numerical calculations from $P(E)$ theory. Double junctions shows a crossover from the global rule, where $V_{\rm off} \approx e/C_\Sigma$ ($C_\Sigma = 2C + C_0$), to the local rule, where each junction contributes with a voltage $e/2C$ to $V_{\rm off}$. Knowing the value of e/C_Σ for various geometries, we can estimate an effective dielectric constant of the environment, $\epsilon_{\rm eff}$, between 4.0 and 4.8, which is reasonable for our type of substrate. We can also obtain a capacitance per unit length of the microstrip which is between 20 aF/μm and 32 aF/μm, depending on strip widths, and an inductance the order of 1 pH/μm.

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