Energy distribution of interface states in the band gap of GaAs determined from x-ray photoelectron spectra under biases

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(Received 27 January 1995; revised manuscript received 23 March 1995)

The energy distribution of interface states in the GaAs band gap is determined for metal-oxide-semiconductor devices with an ultrathin thermal oxide layer of ~ 3.8 nm, from measurements of x-ray photoelectron spectra under biases. The energy distribution has a peaked structure with four peaks at ~ 0.15, ~ 0.5, ~ 0.75, and ~ 1.1 eV above the valence-band maximum (VBM). The 0.75-eV peak has the highest density of $\sim 1.9\times 10^{12}$ cm^{-2} and is attributed to a $(+/0)$ transition of As_{Ga} antisite defects. The weak 0.5-eV peak is tentatively attributed to a $(++/+)$ transition of the As_{Ga} antisite defects. The 0.15- and 1.1-eV peaks that have densities of 1.3×10^{12} and 0.8×10^{12} cm^{-2}, respectively, are attributed to Ga_{As} antisite defects and Ga vacancy defects, respectively. The interface Fermi level of GaAs is located at 0.85 eV above the VBM, indicating that it is strongly affected by the As_{Ga} antisite defects. From the density of the interface states near the Fermi level, i.e., $\sim 1\times 10^{13}$ cm^{-2}eV^{-1}, it is shown that $d\phi/d\chi_M$ (ϕ: barrier height in GaAs, χ_M: metal electronegativity) is 0.24, indicating that the Fermi level is pinned partly by the As_{Ga} antisite defects and that fixed oxide positive charges with a density of $(2-3)\times 10^{12}$ cm^{-2} are present at the GaAs/oxide interface.

I. INTRODUCTION

The formation of Schottky barriers for group III-V semiconductors has been studied extensively for cases of both thin and thick metal overlayers. For the former case, photoelectron spectroscopy (PES) is used while electrical techniques such as current-voltage and capacitance-voltage measurements are mainly employed for the latter case. To explain Fermi-level pinning, many models have been proposed so far, e.g., the unified defect model[1] (or advanced unified defect model[2]), the metal-induced gap-state model[3] (or virtual gap-state model[4]), the disorder-induced gap-state model,[5] the effective work-function model,[6] etc. The (advanced) unified defect model[1,2] predicts interface states with discrete energy levels, while the metal-induced gap-state model[3] and the disorder-induced gap-state model[5] predict a U-shaped energy distribution for the interface state density. The main reason why the mechanism of Schottky barrier formation has not been clarified yet is that the energy distribution of interface states in the semiconductor band gap cannot be obtained directly from conventional PES measurements because of the low densities of interface states and the overlap of high-density metal valence bands with them.

We have recently developed a method to determine the energy distribution of interface states in the semiconductor band gap.[7-9] The characteristic of this method is the measurement of PES spectra under biases in contrast to the conventional PES measurements under zero bias. Biases change the occupancy of interface states, leading to a shift of the semiconductor core level. In the present study, this method is applied to GaAs-based metal-oxide-semiconductor (MOS) devices with an extremely thin oxide layer of ~ 3.8 nm. It is found that the energy distribution of the interface states has a peaked structure.

II. EXPERIMENT

A Si-doped n-type GaAs(100) wafer with a donor density of 1.7×10^{17} cm^{-3} was used for the fabrication of the MOS devices. The wafer was cut into 5×5 mm^2 pieces, washed with boiled acetone and distilled water, and then immersed in a 0.5 wt % KOH solution to form a smooth surface.[10] Then, a thin oxide layer was formed by heating the wafer at 500 °C for 5 min in a wet oxygen atmosphere. In-Ga alloy was scrubbed at two points of the rear GaAs surface separated by ~ 5 mm, the resistance between these two points was checked to be less than 15Ω, and then the alloy was scrubbed on the whole rear surface to make Ohmic contact. The wafer was attached to a copper plate with silver paste. Then it was encapsulated with high-vacuum resin, leaving the front surface uncovered. A ~ 2.5-nm-thick platinum (Pt) layer was evaporated on the wafer surface by an electron-beam evaporation method for XPS measurements, while its thickness was increased to 15 nm for measurements of electrical characteristics. A copper wire was attached to the Pt layer on the high-vacuum resin with silver paste.

The MOS device thus produced was inserted into an XPS ultrahigh-vacuum chamber with the base pressure of 4×10^{-7} Pa. XPS spectra were recorded with a VG ESCALAB 220i-XL spectrometer. It was irradiated with monochromatic Al $K\alpha$ radiation from the Pt layer side at the incident angle of 45°. Photoelectrons were collected in the surface-normal direction. During the XPS measurements, the front Pt layer was grounded and the sample plate which was in electrical contact with the rear GaAs surface was connected to a potentiostat for applying biases. Hereafter, a voltage applied to the rear GaAs surface is defined as the external bias voltage.

Current-voltage (I-V) curves were measured with a potentiostat. For measurements of I-V curves under il-

0163-1829/95/52(8)/5781(8)/$06.00

lumination, a 62-mW cm^{-2} tungsten-halogen lamp was used as the light source. Capacitance-voltage curves were measured at the ac frequency of 10 kHz with a YHP 4192A impedance analyzer.

III. RESULTS

Figure 1 shows XPS spectra for the oxide-covered GaAs(100) surface with no Pt layer. In the As 3*d* spectrum [Fig. 1(a)], doublet peaks were observed at 41.20 and 41.90 eV, and attributed to As $3d_{5/2}$ and $3d_{3/2}$ levels, respectively, for the GaAs substrate. In the higher-energy region, two broader peaks were present at 46.2 and 44.6 eV, and attributed to As^{5+} and As^{3+} oxidation states, respectively.[11–13] The areal intensity of the 46.2-eV peak (or 44.6-eV peak) was 14.6% (or 9.1%) that of the substrate 3*d* peaks.

In the Ga 3*d* region [Fig. 1(b)], a main peak and a shoulder peak appeared at 20.60 and 19.30 eV, respectively. The former and latter peaks were attributed to a Ga oxide and the GaAs substrate, respectively. The areal intensity of the oxide peak was 5.3 times that of the substrate peak.

The valence-band spectrum [Fig. 1(c)] had very similar structure to that for β-Ga_2O_3.[11]

Figure 2 shows the amount of the energy shift of the substrate As $3d_{5/2}$ peak as a function of the bias voltage. The Pt $4f_{7/2}$ peak for the overlayer was taken as the energy reference (70.93 eV).[7–9] Upon applying a forward bias, the substrate peak shifted toward lower binding energy, while it shifted toward higher binding energy upon applying a reverse bias. For the same bias voltage, the binding energies were reversible within ±10 mV for the As $3d_{5/2}$ peak and ±5 mV for the Pt $4f_{7/2}$ peak. The amount of the shift was a complicated function of the bias voltage. There were several bias regions where the amount of the shift was very small. These regions correspond to the energy regions in which almost no interface states are present, as described in the next section.

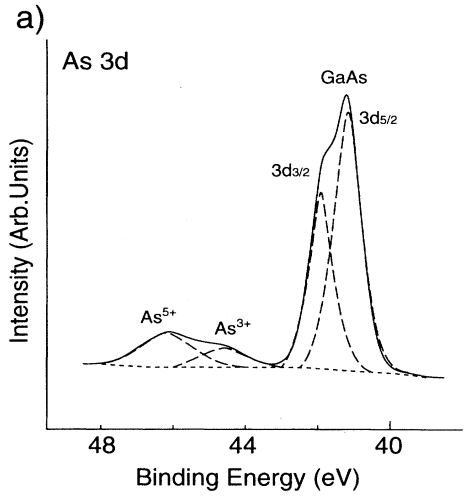
IV. DISCUSSION

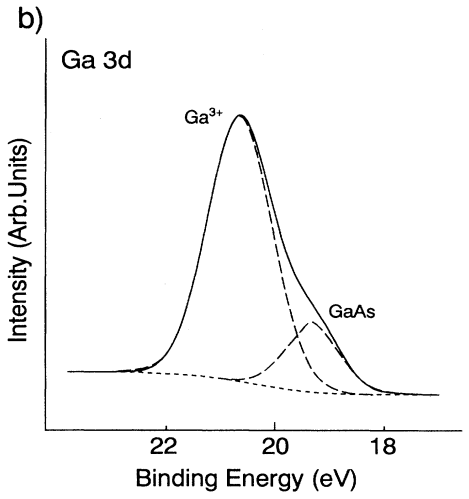
A. Energy distribution of interface states

First, the theoretical basis for the determination of the energy distribution of interface states from measurements of bias-induced energy shifts of the semiconductor core level is given briefly. At zero bias, interface states below the Fermi level are occupied by electrons, while those above it are empty. By applying a forward bias to *n*-type GaAs, the quasi-Fermi-level of GaAs is elevated. Consequently, interface states present between the equilibrium Fermi level E_F^0 and the quasi-Fermi-level E_F^f become newly occupied by electrons. This negative charge changes the potential drop across the oxide layer with the magnitude given by[7–9]

$$\Delta V_{IS} = e \int_{E_F^0}^{E_F^f} D_{IS}(E) dE / C_{ox} , \quad (1)$$

where D_{IS} is the density of the interface states as a function of the energy E with respect to the GaAs valence-





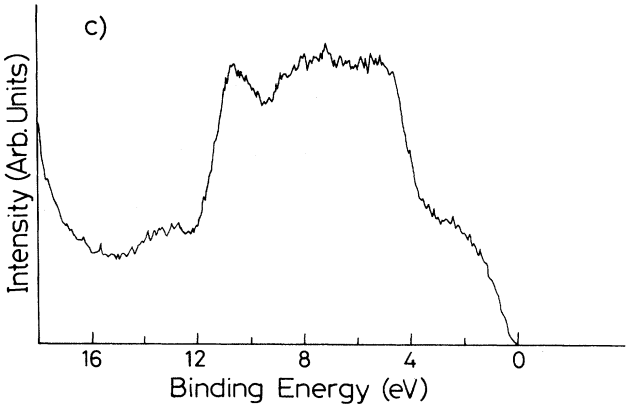


FIG. 1. XPS spectra for the oxide-converged GaAs(100) surface: (a) in the As 3*d* region; (b) in the Ga 3*d* region; (c) in the valence-band region.

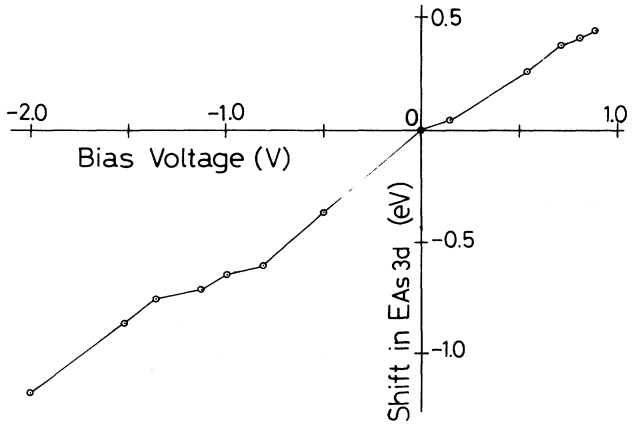


FIG. 2. Amounts of the bias-induced energy shift of the substrate As $3d$ peak vs the effective bias voltage.

band maximum (VBM), C_{ox} is the capacitance of the oxide layer, and e is the elementary electric charge. In Eq. (1), Fermi functions which cause a broadening of the occupancy of the interface states with the magnitude of $\sim kT$ are neglected. A change in the potential drop across the oxide layer is also caused by a change in the amount of the depletion-layer positive charge due to ionized donors. Using the abrupt-junction approximation, this amount, ΔV_D, is given by

$$\Delta V_D=(2eN_D\varepsilon_S)^{1/2}(\sqrt{V_b^0}-\sqrt{V_b})/C_{ox} , \tag{2}$$

where N_D is the donor density, ε_S is the permittivity of GaAs, and V_b^0 and V_b are the built-in potential at zero bias and that under forward bias, respectively. V_b^0 and V_b are written as

$$V_b^0=(1/e)(E_G-E_F^0-\Delta) ,$$
$$V_b=(1/e)(E_G-E_F^f-\Delta) , \tag{3}$$

where E_G is the band-gap energy, Δ is the energy difference between the Fermi level of the GaAs bulk and the bulk conduction-band minimum (CBM), and E_F^0 (or E_F^f) represents the energy difference between the Fermi level (or quasi-Fermi-level) and the valence-band maximum at the GaAs/oxide interface. In Eq. (2), deep impurities are neglected because the impurity density ($\sim 1\times 10^{16}$ cm^{-3} according to the manufacturer) is within the fluctuation level of the donor density from sample to sample. Using Eqs. (1)–(3), the total bias-induced change in the potential drop across the oxide layer, ΔV_{ox}, is written as

$$\Delta V_{ox}=\Delta V_{IS}+\Delta V_D$$
$$=\left[e\int_{E_F^0}^{E_F^f} D_{IS}(E)dE+(2eN_D\varepsilon_S/e)^{1/2}\{(E_G-E_F^0-\Delta)^{1/2}-(E_G-E_F^f-\Delta)^{1/2}\}\right]/C_{ox} . \tag{4}$$

On the other hand, E_F^f is given by

$$E_F^f=E_F^0+e|V|-e|\Delta V_{ox}| , \tag{5}$$

where V is the effective bias voltage.[7] The core level of the GaAs substrate is shifted by the same amount of $e\Delta V_{ox}$, because the energy difference between the GaAs band edge and the oxide band edge is constant. Therefore, by measuring the amount of the energy shift of the GaAs As $3d_{5/2}$ peak as a function of the bias voltage V, as shown in Fig. 2, the energy distribution of interface states in the GaAs band gap can be determined using Eqs. (4) and (5). ΔV_D for the reverse bias of -2.0 V, for example, is estimated to be 0.197 V, much smaller than ΔV_{ox} of 1.18 V (cf. Fig. 2), indicating that most of the shift is caused by the interface states.

In Eq. (4), the quasi-Fermi-level of the interface states is assumed to coincide with that of the GaAs bulk. This assumption is valid because the oxide layer is sufficiently thick, i.e., thicker than 2 nm, for the interface states to equilibrate with the GaAs bulk.[14,15] The bulk Fermi level is estimated to be located at ~ 0.03 eV below the conduction-band minimum,[16] i.e., very close to the CBM. Therefore the energy distribution of interface states in almost all the energy region in the band gap can be determined using Eqs. (4) and (5), i.e., the depletion approximation.

Figure 3 shows the energy distribution of the interface

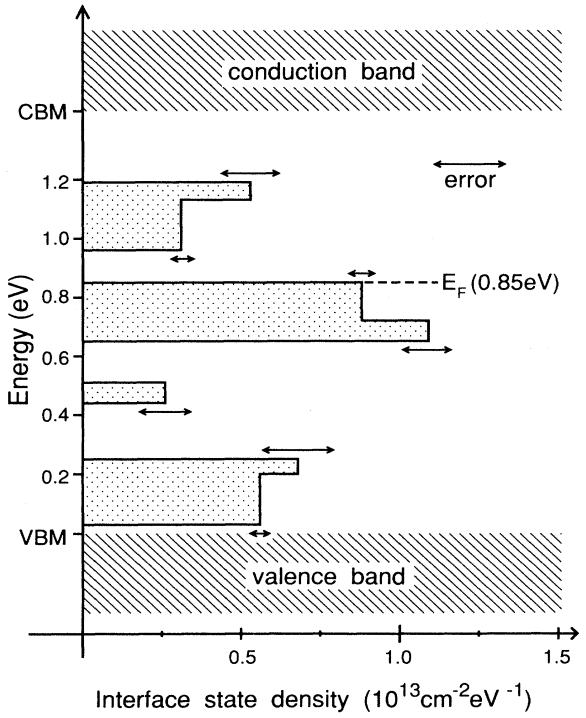


FIG. 3. Energy distribution of interface states for the ⟨2.5-nm-thick Pt/3.8-nm-thick oxide/GaAs(100)⟩ device.

states for the ⟨Pt/oxide/n-type GaAs(100)⟩ device, which is obtained from the analysis of Fig. 2. In the figure, the error bars which are estimated from the error in the energy difference between the substrate As $3d_{5/2}$ peak and the Pt $4f_{7/2}$ peak are included. The oxide capacitance is determined to be 5.5×10^{-7} F cm^{-2} from C-V measurements. The interface Fermi level is determined to be 0.85 eV above the VBM, as described in detail in the next subsection. Spicer and co-workers[1,2,17] show that the Fermi level of a cleaved n-type GaAs(110) surface is pinned at 0.75 eV by oxygen adsorption; this is the same pinning energy as those caused by the deposition of metals. Based on this result, they proposed advanced unified defect model.[2] Therefore it is likely that the interface states observed in the present study are induced by oxygen and the same kinds of interface states are induced by the deposition of metals.

It should be noted that in Fig. 3 there are several energy regions where the density of the interface states is almost zero. This energy distribution is calculated on the basis of the assumptions that the Fermi level at the interface coincides with that of the GaAs bulk and that the interface states below it are fully occupied while those above it are completely unoccupied. The validity of these assumptions is made by the presence of the bias regions where the shift of the substrate As $3d$ peak is caused only by ΔV_D. If these assumptions were not valid, i.e., the Fermi level at the interface were located between the GaAs quasi-Fermi-level and the metal Fermi level and/or interface states with occupancy widely deviating from zero or 1 were present in a wide energy region, the shift would be caused also by the interface states even when the bias voltage is changed within the region of no interface states, because the occupancy of the interface states would always change.

The energy distribution of the interface states has a peaked structure, i.e., four peaks at ~0.15, ~0.5, ~0.75, and ~1.1 eV above the VBM. Such an energy distribution with discrete energy levels is predicted from the advanced unified defect model.[2] This model shows that the surface Fermi level of the small amount of metal-deposited or oxygen-adsorbed GaAs is pinned at the energy level of As_{Ga} antisite defects, i.e., As atoms in the Ga lattice sites. Allen and Dow[18] also strongly support the Fermi-level pinning by As_{Ga}, based on theoretical calculations. Vacancies are less probable because they are thermodynamically less stable than antisite defects.[19] Allen and Dow[18] have also claimed that the vacancies cannot explain the different Fermi-level positions for n-type (~0.75 eV above the VBM) and p-type (~0.5 eV above the VBM) GaAs.[1,10,20] This argument is based on the fact that one electron is present in the uppermost energy level of the neutral vacancy, and hence the vacancy can both donate and accept an electron, leading to Fermi-level pinning of n-type and p-type GaAs at the same energy.

The energy distribution of the interface states with discrete energy levels seems to support the advanced unified defect model[2] because metals are likely to induce the same kinds of interface states as those observed in the present study, as described before. To clarify the mechanism of formation of interface states, a study of the energy distribution of metal-induced interface states is in progress in our laboratory, using the ⟨Pt/oxide/small amount of metal-deposited GaAs⟩ structure.

In bulk GaAs, dominant electron traps called $EL2$ are observed at ~0.7 eV above the VBM, using electron paramagnetic resonance[21–23] (EPR) and electron-nuclear double resonance (ENDOR).[24] In spite of extensive studies, there still remains a controversy as to the microscopic structure of $EL2$, i.e., as to whether they are isolated As_{Ga} defects,[25,26] arsenic interstitials As_i,[27] or As_{Ga}-As_i pairs.[23,24,28] The energy of the interface states at ~0.75 eV above the VBM observed in the present study with the highest intensity is in good agreement with that of the $EL2$ electron trap, supporting the advanced unified defect model.[2] If $EL2$ is attributed to As_{Ga}, the defect acts as a double donor because an As atom possesses two more valence electrons than a Ga atom.

The interface states at ~0.5 eV above the VBM may be due to the $(+/++)$ transition of As_{Ga}, which was observed at ~0.52 eV by EPR.[21,22] However, the density of the interface states at ~0.5 eV is much lower than that at ~0.75 eV. This may indicate that the 0.5-eV interface states have a different origin from that of the 0.75-eV interface states, i.e., another defect, such as vacancies. A more detailed study is needed to clarify the origin of the 0.5-eV interface states.

The As_{Ga} defects in bulk GaAs have a density of the order of 10^{16} cm^{-3}.[21,22,29] If 0.75-eV interface states with a density of $\sim2\times10^{12}$ cm^{-2} are formed by the transfer of the As_{Ga} defects to the interface, it follows that the defects present in the region up to 10–100 μm from the interface should move to the interface. Therefore it seems more likely that the As_{Ga} defects are formed at the interface through reactions of GaAs with oxygen or by a strain energy arising from lattice mismatch.

The energy of the 0.75-eV interface states shows reasonable agreement with that of electron traps at 0.82 eV below the CBM, i.e., 0.61 eV above the VBM, observed by deep-level transient spectroscopy.[29] This energy of 0.75-eV is also in good agreement with the theoretically calculated energy level of ~0.7 eV above the VBM for the As_{Ga} antisite defect at the surface.[18,30] These studies including the present work show that the energy of the As_{Ga} interface states is close to that of As_{Ga} in the bulk.

For bulk GaAs, a double acceptor is the dominant defect when the crystal is grown from a Ga-rich melt by the liquid-encapsulated Czochralski method, and the $(-/--)$ and $(0/-)$ transitions of this defect are observed at 0.20 and 0.08 eV above the VBM.[31–34] This acceptor-type defect has been investigated extensively using many kinds of experimental techniques such as photoluminescence,[35] infrared absorption spectroscopy,[36] deep-level transient spectroscopy,[37] Hall effect,[38] etc. Among several candidates for the defect, i.e., a Ga_{As} antisite defect,[39,40] a B_{As} antisite defect,[38] a complex of B_{As} and intrinsic point defects,[41,42] the Ga_{As} antisite defect is the most probable because the defect is observed for GaAs formed by molecular-beam epitaxy in which no boron is present.[43] Thus the interface states at ~0.15 eV

(Fig. 3) are attributed most probably to the Ga_{As} antisite defect.

The interface states at ~ 1.1 eV above the VBM with a density of 8×10^{11} cm^{-2} (Fig. 3) are probably due to Ga vacancies which act as electron donors. The Fermi levels of the small amount of metal-deposited n-type and p-type GaAs will be pinned at the highest acceptor level and the lowest donor level, respectively. Among much work on the Fermi-level pinning of GaAs, it has never been reported that the surface Fermi level is pinned at ~ 1.1 eV above the VBM. This indicates that the 1.1-eV interface states have a nominal effect on the Fermi-level pinning, and thus they are attributed to Ga vacancies, not to As vacancies which act as electron acceptors. According to theoretical calculations by Allen and Dow,[30] the donor level (or acceptor level) due to Ga (or As) vacancies is located above (or below) that of Ga_{As} (or As_{Ga}) antisite defects, supporting the above attribution.

Chiang and Spicer[44] have shown, by As deposition and desorption experiments for GaAs, that excess As on the surface is responsible for Fermi-level pinning because it leads to the formation of As_{Ga} antisite defects. Segregation of As on the GaAs(110) surface is also observed immediately after cleavage.[45] On the other hand, Chambers[46] has claimed that no excess As is present at the GaAs(001) surface. Similar XPS measurements under biases for MOS devices in which As is deposited between the GaAs substrate and the oxide layer will help to clarify the origin of the interface states.

B. Fermi level of the MOS device

The interface Fermi level E_F^0 is obtained from the intercept of the I-V curve measured in the dark and that under illumination. Photogenerated holes flow from GaAs to the Pt layer through the thin oxide layer, probably by tunneling when the GaAs bands bend upward, while photogenerated electrons flow in the same direction when they bend downward. Therefore the intercept, i.e., the potential at which no photocurrent flows, corresponds to the flat band condition. The built-in potential is determined to be 0.55 V from the intercept. Therefore the interface Fermi level E_F^0 is estimated to be 0.85 eV above the VBM taking into account that the bulk Fermi level is located at 0.03 eV below the conduction-band minimum.[16]

Here, the Fermi-level pinning for a small amount of metal-deposited GaAs and that for MOS devices are compared. In the former case where the amount of the deposited metal is so small that no metallic bands are formed, the countercharge for the interface state charge Q_{IS} is the depletion-layer charge of ionized donors, Q_D, in GaAs [cf. Fig. 4(c)]. In Figs. 4(a) and 4(b), the band diagrams before and after contact are illustrated, respectively. After contact, the interface Fermi level $E_{F,i}$ deviates from the interface neutral level $E_{F,n}$, because of electron transfer from n-type GaAs to the interface states, and this magnitude is depicted as ΔE_F in Fig. 4(b).

Using the abrupt-junction approximation, Q_D is simply given by

$$Q_D=(2eN_D\varepsilon_S V_b)^{1/2} . \tag{6}$$

The built-in potential V_b in Eq. (6) is written as

$$\begin{aligned} V_b&=(1/e)(E_G-E_{F,i}-\Delta)\\ &=(1/e)(E_G-E_{F,n}-\Delta E_F-\Delta) . \end{aligned} \tag{7}$$

On the other hand, Q_{IS} is given by

$$Q_{IS}=-e\int_{E_{F,n}}^{E_{F,i}} D_{IS}(E)dE . \tag{8}$$

Q_{IS} is negative (or positive) in sign when $E_{F,i}$ is above (or below) $E_{F,n}$, independent of the type of the interface states, i.e., donor type or acceptor type. (The type of the interface states affects $E_{F,n}$.) In cases where D_{IS} is nearly constant near $E_{F,i}$, Eq. (8) is simplified to

$$Q_{IS}=-e\Delta E_F D_{IS}(E=E_{F,i}) . \tag{9}$$

From Eqs. (6), (7), and (9), we have

$$\Delta E_F=[2N_D\varepsilon_S(E_G-E_{F,n}-\Delta E_F-\Delta)]^{1/2}/eD_{IS} . \tag{10}$$

Using the values for the present device in Eq. (10), i.e., $N_D=1.7\times10^{17}$ cm^{-3} and $D_{IS}=1\times10^{13}$ cm^{-2}eV^{-1}, and assuming that $E_{F,n}$ is located at the $EL2$ level, ΔE_F is estimated to be ~ 0.1 eV. In practice, Spicer *et al.*[17] observed that the surface Fermi level of cleaved n-type GaAs(110) shifts from 1.4 to 0.8 eV above the VBM with oxygen exposure. We suggest that this shift is caused by

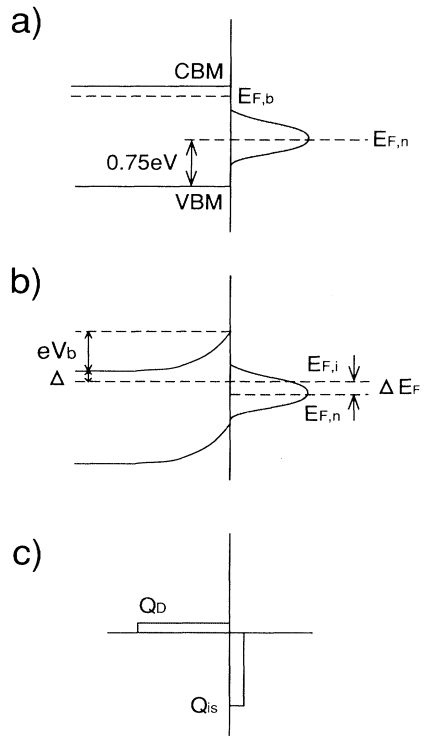


FIG. 4. Band diagrams for a small amount of metal-deposited GaAs surface: (a) before contact between the semiconductor bulk and the interface, (b) after contact, and (c) charge distribution after contact.

an increase in the density of the As_{Ga} interface states.

It is seen from Eq. (10) that ΔE_F depends on N_D. Therefore measurements of the interface Fermi level as a function of the donor (or acceptor) density will give information on the interface neutral level and the interface state density.

For oxide-covered semiconductors without a metal overlayer, the interface state charge is balanced by the depletion-layer positive charge Q_D and the fixed oxide charge $Q_{\rm fix}$. On the other hand, for MOS devices, the countercharges for the interface state charge $Q_{\rm IS}$, that for the depletion-layer charge Q_D, and that for the fixed oxide charge $Q_{\rm fix}$ are induced at the metal/oxide interface because of the large dielectric constant of a metal layer [cf. Fig. 5(c)]:

$$Q_M=-(Q_{\rm IS}+Q_D+Q_{\rm fix}) , \tag{11}$$

where Q_M denotes the charge at the metal/oxide interface. We assume that $Q_{\rm IS}$ and $Q_{\rm fix}$ are present at the GaAs/oxide interface. In Figs. 5(a) and 5(b), the band diagrams before and after contact are depicted, respectively.

Due to charge transfer between the interface states and the metal, that between the interface states and GaAs, and the presence of the fixed oxide charge, the Fermi level at the interface, E_F^0, deviates from the neutral level $E_{F,n}$. To make the interface Fermi level coincide with the metal Fermi level, a potential drop $V_{\rm ox}$ occurs across the oxide layer, whose magnitude is given by

$$V_{\rm ox}=(1/e)(E_F^0-E_{F,m}) , \tag{12}$$

where $E_{F,m}$ is the metal Fermi level before contact with respect to the VBM [cf. Fig. 5(a)]. Therefore Q_M is written as

$$Q_M=-V_{\rm ox}C_{\rm ox} . \tag{13}$$

For MOS devices, Q_D and $Q_{\rm IS}$ are also given by Eqs. (6) and (8), respectively. Taking into account that the depletion-layer charge is positive in sign and the interface state charge is negative in sign when E_F^0 is located above $E_{F,n}$, and using Eqs. (6), (8), (12), and (13) in Eq. (11), we have

$$-e\int_{E_F^0}^{E_{F,n}} D_{\rm IS}(E)dE+(2eN_D\varepsilon_S V_b^0)^{1/2}+eN_{\rm fix} =(1/e)(E_F^0-E_{F,m})C_{\rm ox} , \tag{14}$$

where $N_{\rm fix}$ is the density of the fixed oxide charge.

The neutral level for the MOS device is likely to be located at 0.75 eV above the VBM as for a small amount of metal-depositied n-type GaAs. $E_{F,m}$ for Pt is located probably near the VBM (5.5 eV below the vacuum level[16]), i.e., $E_F^0-E_{F,m}=0.85\pm0.1$ eV (Ref. 47) [cf. Figs. 5(a) and 5(b)]. Using the experimentally determined values of $D_{\rm IS}$, V_b^0, and $C_{\rm ox}$ in Eq. (14), it is seen that $N_{\rm fix}$ has a positive sign, i.e., fixed oxide positive charge, and that its density is $(2-3)\times10^{12}$ cm^{-2}.

$dE_F^0/dE_{F,m}$ for the present device is estimated to be 0.24 from Eq. (14), indicating that the Fermi level is partly pinned by the As_{Ga} interface states. ($dE_F^0/dE_{F,m}$ is usually expressed as $d\phi/d\chi_M$ where ϕ is the barrier height and χ_M is the electronegativity of the metal.) In the above discussion, interface states at the Pt/oxide interface are neglected. For such interface states, the countercharge is located close to the interface state charge, and thus the amount of the potential drop between these charges is likely to be much smaller than the potential drop across the oxide layer, $V_{\rm ox}$. Therefore the interface states at the Pt/oxide interface have a nominal effect on the above estimated value of $dE_F^0/dE_{F,m}$.

Zur *et al.*[48] suggested that a defective layer with a thickness of ~0.5 nm and a dielectric constant the same as that of bulk GaAs is present at the GaAs/metal interface. The above argument also holds for thick metal-deposited Schottky devices considering that the defective layer at the interface can be regarded as an insulating layer. Adopting the above values in estimating the capacitance of the defective layer, i.e., 2.3×10^{-5} F cm^{-2}, and assuming that $D_{\rm IS}$ near the Fermi level is 1×10^{13} cm^{-2} eV^{-1}, the same as that for the present MOS device, $dE_F^0/dE_{F,m}$ for thick metal-deposited Schottky devices is estimated to be almost unity, in disagreement with the results of Fermi-level pinning.[49,50] Therefore it can be concluded that the density of the interface states for the MOS device is much lower than that for Schottky devices. If $dE_F^0/dE_{F,m}$ for Schottky devices is assumed to be 0.1, for example, the density of the interface states is

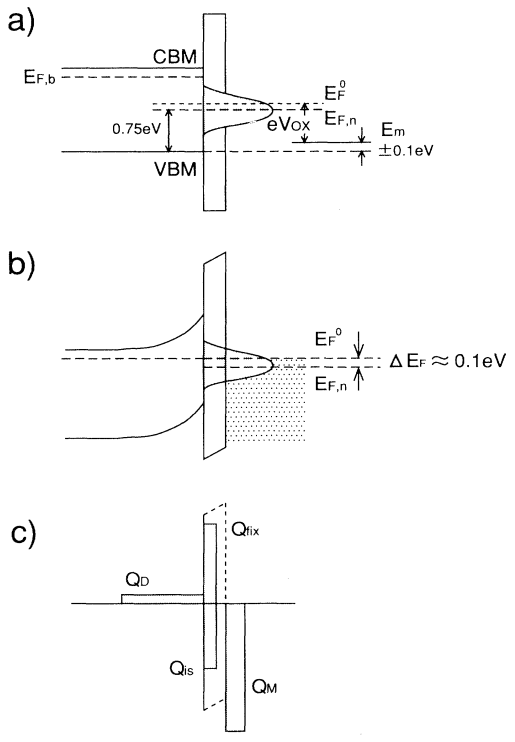


FIG. 5. Band diagrams for a GaAs-based MOS device: (a) before contact, (b) after contact, and (c) charge distribution after contact. Although the interface Fermi level E_F^0 cannot be defined before contact, it is included in (a) for the sake of convenience.

estimated to be $\sim 1\times 10^{15}$ cm^{-2} eV^{-1}, two orders of magnitude larger than that for the MOS device. However, it seems very difficult to obtain the real relation between the surface Fermi level and the metal work function, $E_{F,m}$, because it is very likely that the density of the antisite interface states depends on the reactivity of the metal. In fact, Spicer *et al.*[49] reported that Ga_{As} is the dominant defect in cases where deposited metals form compounds with As, e.g., Ga, Al, and Ti, whereas As_{Ga} is dominant in cases where Ga compounds are formed, e.g., Au.

C. Characteristics of the oxide layer

The valence-band spectrum for the oxide layer [Fig. 1(c)] is very similar to that of Ga_2O_3,[11] indicating that Ga_2O_3 is the dominant oxide species, in good agreement with the core-level spectra. Wilmsen[51] reported that the main species in the thermal oxide layer is Ga_2O_3 unless the oxidation temperature is very high, in good agreement with the present result. He also reported that pileup of elemental As occurs at the interface, and it is attributed to the instability of As_2O_3 in the presence of GaAs and the stability of Ga_2O_3/As. On the other hand, little or no As pileup was observed at the oxide/GaAs interface by Sealy and Hamment,[52] in agreement with the present study. The amount of elemental As at the interface may be greatly changed by a slight change in the oxidation conditions.

If a layered structure of the Ga oxide and the As oxide is assumed (this is not the case as described below), the thickness of the Ga oxide layer, $d_{Ga_2O_3}$, is estimated to be 3.3 nm from the ratio of the areal intensity of the Ga 3*d* peak for the oxide to that for the GaAs substrate.

The amounts of the shift of the oxide As 3*d* peaks from the substrate As $3d_{5/2}$ peak, i.e., 3.4 and 5.0 eV, show that As is in the As^{3+} and As^{5+} oxidation states, respectively.[11–13] Assuming the layered structure, the thickness of the As oxide layers, $d_{As_2O_3}$ and $d_{As_2O_5}$, is estimated to be 0.2 and 0.3 nm, respectively. Therefore the total thickness of the oxide layer is estimated to be 3.8 nm.

Hollinger, Skheyta-Kabbani, and Gendry[11] suggested that the thermal oxide layer is not a macroscopic mixture of As oxide and Ga oxide but is a single-phase nonstoichiometric compound in which AsO_3 (As^{3+}) and AsO_5 (As^{5+}) units are microscopically mixed with GaO_4 and GaO_6 units for Ga_2O_3. For a single phase, the thickness of the oxide layer *d* would be estimated more accurately from the following equation:

$$\frac{I_{Ga(oxide)}}{I_{Ga(GaAs)}}=\frac{D_{Ga(oxide)}}{D_{Ga(GaAs)}}[\exp(d/\lambda)-1]\ , \tag{15}$$

where $I_{Ga(oxide)}$ and $I_{Ga(GaAs)}$ are the areal intensities of the Ga 3*d* peaks for the oxide and for the GaAs substrate, respectively, $D_{Ga(oxide)}$ and $D_{Ga(GaAs)}$ are the densities of Ga atoms in the oxide and in the GaAs substrate, respectively, and λ is the mean free path of Ga 3*d* photoelectrons, which is taken to be 2.5 nm.[53,54] $D_{Ga(oxide)}/D_{Ga(GaAs)}$ in Eq. (15) is estimated using the following equation:

$$\frac{D_{Ga(oxide)}}{D_{Ga(GaAs)}}=\frac{2D_{Ga_2O_3}d_{Ga_2O_3}/M_{Ga_2O_3}(d_{Ga_2O_3}+d_{As_2O_3}+d_{As_2O_5})}{D_{GaAs}/M_{GaAs}}\ , \tag{16}$$

where $D_{Ga_2O_3}$ and D_{GaAs} are the specific gravity of Ga_2O_3 and that of GaAs, respectively, and $M_{Ga_2O_3}$ and M_{GaAs} are the molecular weight of Ga_2O_3 and that of GaAs, respectively. Using the values of 6.48 for $D_{Ga_2O_3}$, 5.32 for D_{GaAs}, 3.3 nm for $d_{Ga_2O_3}$, 0.2 nm for $d_{As_2O_3}$, and 0.3 nm for $d_{As_2O_5}$, the thickness of the single-phase oxide layer is estimated to be 3.8 nm, in good agreement with that estimated assuming the layered structure.

V. SUMMARY

The energy distribution of the interface states of the ⟨Pt/3.8-nm-thick oxide/GaAs(100)⟩ device is obtained from the analysis of the bias-induced energy shift of the substrate As 3*d* peak measured as a function of the bias voltage. The energy distribution has four peaks. The 0.75-eV peak has the highest density of $\sim 1\times 10^{13}$ cm^{-2} eV^{-1} (total density 1.9×10^{12} cm^{-2}) and is attributed to the (+/0) transition of the As_{Ga} antisite defect. The interface Fermi level is partly pinned by this defect and is located at 0.85 eV above the VBM. From the density of the interface states near the Fermi level, the density of the fixed oxide positive charge is estimated to be $(2-3)\times 10^{12}$ cm^{-2}. The 0.5-eV interface states are tentatively attributed to the (++/+) transition of the As_{Ga} antisite defect. The 0.15-eV interface states with a total density of 1.3×10^{12} cm^{-2} are attributed to the Ga_{As} antisite defect. The 1.1-eV interface states with a total density of 8×10^{11} cm^{-2}, which have a nominal effect on Fermi-level pinning, are attributed to the Ga vacancy defect.

A simple calculation shows that $d\phi/d\chi_M$ for the present device is 0.24, indicating partial Fermi-level pinning. If the density of the interface states for thick metal-deposited GaAs Schottky devices is assumed to be the same as that for the present MOS device (1×10^{13} cm^{-2} eV^{-1}), $d\phi/d\chi_M$ is estimated to be almost unity, in disagreement with previous studies. Therefore it can be concluded that the density of the interface states for the MOS device is much lower than that for Schottky devices.

The oxide layer prepared by heating the GaAs wafer at 500 °C for 5 min in oxygen is mainly composed of Ga_2O_3, with a small amount of AsO_3 (As^{3+}) and AsO_5 (As^{5+}) units. Using the ratio of the density of Ga atoms in the oxide layer to that in the GaAs substrate, the thickness of the single-phase oxide layer is estimated to be 3.8 nm from the Ga 3*d* spectrum.

ACKNOWLEDGMENTS

We are grateful to F. Sakamoto of Marubun Corporation for measuring the XPS spectra. We are also grateful to Sumitomo Electric Industries for supplying the *n*-type GaAs(100) wafers. We wish to acknowledge the Iwatani Naoji Foundation's Research Grant for financial support.

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