PHYSICAL REVIEW B VOLUME 50, NUMBER 24 15 DECEMBER 1994-II

Interfacial defects in $Si_{1-x}Ge_x$/Si quantum wells detected by deep-level transient spectroscopy

Qinhua Wang and Fang Lu
Fudan T. D. Lee Physics Laboratory, Fudan University, Shanghai, China

Dawei Gong and Xiangjun Chen
Surface Physics Laboratory, Fudan University, Shanghai, China

Jianbao Wang, Henghui Sun, and Xun Wang
Fudan T. D. Lee Physics Laboratory, Fudan University, Shanghai, China

(Received 9 May 1994; revised manuscript received 19 September 1994)

The carrier-emission processes from quantum wells and from deep-level defects have been identified in deep-level transient spectroscopy (DLTS) measurements. The emissions from quantum wells contribute to a majority carrier peak, from which the valence-band offset ΔE_v at the heterointerface is derived. For $Si_{0.67}Ge_{0.33}$/Si, our experimental result $\Delta E_v = 0.24$ eV is comparable with the theoretical prediction and previous measurement. The emission of carriers from a high density of interfacial defects gives rise to a minority carrier signal in DLTS, which can be detected only by using an injection pulse with a relatively large pulse width. The partial relaxation of the misfit strain or the nucleation of dislocations may be responsible for the formation of interfacial defects.

I. INTRODUCTION

Deep-level defects in $Si_{1-x}Ge_x$/Si quantum-well structures play an important role in determining their electrical and optical properties. $Si_{1-x}Ge_x$/Si is a type of lattice mismatched system, the partial or full relief of misfit strains at the heterointerfaces will cause the formation of dislocations which will deteriorate the properties of quantum wells. The most effective method in measuring the deep-level defects is deep-level transient spectroscopy (DLTS), which has been successfully employed to study the characteristics of deep-level defects in many semiconductor bulk materials. In recent years, DLTS has been applied to study quantum-well structures of III-VI semiconductor materials,[1,2] and has proved to be a useful method to determine the band offset at the heterointerface.[3] In a quantum-well structure, the emission and capture of carriers confined in the well regions behave similarly to the emission and capture of carriers by the deep-level defects. It is thus in principle possible to observe these two phenomena by DLTS. However, in many cases, the interference between the DLTS signals from defects and that from the quantum well makes the data analysis and peak identification difficult. The first attempt to detect the deep levels in a $Si_{1-x}Ge_x$/Si system by DLTS was made by Brighten *et al.*[4] They observed the trap distributions in the Si cap and $Si_{1-x}Ge_x$ layer but not the interfacial defects. In this work, we use DLTS measurements to distinguish two different thermal emission processes, i.e., the emission from defects and the emission from quantum wells, by appropriately setting the experimental parameters.

II. EXPERIMENTAL METHODS

The samples were grown by molecular-beam epitaxy (MBE) on p^+-type Si(100) substrates. Before the growth of heterojunction or quantum well, a Si buffer layer with the thickness of 300–500 nm was deposited. The structures of the samples are shown in Table I. All the growths were carried out at the substrate temperature of 500 °C. The thicknesses and the Ge contents of the layers were controlled by the beam fluxes of coevaporated Si and Ge sources, and were monitored by two quartz crystal oscillators. *In situ* Auger electron spectroscopy and *ex situ* x-ray diffraction measurements have been used as calibration. The unintentional doped films were found to be *p* type in their conductance. After the MBE growth, an Ohmic contact was made at the back side of the wafer by evaporating the Al film followed by alloying at 500 °C in N_2 ambient, and a Schottky contact was formed on the front side of the sample later by evaporating the Al dot without alloying.

The *C-V* measurements were used to determine the distributions of carrier concentrations in the samples, from which the different regions could be identified. A computer-controlled DLTS system was used to measure the carrier emissions from both the quantum wells and defects.

Doing the data analysis, the DLTS signals contributed by the defects were treated by the formula derived for bulk materials. For the DLTS signals of quantum-well emissions, the method of Debbar, Biswas, and Bhattacharga[3] was used to derive the band offset at the heterointerface. The emission rate e_p of holes in a quantum well across the barrier region is given by

$$e_p = \alpha\sqrt{kT}\exp\left[-\frac{\Delta E}{kT}\right], \tag{1}$$

where α is a temperature-independent constant, k is the Boltzmann constant, and ΔE is the activation energy, which is the difference in energy between the first hole subband E_1 and the top of the well. The valence-band

TABLE I. Structural parameters of samples.

Sample	Si buffer thickness (nm)	Si_xGe_{1-x} well		Si barrier thickness (nm)	Number of periods	Si cap thickness (nm)
		x	thickness (nm)			
A	300	0.1	100		1	300
B	500	0.33	15		1	270
C	300	0.25	4	15	10	50
D	300	0.5	4	15	10	50

offset ΔE_v can be given by the following relation:

$$\Delta E_v = \Delta E + E_1 + e\Delta V \ , \qquad (2)$$

where ΔV is the potential difference between the two sides of the well, and e is the charge of the electron.

III. RESULTS AND DISCUSSION

A. Double heterojunction

The thickness of the $Si_{0.9}Ge_{0.1}$ layer of sample *A* is 100 nm, which is too large to be considered as a quantum well. The sample is actually a double heterojunction. Its carrier distribution measured by the *C-V* technique is shown in Fig. 1. The charge transfers at the heterointerfaces lead to the depletion of holes in the Si cap and the accumulation of holes in the SiGe layer. The points *a*, *b*, and *c* in Fig. 1 correspond to the reverse bias V_R of 0, 1, and 3 V, respectively. DLTS signals measured at three different reverse biases and with different injection pulse amplitudes V_P are shown in Fig. 2. The injection pulse makes the diode less reverse or even forward biased. According to Fig. 1 and the experimental condition, the depletion region of the Schottky diode extends basically over the Si cap, heterointerface, and the bulk of the SiGe alloy layer for the spectra *a*, *b*, and *c* in Fig. 2, respectively. In spectra *a* and *c*, no deep-level defects could be observed in the Si cap and the SiGe layer. While at the heterointerface region *b*, DLTS shows a majority carrier peak, which may be attributed to the thermal emission of holes accumulated at the SiGe side of the heterointerface. This has been verified by the admittance spectroscopy measurement[5] (not shown here), where a maximum of conductance appeared near the temperature as that of the DLTS peak *b* in Fig. 2. The activation energy derived from Eq. (1) is 0.06 eV, which is close to the band offset of 0.07 eV for $Si_{0.9}Ge_{0.1}$/Si heterojunction by theoretical prediction.[6] The capture cross section related to the scattering rate of carriers into the well is 10^{-22} cm^2. Besides the majority carrier peak, no other DLTS signal related with defects could be observed. The whole sample may be regarded as a defect-free one. The small Ge composition makes the SiGe alloy layer and Si cap layer grow pseudomorphically without the nucleation of dislocations by relieving the misfit strain.

B. Single quantum well

Sample *B* is a single quantum well. Its *C-V* carrier distribution indicates that the holes are accumulated in the thin well region and the distribution width (full width at half maximum) is about the same as that of the well width (15 nm).[7] Figure 3 shows the DLTS spectrum taken at the reverse bias of -1 V and pulse amplitude of 2 V. Besides the majority carrier peak, which is attributed to the hole emission from the well, there also exists a minority carrier peak which could not be detected unless the duration of injection pulse is large enough. In our case, it must be larger than 10 ms.

The activation energy of the majority carrier peak is determined to be 0.23 eV by using Eq. (1). For well width

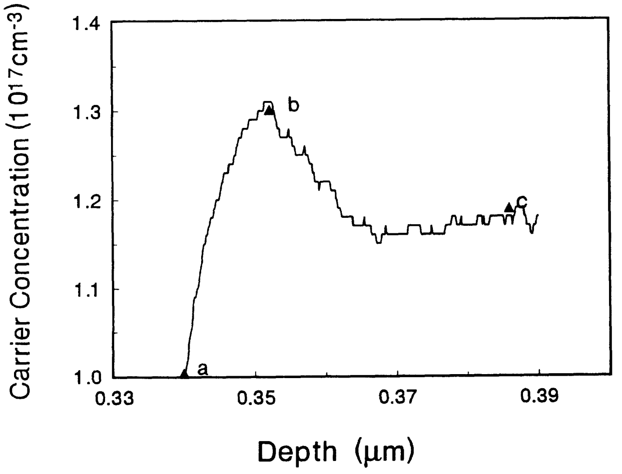

FIG. 1. *C-V* carrier concentration profile of sample *A*.

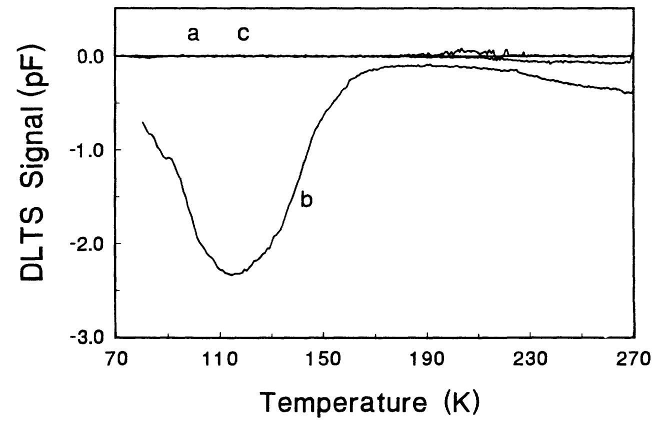

FIG. 2. DLTS spectra of sample *A* at different experimental conditions: *a*, $V_R = 0$ V, $V_P = 1.5$ V; *b*, $V_R = -1$ V, $V_P = 1.5$ V; *c*, $V_R = -3$ V, $V_P = 2$ V.

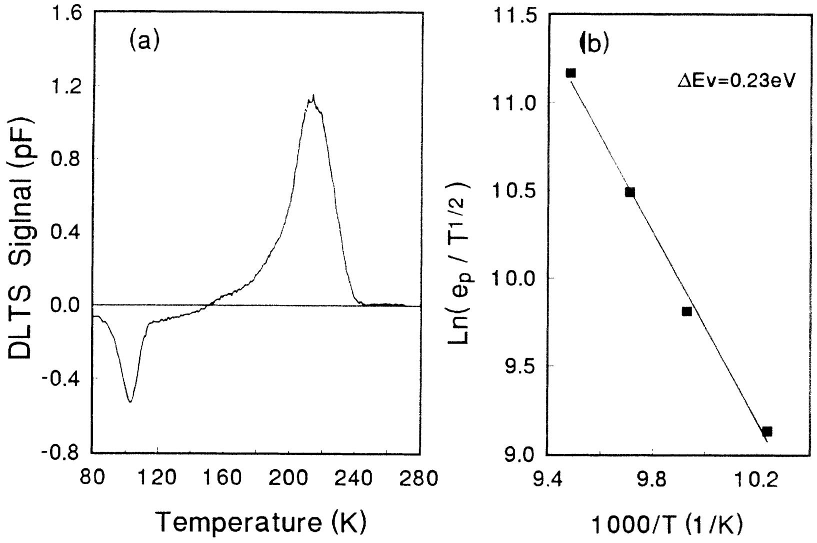

FIG. 3. (a) DLTS spectrum of sample B at $V_R=-1$ V and $V_P=2$ V. (b) $\ln(e_p/T^{1/2})\sim 1/T$.

of 15 nm and $x=0.33$, E_1 is very small ($\sim$3 meV) and could be neglected, the measured band offset is 0.24 eV by considering the effect of electric field. The band offset is agreed with its theoretical value 0.24 eV. The band offset of $Si_{0.7}Ge_{0.3}/Si$ measured by Vescan *et al.*[8] for a single quantum well was 0.22 eV, which is comparable with our result. However, the DLTS peaks in their measurements were broadened due to the thickness variations of the SiGe layer and the presence of SiGe islands in the interface.[8] In our case, we did not see the peak broadening at all. The Arrhenius curve $\ln(e_p/T^{1/2})-1/T$ follows a nice monoexponential relation as shown in Fig. 3(b). It again verifies that the DLTS majority carrier peak is contributed by the thermal emissions of holes from quantum well.

The DLTS peak height of the quantum-well emission varies under different reverse biases. By increasing reverse bias, the height of the majority carrier peak increases first and decreases after reaching a maximum. This result is in qualitative agreement with the bias voltage dependence of the peak intensity of an $In_{1-x}Ga_xAs/Al_{1-y}Ga_yAs$ single quantum well by Debbar, Biswas, and Bhattacharga[3] and could only be explained by the carrier emission from the quantum well rather than from defects. No defects could be detected for the Si layer.

In ordinary DLTS measurements, the minority carrier signal is not visible in the Schottky barrier diode. When the diode was made on a p-type semiconductor, only those deep levels located below the midgap can be observed as majority carrier signal in DLTS measurements. The origin of the minority carrier peak in Fig. 3(a) can be explained as follows. If high-density donorlike defects, whose levels are located above the midgap, exist in a very thin layer near the interfacial region, the Fermi level will pin near the top of the defect levels and the interfacial region will be converted into an inversion layer due to the compensation of the valence-band hole concentration by the electrons on the defect levels. Under reverse bias, a unified Fermi level no longer exits in the space-charge region, the electron and hole concentrations vary according to their quasi-Fermi level E_{Fn} and E_{Fp}, respectively. Crowell and Beguwala[9] pointed out that the quasi-Fermi levels are invariant in the space-charge region of a Schottky diode and E_{Fn} coincides basically with the Fermi level of the contact metal electrode. As the bias increases, E_{Fn} shifts downward slightly. Due to the large density of interfacial defects, a small variation of Fermi-level position still induces a significant change of electron concentration on the defect levels. The emission of electrons from defect levels into the conduction band reduces the negative charges in the space-charge region. In order to maintain the electric neutralization, the space-charge region must extend. The transient capacitance thus decreases and a positive DLTS signal is expected. Besides, the defect levels located near E_{Fn} are not very efficient in capturing electrons. It is thus necessary to use larger pulse duration to enhance the emission and capture processes in DLTS measurements.

From the above analysis, it can be seen that the minority carrier peak originates from the emission of interfacial defects. The depletion-accumulation region of a single quantum well occurs at the heterointerface region. It is therefore easier to change the depletion layer into an inverse layer if high-density donorlike defects do exist there. Unlike the deep-level defects in bulk materials in which we can determine the defect density by DLTS, for interfacial defects in our case, we cannot determine the defect density if they distribute spatially in a very narrow region with unknown thickness. Following the approach in Ref. 4, the apparent defect concentration in sample B is about 10^{14} cm^{-3}.

Figure 4 shows the DLTS signal of a minority carrier under different reverse biases. The peak height passes through a maximum at a reverse bias of about 1.5 V. Furthermore, by etching away the Si cap and the SiGe quantum-well layer, all the DLTS signal of majority carriers and minority carriers disappeared. We therefore conclude that the DLTS peaks can only come from the quantum well and its interfaces.

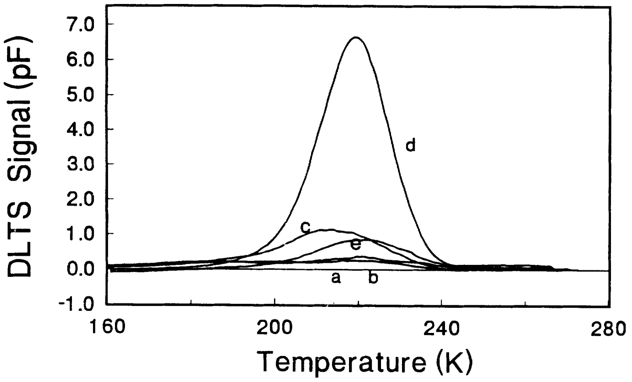

FIG. 4. The minority carrier peak of sample *B* varies with the V_R (*a*) 0 V, (*b*) 0.5 V, (*c*) 1.0 V, (*d*) 1.5 V, (*e*) 2.0 V, $V_P=2$ V.

C. Multiple quantum wells

Figure 5 shows the DLTS spectra of two multiple-quantum-well samples *C* and *D*. Both the majority carrier peak and the minority carrier peak of sample *C* are not well identified. The majority carrier peak of the quantum-well emission in sample *C* is expected to appear at a temperature below 77 K, i.e., out of the temperature range in Fig. 5, while for sample *D*, two majority peaks and one minority peak are clearly seen. The activation energy of peak D_2 is 0.30 eV, which could be attributed to the hole emission from quantum wells. Another majority peak D_1 is rather wide in its peak width and thus might not be contributed by a single level. The minority carrier peak D_3 behaves similar to that in single quantum-well sample in terms of the peak height versus bias voltage relation. The same origin of the minority carrier peak is expected. The peak here seems quite noticeable, which implies the existence of a high density of interfacial defects for the quantum-well structure with high Ge composition. Also, the depletion of the barrier regions makes the minority carrier peak appear more easily.

By comparing the results of the above four samples, it could be seen that the minority carrier peak appears in samples with larger Ge contents, that is, sample *B* ($x=0.33$) and sample *D* ($x=0.5$). For these two samples, the thickness of the SiGe alloy layer is larger than the critical thickness of pseudomorphic growth of SiGe on Si predicted by the Matthews-Blakeslee equilibrium theory,[10] but smaller than the critical thickness determined by the experiment under the growth temperature of 550 °C,[11] as shown in Table II. The samples are in the metastable regime, where the large misfit strains (which are proportional to *x*) would be partially relaxed. Although the samples are nominally pseudomorphic and their cross-sectional transmission electron microscopic pictures did not show threading dislocations across the samples, the existence of high densities of interfacial traps might be indicative of the partial relaxation of large misfit strains in these two samples. For multiple-quantum-well sample *C*, the thickness of the SiGe layer is well below the theoretically predicted critical thickness. The total thickness of multiple quantum wells is also smaller than the critical thickness of an equivalent SiGe alloy layer (with Ge content of ~0.05) grown on Si. So the sample could be thought of as in thermodynamic equilibrium. The relaxation of misfit strain could be neglected. As with sample *A*, although the thickness of the SiGe alloy exceeds the theoretically predicted critical thickness, it is still one order of magnitude smaller than the experimental value. The relaxation of misfit strain seems unlikely. In addition, the small lattice mismatch in this sample will not give rise to remarkable effect on the nucleation of dislocations even if the partial relaxation of misfit strain occurs.

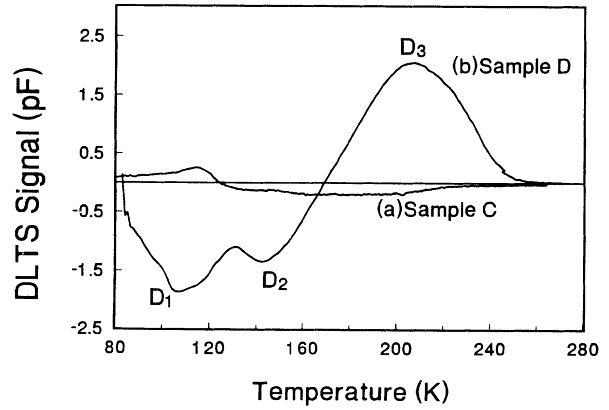

FIG. 5. DLTS spectra of samples *C* and *D* measured at $V_R=-1$ V, $V_P=2.5$ V.

TABLE II. Critical thicknesses for pseudomorphic growth.

	Si_xGe_{1-x} layer		Critical thickness (nm)	
Sample	*x*	thickness (nm)	theory[a]	experiment[b]
A	0.1	100	25	2000
B	0.33	15	5.5	30
C	0.25	4	8	100
D	0.5	4	3	10

[a] Matthews-Blakeslee model (Ref. 10).

[b] Experimental results by Bean *et al.* (Ref. 11) at a growth temperature of 550 °C.

IV. CONCLUSIONS

The carrier emission processes from the quantum wells and from the deep-level defects have been identified in the DLTS measurements. The emissions from quantum wells contribute to a majority carrier peak, from which the valence-band offset at the heterointerface is derived. For $Si_{0.67}Ge_{0.33}$/Si, our experimental result $\Delta E_v=0.24$ eV is comparable with the theoretical prediction and previous measurement. The emission rate of carriers from quantum wells follows a monoexponential relation with temperature. The emission of carriers from a high density of interfacial defects gives rise to a minority carrier signal in DLTS, which could be detected only by using an injection pulse with relatively large pulse width. The minority carrier peak is significant in samples with large Ge compositions. The partial relaxation of misfit strains may be responsible for the formation of interfacial defects. To clarify the mechanism of interfacial defects, further investigation is needed.

ACKNOWLEDGMENTS

This work was partially supported by the National Natural Science Foundation of China and the State Commission of Science and Technology.

---

[1] D. J. As, P. W. Epperlein, and P. Mooney, J. Appl. Phys. **64**, 2408 (1988).

[2] S. L. Feng, J. C. Bourgoin, A. Mauger, D. Stievenard, E. Barbier, J. P. Hirtz, and A. Chomette, Phys. Rev. B **39**, 13 252 (1989).

[3] N. Debbar, D. Biswas, and P. Bhattacharga, Phys. Rev. B **40**, 1058 (1989).

[4] J. C. Brighten, I. D. Hawkins, A. R. Peaker, R. A. Kubiak, T. E. Whall, and E. H. C. Parker, in *Extended Abstracts of the 1993 International Conference on Solid State Devices and Materials,* edited by K. Tada (Makuhari Messe, Chiba, Japan, 1993), p. 391.

[5] K. Nauka, J. I. Kamins, J. E. Turner, C. A. King, J. L. Hoyt, and J. F. Gibbons, Appl. Phys. Lett. **60**, 195 (1992).

[6] R. People and J. C. Bean, Appl. Phys. Lett. **48**, 538 (1986).

[7] E. F. Schubert, R. F. Kopf, F. M. Kuo, H. S. Luftman, and P. A. Garbinski, Appl. Phys. Lett. **57**, 497 (1990).

[8] L. Vescan, R. Apetz, and H. Luth, J. Appl. Phys. **73**, 1427 (1993).

[9] C. R. Crowell and M. Beguwala, Solid State Electron. **14**, 1149 (1971).

[10] J. W. Matthews and A. E. Blakeslee, J. Cryst. Growth **27**, 118 (1974).

[11] J. C. Bean, L. C. Feldman, A. T. Fivry, S. Nakahara, and I. K. Robinson, J. Vac. Sci. Technol. A **2**, 436 (1984).