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Observation of carrier-concentration-dependent reflectionless tunneling in a superconductor–two-dimensional-electron-gas–superconductor structure

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We report on the conductance of a short (<100 nm) *silicon-based* two-dimensional electron gas with superconducting source and drain electrodes. Below 1 K a zero-bias enhanced conductance is observed which depends on the carrier concentration in the electron gas. The data can qualitatively be understood as due to reflectionless tunneling, i.e., quantum-coherent-enhanced Andreev scattering.

Traditionally, mesoscopic transport phenomena are studied by coupling a short conductor to metallic contacts at different chemical potentials. The consequences of using *superconducting* contacts are presently largely unexplored. A detailed experimental investigation of many aspects of the conduction mechanism through such contacts is lacking, in particular its energy-dependence and dependence on phase-coherence. In this paper we focus on a phenomenon reported by Kastalsky *et al.*[1] They observed an enhanced conductance around zero bias at a superconductor-semiconductor junction. This enhanced conductance was found to decrease strongly with bias voltage and applied magnetic field, and quantum-coherent scattering combined with Andreev reflections have been suggested by Van Wees *et al.*[2] as an explanation. In the remaining part of this paper we will call this effect reflectionless tunneling (RLT) following a proposal of Marmorkos *et al.*[3]

We have developed a type of superconductor-semiconductor metal-oxide-semiconductor field-effect transistor (MOSFET) structure (Fig. 1), which allows us to study this phenomenon in a well-characterized way. Fabrication of the device is described in more detail in Ref. 4. All previous experiments reported only on magnetic field and temperature dependencies, Refs. 1 and 5 dealt with scattering in three dimensions, Ref. 6 reported reflectionless tunneling in a structure with a two-dimensional electron gas (2DEG). The present experiment uses a 2DEG with a controlled change of the electron density.

The device is structured as a short-channel MOSFET with superconducting source and drain contacts. These contacts are made by selective chemical vapor deposition of amorphous W-Ge,[7] which is superconducting with a transition temperature of about 4 K, the precise value depending on the thickness. It has an upper critical field of about 5 T. The fabrication procedure allows the simultaneous formation of a self-aligned gate with a length of less than 100 nm. We used a strong As-implant (doping at the surface $\approx 2 \times 10^{20}$ cm^{-3}) underneath the a-W/Ge superconducting contacts to promote superconductivity in the heavily doped silicon. The conductance of the samples is studied at temperatures below 1 K in a ^{3}He-^{4}He dilution refrigerator equipped with a superconducting magnet. The conductance is measured with standard lock-in techniques and additional care is taken to avoid the influence of external noise sources. The 2D nature of the electron gas was verified by Shubnikov–de Haas oscillations.

The measured I-V curves for various carrier concentrations, i.e., gate voltages, are shown in Fig. 2. In contrast to Refs. 8 and 9 we did not observe a supercurrent. A gradual decrease of the resistance with increasing gate voltage is clearly visible, demonstrating a proper field effect operation of the device. A change in slope is observed around 0.6 meV, the energy gap value of the superconducting electrode. For voltages above the gap voltage

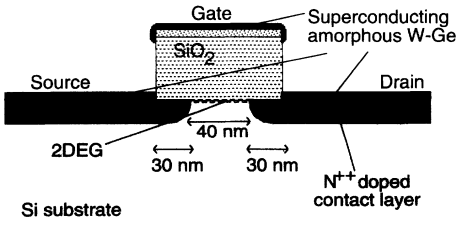

FIG. 1. Cross section of the device.

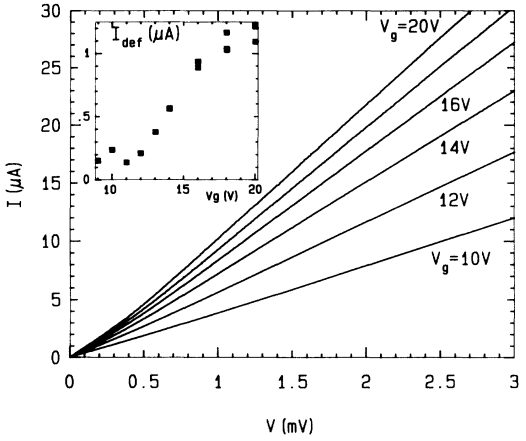

FIG. 2. *I-V* characteristic of the device at different gate voltages at 200 mK. The inset shows the current deficit as function of gate voltage.

the curve does not extrapolate to the origin but intercepts the current axis at negative values, a phenomenon known as "current-deficit."[10] In Fig. 2 (inset) the current deficit is shown as a function of gate voltage. Clearly the amount of current-deficit decreases with decreasing carrier concentration. Heslinga *et al.*[10] have identified the current deficit as due to a nonequilibrium distribution of carriers in the normal conductor between the superconducting electrodes. The degree of nonequilibrium depends on the competition between injection rate from the superconducting contact into the normal area and energy relaxation rate in the normal area. The physical origin is the blockage of conducting channels in a band of 2Δ due to the presence of the energy gap in the electrode. If the energy gap is absent these channels do conduct. Heslinga *et al.* assume that the voltage drop is mainly present across the interface. In our case a large part of the voltage drop occurs across the channel. The ratio between the voltage drop across the channel and across the interface increases with decreasing gate voltage. We assume that this phenomenon is the main reason for the decrease of the current deficit with decreasing gate voltage.

In the present paper we focus on the differential resistance around $V = 0$. From Fig. 2 we expect a broad maximum in resistance extending up to the gap voltage, where the curve would become flat. As shown in Fig. 3 such a broad maximum is indeed found. As the temperature is lowered below 1.2 K a narrow region of reduced resistance (or excess conductance) near zero bias clearly becomes visible, extending to approximately 0.1 meV. A similar signature has been reported previously for Nb-InGaAs interfaces by Kastalsky *et al.*,[1] Nb-Si interfaces by Magnée *et al.*[5] and in $GaAs/Al_xGa_{1-x}As$-Sn 2DEG structure by Lenssen *et al.*[6] An explanation based on quantum-coherent-enhanced Andreev reflection has been proposed by van Wees *et al.*,[2] i.e., reflectionless tunneling.[3]

Figure 3 shows the differential resistance as function of bias voltage for different gate voltages, temperatures [Fig. 3(a)], and magnetic fields [Fig. 3(b)]. As usual for MOSFET's, the resistance decreases with increasing elec-

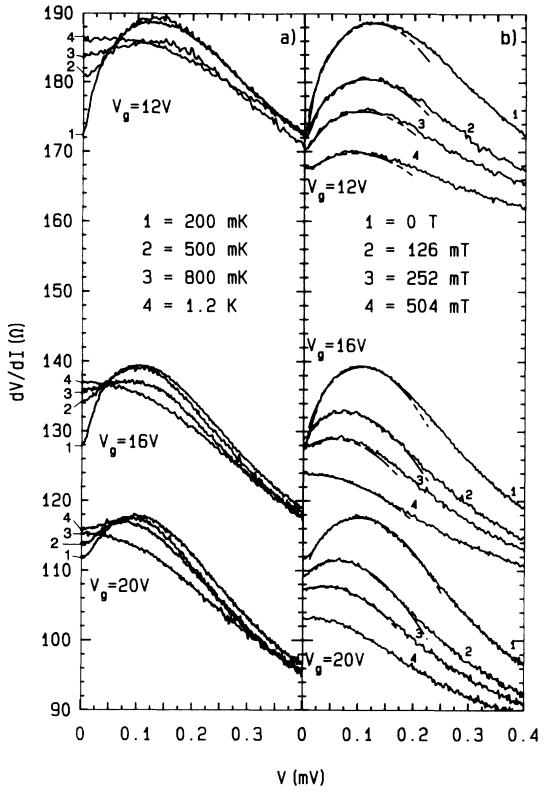

FIG. 3. Differential resistance as function of bias voltage at different gate voltages. (a) At different temperatures. (b) At different magnetic fields. The broken lines are fits using the expression given by Volkov and co-worker (Ref. 17) and using a parabolic background.

tron concentration (gate voltage). Similarly, the absolute size of the RLT structure decreases. Figure 4 shows the differential resistance as a function of voltage bias normalized to the normal-state resistance of the device R_N. The inset shows the difference ΔR between the minimum at $V = 0$ and the maximum at finite voltage, as a function of gate voltage. Apparently, the relative resistance change ΔR associated with the RLT is roughly gate voltage independent. In addition, we find from Fig. 3 that the temperature at which the RLT is fully suppressed (defined as the point where the differential resistance no longer decreases near $V = 0$) is not influenced by the carrier density, whereas the corresponding magnetic field is.

For the extraction of the device parameters the standard small source-drain voltage MOSFET model[11] is fitted to the low-temperature differential resistance at voltages well above twice the superconducting gap in which we neglect the proximity effect. In this MOSFET model, a resistance R_s is connected in series with the 2DEG region. This resistance models the contact resistance between metal and silicon as well as the resistance contribution of the heavily doped contact layer underneath the metal contact. The total resistance of the device is then given by

$$R_N = R_s + R_{2DEG} = R_s + d_{ox}L/W\mu\varepsilon_{ox}(V_g - V_t) \qquad (1)$$

where V_g is the gate voltage, V_t the threshold voltage, d_{ox} the thickness of the gate oxide, μ the mobility of

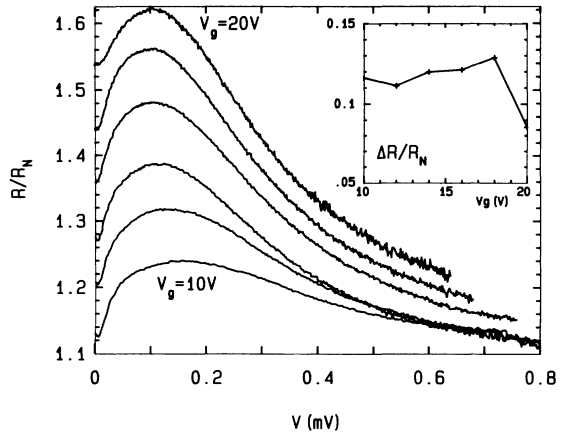

FIG. 4. Normalized differential resistance of the device as a function of bias voltage at different gate voltages, the upper one at 20 V, decreasing in steps of 2 V to the lowest one at 10 V. The curves are results normalized to the normal-state resistance as defined in Eq. (1). Inset: Magnitude of the normalized excess conductance as function of gate voltage.

the 2DEG, and $\varepsilon_{ox} = 3.45 \times 10^{-11}$ C/V m the dielectric constant of the gate oxide. W is the width and L the length of the channel. The channel length is the gate length (≈ 100 nm) minus the length of the heavily doped area reaching under the gate (twice about 30 nm).[12]

In our device the different parameters have the following values: $d_{ox} = 60$ nm, $L \approx 40$ nm, and $W = 5$ μm. A fit to Eq. (1) gives $R_s = 18 \pm 7$ Ω, $V_t = 5.78 \pm 0.15$ V, and $\mu = 180 \pm 70$ cm^2/V s. The relatively low mobility and high threshold voltage indicate[11] a high interface charge on the silicon-silicon dioxide interface. Another reason for the low mobility might be the high doping (around 10^{18} cm^{-3}) in the channel. The uncertainty in the mobility originates mainly from uncertainty in the determination of L. We can alternatively estimate R_s from the contact resistance and the resistance of the heavily doped silicon. In this case $R_s = 2\sqrt{R_c R_\square}/W$, where R_c is the contact resistance and $R_\square$ the sheet resistance of the heavily doped contact layer. We estimate $R_\square = 175$ Ω from the calculated doping profile[12] and obtain $R_c = 1.3 \times 10^{-6}$ Ωcm^2 (doping level 2×10^{20} cm^{-3}), using data from van der Jeugd *et al.*[13] The resulting value R_s=60 Ω is higher than the experimental value of 18 Ω given above, even without taking into account mobility degeneration caused by the perpendicular electric field. The discrepancy between the estimated series resistance and the fitting result might have its cause in the large uncertainties associated with the fit. In addition, the contact resistance is very difficult to measure and very sensitive to doping. For instance, we found that R_c decreased by a factor of 2 if some parameters in the simulation are slightly changed within the error margins of the processing conditions.

We believe that the conductance peak can be described by a modification due to phase-coherent processes of the Boltzmann-equation approach outlined by Heslinga *et al.*[10] First however, we need to address a crucial question related to the specific structure of our device. Ideally, the device (Fig. 1) should behave as a superconductor-2DEG-superconductor system. The additional complication here is the induced superconductivity within the heavily doped silicon, which causes a further intermediate region between the superconductor and the 2DEG. Moreover, the heavily doped layer extends to a certain depth underneath the gate. However if we replot the data of Fig. 4 by subtracting the resistance of the 2DEG [second part of Eq. (1)] against bias current, the traces fall almost on top of each other except near $V = 0$. The resistance anomaly strongly decreases with rising gate voltage, clearly indicating influence of the gate on the RLT. We can neglect the influence of the gate on the heavily doped silicon underneath it.

In MOSFETs the gate voltage controls the carrier concentration of the inversion layer through $N_s = \varepsilon_{ox}(V_g - V_t)/(ed_{ox})$ and thereby also controls the diffusion constant:[14] $D = \pi N_s \mu \hbar^2/(\nu e m^*)$, where m^* is the effective mass, which is 0.19 times the free electron mass, and ν the valley degeneracy in the (100) plane, which is 2.

Gao *et al.*[15] measured the phase breaking length in a 2DEG and found $l_\phi = 220$ nm at 1.76 K and a $T^{-1/2}$ dependence on temperature. Scaling this value for our lower mobility gives about a factor of 7 shorter phase breaking length. This means that at 1.2 K the phase breaking length in the 2DEG is about the same as the channel length (≈ 40 nm), but at lower temperatures it exceeds the channel length. In heavily n-doped silicon Heslinga and Klapwijk[16] measured $l_\phi = 408$ nm at 1.2 K and a $T^{-1.1}$ power law. The energy-dependent correlation length for superconducting correlations[17] $\sqrt{\hbar D/E}$ becomes shorter than the channel length only for $E > 0.15$ meV. Thus for bias voltages below about 0.15 mV and temperatures below 1 K both the correlation length and the phase breaking length exceed the channel length. In Fig. 3 these conditions coincide with the onset of RLT.

We now turn to a discussion of potential mechanisms behind the observed RLT. All the presently available models considered a somewhat idealized device configuration. However, a qualitative comparison with the observations should be possible. A semiclassical picture for the RLT has been proposed by van Wees *et al.*[2] In this explanation Andreev reflection and normal reflection on the superconductor-semiconductor interface are assumed, as well as elastic scattering in the semiconductor. Excess conductance is caused by constructive quantum interference that results from the phase conjugation between electrons and holes. This phase conjugation originates from Andreev reflection and is destroyed by finite energy, eV or kT, or a magnetic field.

Numerical simulations with a more rigorous treatment of the scattering have been done by Takane and Ebisawa[18] and Marmorkos *et al.*[3] Here, as in the model of van Wees *et al.*,[2] the calculation is done by using a disordered 2D square lattice connected on one side with a superconductor via a potential barrier and on the other side with a perfect-conducting lead. Only small bias voltages are considered ($V \ll \Delta$). Both groups find the RLT, but with a different bias, magnetic field, and disorder dependence than van Wees *et al.*[2]

Marmorkos *et al.*[3] define a magnetic field B_c at which

the excess condutance is reduced by one half. In wide channels ($W > l_\phi > L_N$) they find that B_c is given by $2\Phi_0/l_\phi L_N$ with Φ_0 the magnetic flux quantum and L_N the total length of the normal region. For our device this leads to $B_c \approx 0.3$ T, decreasing with increasing gate voltage, a value reasonably close to the observations and with the correct dependence on gate voltage. The same group also defines V_c, the bias voltage at which the excess condutance is reduced by a factor of 2. In Fig. 5 we plot quantities characteristic for the RLT as a function of gate voltage. The width of the excess conductance at the base (crosses) decreases with increasing gate voltage. The half-width (the definition used by Marmorkos *et al.*[3]) is roughly constant and increases at high gate voltages (open squares). According to Marmorkos *et al.*[3] V_c should be equal to the Thouless energy $[\pi D\hbar/e(L_N)^2]$. Given the geometry of our device we estimate the Thouless energy about 0.1 meV, which is clearly the right order of magnitude.

Analytic calculations using Green's function techniques were done by Volkov and co-workers[17] for double barrier structures (a SININ′ geometry with S a superconducting region, I a barrier, and N and N' normal regions) with bias voltages in the range from zero to above the gap Δ/e. In these calculations it is assumed that the length of the current path through the normal area L_N is larger than the pair coherence length $\xi_N(\Delta) = \sqrt{\hbar D/\Delta}$. Volkov and co-workers[17] provide an expression for the normalized excess conductance as a function of both voltage and magnetic field:

$$\sigma_d(v) = \left[1 + \left(\frac{h^4 + v^2}{v_0(h^2 + \sqrt{h^4 + v^2})}\right)^{1/2}\right]^{-1} \qquad (2)$$

with h the normalized magnetic field $h = 2\pi\lambda\xi_N(\Delta)B/\Phi_0$ with λ the London penetration depth and v the voltage eV normalized to the energy gap Δ. In Eq. (2) v_0 is a characteristic voltage, which depends on the barrier transmission and normal-state conductance of the normal metal N. Here it is used as a free parameter. Superposing a parabolic background on Eq. (2) the excess conductance, shown in Fig. 3(b), is very well reproduced, using λ and v_0 as fitting parameters. Excellent fits are obtained with v_0 varying by a factor of 10 for different magnetic fields. Strictly speaking if the definition for v_0 of Volkov and co-workers[17] applies, v_0 should be constant. However, our geometry is different from the double barrier tunnel device studied by Volkov and coworker. A further test is the magnetic field at which the RLT is fully suppressed. For our geometry we estimate a theoretical value in the order of 1 T, decreasing with increasing gate voltage, which is in reasonable agreement with the observations.

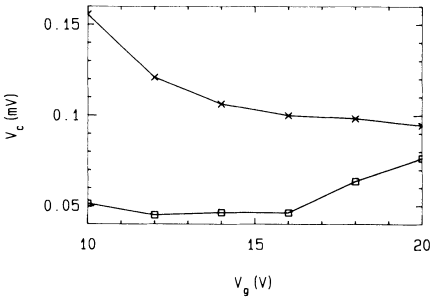

FIG. 5. Characteristic size of the RLT as a function of gate voltage. The symbols show both the width of the excess conductance peak at the base (crosses) and the half-width (open squares).

In conclusion, we have observed a dependence of reflectionless tunneling on the electron density in a 2DEG between superconducting electrodes. The relative strength of the RLT and the temperature at which the RLT is fully suppressed were found to be independent of carrier concentration. On the other hand, our data show that the magnetic field at which the RLT is suppressed does depend on carrier concentration and decreases with increasing carrier concentration. Presently available numerical calculations for several model geometries with a rigorous treatment of the scattering[3,18] and analytic Green's function approaches[17] provide a good estimate for the characteristic magnetic field.

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