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## Analytical model of a one-dimensional constriction with many occupied subbands: Calculation and experiment

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We have measured the differential conductance of two different one-dimensional (1D) constrictions with several occupied subbands at low temperature under conditions of high dc source-drain bias relative to the 1D subband spacing. The results are compared with a simulation based on a saddlepoint potential with and without a thin equipotential strip at the center. We fit the experimental results at high conductance by increasing the width of the equipotential strip with an increase in number of conducting subbands. For a split gate where the depth of the electron gas is 70 nm and where there are at most three occupied 1D subbands, a simple parabolic saddle-point model is sufficient. For a device where the depth of the electron gas is 27 nm and there are eight occupied 1D subbands, the modified potential model is needed to give good agreement with experimental data.

Quantized ballistic conductance, arising from the formation of one-dimensional (1D) electron energy subbands in a short and narrow constriction in a twodimensional electron gas (2DEG) remains the clearest example in lateral electron transport of a quantummechanical size effect.<sup>1</sup> In this paper we begin by reviewing previous models of the simple split gate. We then present the experimental and calculated differential conductance when there are several conducting 1D channels and the applied dc bias is of the same order as the 1D subband energy separation. The model used is analytically soluble in the direction of electron travel and in the direction of lateral confinement.

The simplest model of a 1D constriction comprises a constriction between two semi-infinite 2DEG planes with a hard-wall confining potential.<sup>2</sup> Transverse standing waves in the electron wave function allow the calculation of the 1D subband energy spacings. This model may be modified to incorporate a degree of adiabatic transport by having a linear decrease in width of channel approaching the constriction<sup>3</sup> or a finite radius of curvature to all the corners in the device.<sup>4</sup> In a numerical calculation using these models, electron phase coherence is assumed throughout the device. When sharp corners or hard walls are present, length resonances are predicted due to quantum-mechanical interference between phase-coherent components of the electron wave function. These have not been unambiguously observed in a simple split-gate device because it is difficult to pattern the 2DEG on a length scale comparable with the electron Fermi wavelength and maintain phase coherence throughout the whole device. Lithographic limitations restrict the sharpness of Schottky gate corners and the potential at the depth of the 2DEG is also smoothed because the Fourier components of the surface patterning decay exponentially with depth as  $\exp(-2\pi an/b)$ , where *n* is the order of the Fourier component, *a* is the depth of the 2DEG, and *b* is the inverse of the maximum spatial frequency in the pattern.<sup>5</sup> Even when the depth of the 2DEG is equal to the characteristic period of the lithography, the modulation is greatly reduced  $[\exp(-2\pi) \approx 0.001]$ .

A more realistic analytical model for a short constriction was applied by Büttiker, treating the electrostatic potential as a parabolic saddle point, leading to an equation for the potential,<sup>6</sup>

$$V(x,y) = V_0 - \frac{1}{2}m^*\omega_x^2 x^2 + \frac{1}{2}m^*\omega_y^2 y^2 .$$
 (1)

The saddle-point model is applicable principally where there are few 1D subbands and the device approaches pinch-off, but above a conductance of  $e^2/h$ . Within these limits, this model has been used with great success.<sup>7</sup> For larger numbers of 1D subbands in a long 1D wire, self-consistent Poisson-Schrödinger calculations show that the parabolic potential is flattened at the bottom by the screening effect of conduction electrons in the constriction.<sup>8</sup>

The model that we have chosen is based on a saddle point and approximates the self-consistent result in an analytical form with a thin equipotential region of width W in the middle of the lateral confining potential. For |y| > W/2,

$$V(x,y) = V_0 - \frac{1}{2}m^*\omega_x^2 x^2 + \frac{1}{2}m^*\omega_y^2 (|y| - W/2)^2$$
. (2a)

In the flat regions we have

$$V(x,y) = V_0 - \frac{1}{2}m^*\omega_x^2 x^2$$
 . (2b)

The width is sensitive to the number of electrons in the

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constriction. In the few-electron limit  $W \to 0$  and the confinement is parabolic with equidistant spacing of subbands,

$$E_n = \hbar \omega_y (n + \frac{1}{2}), \quad n = 0, 1, 2, \dots$$
 (3a)

The constriction widens with increasing electron density because of the additional screening, i.e., W increases while  $E - V_0$  remains constant. The 1D subband energy becomes<sup>9</sup>

$$E_n = \{-(\omega_y W/2\pi)(2m^*)^{1/2} + [\hbar\omega_y(n+\frac{1}{2}) + 2m^*(\omega_y W/2\pi)^2]^{1/2}\}^2 .$$
(3b)

The differential conductance at zero temperature is given by

$$G = \frac{2e^2}{h} \sum_{n} \{ (1-\beta)T_n[E_n - (1-\beta)eV_{\rm sd}] +\beta T_n(E_n + \beta eV_{\rm sd}) \}, \qquad (4)$$

where  $V_{\rm sd}$  is the source drain voltage,

$$T_n = 1/[1 + \exp(-\pi\varepsilon_n)] \tag{5}$$

and

$$\varepsilon_n = 2[E - E_n - V_0]/\hbar\omega_x . \qquad (6)$$

In deriving Eq. (4) we have assumed that the Fermi energy  $E_F > eV_{\rm sd}$ . The parameter  $\beta$  defines the potential drop over the constriction  $(0 \leq \beta \leq 1)$ :  $\beta V_{\rm sd}$  is the potential difference between the source region and saddle point and  $(1 - \beta)V_{\rm sd}$  from saddle point to drain. We assume that the voltage drop is symmetric across the device so that  $\beta = 0.5$  for conductance down to  $e^2/h$  and then drops linearly to zero at device pinch-off in order to match the experimental data. On general grounds  $\beta = 0$ when G = 0.

Comparisons between experimental and calculated data for two split-gate devices are presented.<sup>10</sup> Both are made by electron beam lithography with Nichromegold metallization overlaying a GaAs-Al<sub>x</sub>Ga<sub>1-x</sub>As heterostructure. The calculated data have not been corrected for the thermal smearing because the subband spacings deduced from the high dc bias differential conductance measurements are greater than 10 kT in both devices at their respective measurement temperatures.

The first device A544-QPC13 is a split gate with length 0.1  $\mu$ m and width 0.3  $\mu$ m fabricated on a 2DEG at a depth of 70 nm with sheet carrier density  $n_s = 4 \times 10^{11}$  cm<sup>-2</sup> ( $E_F = 14$  meV) and mobility  $\mu = 2 \times 10^6$ 

V cm<sup>-2</sup>s<sup>-1</sup>. Measurements were made by phase-sensitive detection at a temperature of 300 mK with a constant ac excitation of 10  $\mu$ V. Conductance versus gate voltage characteristics with  $V_{sd} = 0$  show that this device has only three occupied 1D subbands at channel definition and a fit with a simple parabolic model gives the factor  $g = \omega_y/\omega_x = 1.5$ . Figure 1(a) shows the experimental differential conductance versus gate voltage for incremental  $V_{sd}$  for  $V_{sd} = 0$ -4.3 mV with a 0.031-mV step. Figure 1(b) shows the calculated differential conductance versus energy for incremental  $V_{sd}$  based on the simple parabolic saddle point with no equipotential strip and matches the experimental data closely. The equal length "bundles" show that the parameter  $\beta$  is close to 0.5 and the fact that the crossing points lie on a straight



FIG. 1. (a) Sample A544-QPC13: Experimental differential conductance (G) vs gate voltage for incremental  $V_{\rm sd}$ for  $V_{\rm sd} = 0-4.3$  mV with a 0.031-mV step. (b) Sample A544-QPC13: Theoretical conductance G as a function of electron energy at constant source-drain bias  $V_{\rm sd}$ . The parameter  $\beta$  tends to zero linearly below the lowest plateau. The parameters  $\hbar \omega_y = 4.3$  meV and g = 1.5 are obtained by comparing theoretical values of G vs energy with experiment.

line shows that the spacings between the first three 1D subbands are equal, as predicted by the parabolic model.

The second device A704HIT2-2 is a split gate formed by two offset rectangular corners with a separation of 0.1  $\mu$ m fabricated on a 2DEG at a depth of 27 nm with  $n_s = 1 \times 10^{12} \text{ cm}^{-2} (E_F = 35 \text{ meV}) \text{ and } \mu = 7.1 \times 10^5 \text{ V cm}^{-2} \text{ s}^{-1}$  after illumination by a red light-emitting diode.<sup>11</sup> The radius of curvature of the gate metallization in this device is between 10 and 20 nm. Measurements were made by phase-sensitive detection at a temperature of 4.2 K with a constant ac excitation of 100  $\mu$ V. The sheet carrier density, shallow depth of 2DEG, and short channel of the second device give large subband energy spacings and this allows the measurements to be made at 4.2 K. A correction has been made for the effect of a 500- $\Omega$  series resistance on the conductance and the sourcedrain bias across the device. Conductance versus gate voltage characteristics with  $V_{sd} = 0$  show that this device has at least seven occupied 1D subbands at channel definition and a fit with a simple parabolic model for the first few 1D subbands gives the factor  $g = \omega_y/\omega_x = 2$ . Figure 2(a) shows the experimental differential conductance versus  $V_{\rm sd}$  for incremental gate voltage for gate voltage  $V_g = -0.7$  to -1.2 V with a step of -0.01 V. The device is modeled well by the simple saddle-point model at low conductance. A nonparabolic term in the potential would lead to deviations of the plateaus conductance away from the exact half-plateaus values at high dc bias.<sup>7</sup> At high conductance, the analytical model of Eq. (2) is more appropriate. Figure 2(b) shows the differential conductance versus  $V_{\rm sd}$  for incremental electron energy calculated from Eqs. (3b) and (4) with the value of Wvarying nonlinearly between 0 at subband index n = 1and 65 nm at n = 7.

We have confirmed the validity of the simple parabolic saddle-point model with parameters  $\hbar \omega_y$ ,  $\beta$ , and  $\omega_y/\omega_x$ for a simple split gate with few (<4) occupied 1D subbands. We have also presented an analytical model with an additional parametric equation W(n) which describes the differential conductance in the range when there are large numbers (approximately seven) occupied 1D subbands at channel definition. Both models are valid when





FIG. 2. (a) Sample A704HIT2-2: Experimental differential conductance vs  $V_{\rm sd}$  for incremental gate voltage for gate voltage  $V_g = -0.7$  to -1.2 V with a -0.01-V step. The dashed lines indicate half-plateaus used for finding the width W. Dot-dashed lines connect integer plateaus as predicted by the model. (b) Theoretical conductance for device A704HIT2-2 according to the present model with  $\hbar\omega_y = 9$  meV, g = 2. The dashed lines indicate half-plateaus used for finding the width W. Dot-dashed lines connect integer plateaus as predicted by the model. Below the lowest plateau the parameter  $\beta$  tends to zero linearly with  $(E - V_0)$ .  $E_F > E - V_0$ , and when the applied dc bias is less than or equal to approximately two times the 1D subband spacing. The models fit the experimental data if the parameter  $\beta$  is reduced linearly from 0.5 to zero between a conductance of  $e^2/h$  and pinch-off. We would like to thank C. J. B. Ford for useful discussions and D. Heftel, T. Jobson, and S. Gymer for technical support. We would like to acknowledge financial support from the Science and Engineering Research Councils of Sweden and the United Kingdom.

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