Theoretical study of electric-field effects in high-T_c oxide superconductors using an ultrathin-metal-insulator superlattice model

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A theory is proposed for describing electric-field effects to a superlattice covered by an insulator and a gate electrode. The superlattice consists of alternately stacked metal and insulating layers. The carriers in the metal layers behave as two-dimensional free particles, and they can move by tunneling in the insulating layer between two adjacent metal layers. The field effects are induced by application of a voltage to the gate electrode. The model is applied to an example whose superlattice is an oxide superconductor, $Bi_2Sr_2CaCu_2O_8$. Numerical results exhibit the penetration of the electric field and potential into the superlattice, and the condition of the carrier depletion. The theory also predicts jumps of the capacitance of the diode as a function of the applied gate voltage.

I. INTRODUCTION

Electric-field-induced charging effects to superconductors were studied by Glover and Sherill in 1960.[1] They investigated the changes in superconducting transition temperature T_c of tin and indium by application of voltages to metal-insulator-superconductor structures, but the obtained changes were extremely small,[1] which was ascribed to the large carrier densities of conventional superconducting metals. This led to the electric-field penetration length of less than 1 Å.[2] To get large effects by application of electric fields, superconducting plates must be thin on the same scale, but their fabrication, particularly together with an insulator, is technologically difficult and how the superconductivity on such a scale changes from that of thick cases is a different subject.[3]

Characteristics of recently discovered high-T_c oxide superconductors are that the carrier densities are small compared to the conventional superconductors, and the superconductivity is very sensitive to the carrier density.[4] The above-mentioned penetration length becomes around tens of Å and thus larger electric-field effects are expected. Furthermore, the superconductivity even appears at the unit-cell thickness limit and after making heterostructures to insulators (most usually oxides). Terashima, Shimura, and Bando showed the superconductivity of one unit cell (11.7-Å-thick $YBa_2Cu_3O_x$) sandwiched by semiconducting $PrBa_2Cu_3O_x$ layers.[5] In the case of the Bi-Sr-Ca-Cu-O system, the superconductivity was shown by 35-Å-thick films,[6] and by a heterostructure to a $SrTiO_3$ film.[7] The development of atomic-layer-controlled technologies for heteroepitaxial growth such as molecular-beam epitaxy[8] will provide more improved films that will exhibit less degradation of the superconductivity at the limit thickness of the electric-field penetration-length level. It is preferable that the insulator, separating the superconductor from the voltage-applied metal, has a high dielectric constant, which results in the large induced charging. A candidate of the gate insulator is strontium titanate, $SrTiO_3$. By using a heterostructure of $YBa_2Cu_3O_x$ and $SrTiO_3$, field-effect-transistor structures were made and preliminary results were obtained.[9-11] Mannhart *et al.*[9] obtained the change of 50% supercurrent and a 24% change of the normal resistance by the application of about 2×10^5 V/cm in the insulator. Xi *et al.*[10] also showed a similar amount of modification of the resistance.

Recent experimental data of the Bi-Sr-Ca-Cu-O system (most typically $Bi_2Sr_2CaCu_2O_8$) showed strong anisotropic properties between the directions parallel to the c axis and perpendicular to it. Kleiner *et al.*[12] indicated by a current-voltage measurement along the c axis that $Bi_2Sr_2CaCu_2O_8$ was a natural superconductor-insulator superlattice, where two adjacent superconducting layers were coupled by the Josephson effect. An experiment by a scanning tunneling microscope showed that the CuO_2 layer was conductive and the Bi_2O_2 layer was insulating.[13] A possible model of $Bi_2Sr_2CaCu_2O_8$ is that a CuO_2 double layer with a Ca layer of 3-Å total thickness is a superconductor, while the remaining 12-Å-thick $Bi_2Sr_2O_4$ layer is an insulator. Thus a clear boundary may exist between the 3-Å superconducting layer and the 12-Å insulating layer. If the superlattice fabrication is finished when the surface is the insulating layer, the superconducting layer closest to the surface is expected to have much less degradation of its superconductivity because of the clearness of the boundaries. In a practical sense, the study of electric-field effects to the Bi-Sr-Ca-Cu-O is interesting at a limit of an ultrathin superconducting layer, and this may be a good probe investigating fundamental properties, e.g., two-dimensionality of the system and evaluations of the dielectric properties.

Section II presents the theory describing the electric-field effects to a diode where a superlattice is covered by an insulator and a gate-metal electrode. The model may be fairly simplified but general. Section III discusses numerical examples using the parameters that the Bi compound-$SrTiO_3$ heterostructure system has. The theory can predict how and how much electric fields penetrate in the system, and the relationship between the

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capacitance (or the reciprocal of it) and the applied voltage. Jumps of the capacitance occur as a function of the voltage. This is evidence of the two-dimensionality of the system. Comparison of this to future experiments is possible and important. Furthermore, the condition of superconductor-insulator transitions in a transistorlike operation is shown.

II. THEORY

Let us consider a layered superlattice on which an insulator and a gate-metal electrode are successively formed. The structure is drawn schematically in Fig. 1(a). In the superlattice, metal M layers and insulator I layers are alternately stacked. Here the metal M may in some case be a superconductor and it is so thin that the conduction in the layer is two dimensional: In the superlattice the presence of carriers (electrons or holes) along the direction perpendicular to the plane [x direction in
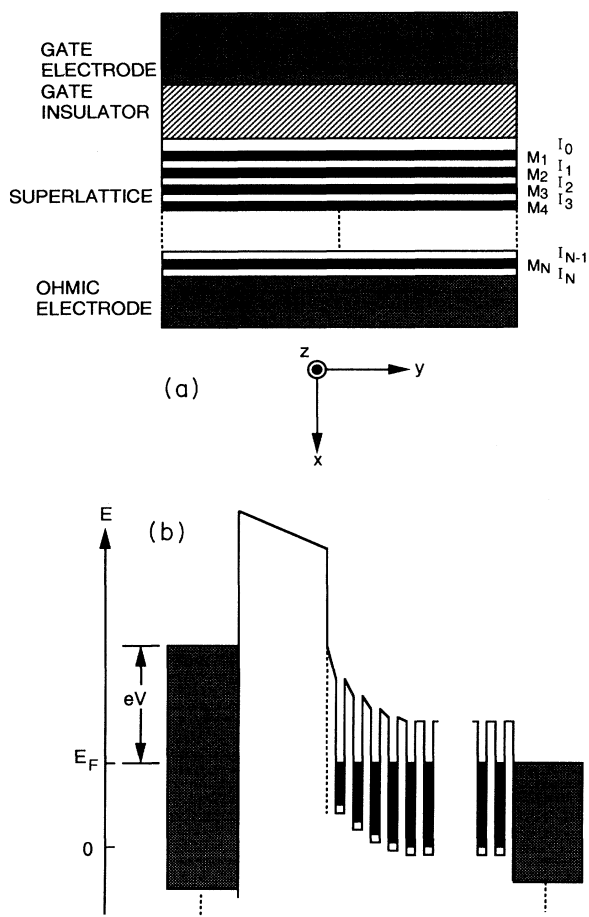

(a)

(b)

FIG. 1. (a) Diagram of a metal-insulator-superlattice diode. The superlattice consists of alternately stacked metal and insulating layers. The conduction is two-dimensional in the metal layers, and the carrier tunneling occurs between two adjacent metal layers. At the other side of the superlattice an electrode is put for the Ohmic contact. (b) Schematic diagram of the energy band when voltage V is applied to the metal gate.

Fig. 1(a)] is confined to the metal layers, but the carriers behave like free particles with mass m and electric charge $+e$ or $-e$ in the plane (y and z directions). By solving the corresponding Schrödinger equation, the energies of the carriers are quantized to the x direction, and the density of states is represented by a step function.[14]

The insulator I in the superlattice is also thin enough so that carriers between two adjacent metal layers can move back and forth by the quantum-mechanical tunneling. The lower potential barrier height gives the higher tunneling probability between two metal layers. The splittings of the quantized energy levels that occur by this tunneling are assumed to be so small that they can be ignored.

Among the quantized states, only the lowest one E_0 is taken into account,[15] and we choose the zero energy level in this lowest level, i.e., $E_0 = 0$. Then at the 0-K temperature, the carrier density per unit area at a layered metal is proportional to the Fermi energy E_F:[14]

$$n_s = \frac{m}{\pi\hbar^2}E_F .$$ (1)

The circumstance investigated here is that the thermal energy kT is much less than E_F. So, Eq. (1) can be used. For simplicity, let us assume that the metal layers in the superlattice have carriers with plus polarity (holes). If carriers have minus polarity (electrons), the following discussions are perfectly similar except for proper changes of the polarities. A voltage V is applied to the gate metal, while the backside of the superlattice directly contacts to some metal electrode and at this contact the current flowing obeys the Ohmic law.

By application of a gate voltage, carrier rearrangement in the superlattice takes place. If $V > 0$, some amount of holes at the surface side is expelled, by which minus charge of the background lattice appears. The diagram of the energy band is shown in Fig. 1(b). At $V \neq 0$, the electric potential φ_i is different among the metal layers, where the suffix i corresponds to the ith metal layer as shown in Fig. 1(a). Since the mechanism of inducing charge is ascribed to the carrier moving, and since the layers considered are very thin, the potential is assumed to be constant inside the metal layers. The induced charge density in the ith metal layer is defined as Q_i.

Inside the insulating layers in the superlattice, there is no electric charge, except for the negligible penetration components of the wave functions of holes. The potential obeys the one-dimensional Laplace equation, and thus the x component of the electric field $E_{i+1,i}$ inside the insulator I_i between the ith and $(i+1)$th metal layers is constant. Using the potentials φ_i, φ_{i+1} at the metal, the electric field is expressed as

$$E_{i+1,i} = \frac{\varphi_i - \varphi_{i+1}}{d_b}, \quad \text{for } i \geq 1 ,$$ (2)

where d_b is the thickness of the insulating layer in the superlattice.

Let us mention, in particular, the structure between the gate metal and the topmost metal layer M_1 in the superlattice. In our model, the material of the insulator isolat-

ing the conduction between the gate metal and the super-lattice (hereafter called the *gate insulator*) is different from that of the insulating layers in the superlattice. Furthermore, we assume that there is an insulating layer I_0 [as shown in Fig. 1(a)] between the gate insulator and the metal layer M_1. This makes the present model more realistic because, in some cases, this layer works as the carrier supplier for the adjacent metal layer.[16] Let the dielectric constant and the thickness of this layer be generally different from those of the insulating layers in the superlattice.

The electric displacement is constant and the same in the gate insulator and the first insulating layer I_0. Thus using the voltage V and the potential φ_1 of the first metal layer M_1, the electric field E_s in the layer I_0 is given by

$$E_s = \frac{\epsilon_i}{\epsilon_s d_i + \epsilon_i d_s}(V - \varphi_1) \ , \tag{3}$$

where ϵ_i and ϵ_s are the dielectric constants of the gate insulator and the insulating layer I_0, respectively, and d_i and d_s are their thicknesses, respectively.

The divergence of the electric displacement is equal to the electric charge density. In the superlattice the electric charging appears as the form of the induced charge densities Q_1, Q_2—at the two-dimensional metal layers M_1, M_2—and in the gate metal Q appears at the gate-insulator side interface. Thus Eqs. (2) and (3) can be changed to formulas showing the relationships between the induced charge densities and the potentials:

$$C_b(\varphi_1 - \varphi_2) - C_g(V - \varphi_1) = Q_1 \ , \tag{4}$$

$$C_b(-\varphi_{i-1} + 2\varphi_i - \varphi_{i+1}) = Q_i, \quad (i \geq 2) \ , \tag{5}$$

with

$$C_b = \frac{\epsilon_b}{d_b} \ , \tag{6}$$

and

$$C_g = \frac{\epsilon_i \epsilon_s}{\epsilon_s d_i + \epsilon_i d_s} \ , \tag{7}$$

where the expression of C_b is the same as that of the capacitance when an insulating layer with ϵ_b and d_b is sandwiched by two thick metal plates, and C_g is the same as that of the capacitance when two stacked insulators having ϵ_i and d_i, and ϵ_s and d_s, are sandwiched by thick metal plates.

The charge density Q induced at the gate electrode is

$$Q = C_g(V - \varphi_1) \ . \tag{8}$$

Induced charge densities at the metal layers in the superlattice are a function of their potentials. From Eq. (3) and the density of states of the step function shape, they are expressed as two different equations, depending on whether the potential energy is larger or smaller than the Fermi energy:

$$Q_i = -\frac{me^2}{\pi \hbar^2}\varphi_i, \quad \text{for } e\varphi_i \leq E_F \ , \tag{9a}$$

$$Q_i = -\frac{me}{\pi \hbar^2}E_F, \quad \text{for } e\varphi_i > E_F \ . \tag{9b}$$

Equation (9a) is used when the carriers remain in the metal layer M_i, while Eq. (9b) is used when the carriers in the layer are fully expelled. The latter case is called a *depletion condition* hereafter.

A method for obtaining the Ohmic contact at the other side of the superlattice is to put a conventional metal as shown in Figs. 1(a) and 1(b). Let the superlattice have N metal layers. The electric potential in the Ohmic metal is defined as zero. The charge density Q_{N+1} induced at the interface contacting to the superlattice side is related to the potential of the Nth metal layer (M_N) by

$$Q_{N+1} = -C_b\varphi_N \ , \tag{10}$$

where the barrier insulator between M_N and the metal electrode is simply assumed to have the same thickness and dielectric constant as the insulating layers in the superlattice. Note that the physically important side is the side close to the gate insulator. So the choice of the properties of this last insulating layer does not give a significant difference in the results. The induced charge density at the Nth layer is expressed as

$$C_b(-\varphi_{N-1} + 2\varphi_N) = Q_N \ . \tag{11}$$

From Eqs. (4), (5), (8), (10), and (11),

$$Q + \sum_{i=1}^{N+1} Q_i = 0 \tag{12}$$

is obtained. This means that the whole induced charge of the system is zero.

Now we can analyze the electric-field effects to the diode of the present model: Combining Eqs. (4), (5), and (11) together with Eq. (9) provides coupled linear equations to solve a set of φ_i, $(1 \leq i \leq N)$. Note that, depending on the condition of V, the coupled equations are different, because the potential at each metal layer may have two different cases of Eqs. (9a) and (9b). After getting the solution of φ_i, all induced charge densities $Q, Q_1, \ldots, Q_{N+1}$ can be obtained from Eqs. (4), (5), (8), (10), and (11).

III. NUMERICAL EXAMPLES AND DISCUSSION

Let us consider an oxide superconductor, $Bi_2Sr_2CaCu_2O_3$, whose layered crystal structure is sketched in Fig. 2. Its physical properties are strongly anisotropic between the directions parallel to the c axis and perpendicular to it. The current flowing in the ab plane is much larger than that along the c axis. Recent experimental data[12,13] support that CuO_2 planes are the conductive planes which give large supercurrent density, and the tunneling between CuO_2 planes of two adjacent half unit cells is the mechanism of the conduction along the c axis. Below the superconducting transition temperature, this gives Josephson-coupled supercurrent of low current density.[12] Above it, semiconductorlike temperature dependence of the resistance was reported.[17] Thus we can assume that $Bi_2Sr_2CaCu_2O_8$ naturally has the nature of the superlattice, which may fit to our model. A
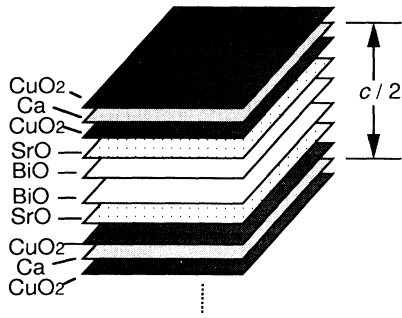
FIG. 2. Layered crystal structure of $Bi_2Sr_2CaCu_2O_8$ super-conductor. Half of the characteristic length along the c axis of the unit cell is shown in the figure. The $c/2$ length becomes the minimum period for the atomically controlled film preparation and for describing electric properties as in the text.

set of the double CuO_2 layers with the Ca layer having total thickness of about 3 Å is interpreted as the metal layer M_i of our model. The remaining part of the half unit cell which is made by $Bi_2Sr_2O_4$ may be an insulating layer of 12 Å in thickness in which the quantum-mechanical tunneling is possible. The carrier density experimentally obtained[18,19] is around 10^{21} cm^{-3}. Here a typical value of 1×10^{21} cm^{-3} is used. In the present model the carriers are confined to the metal layers, so the carrier density can be converted to the sheet carrier density of

$$n_s = (d_s + d_i) \times 10^{21} = 1.5 \times 10^{14} \text{ cm}^{-2} .$$

The mass for the ab plane in oxide superconductors evaluated from the muon-spin-resonance measurement is not far from the free-electron mass.[20] Here $m = 3m_0$ is used where $m_0 = 9.11 \times 10^{-31}$ kg is the free-electron mass. From Eq. (1), $E_F = 0.12$ eV is obtained. The dielectric constant of the insulating layer, $Bi_2Sr_2O_4$, has not been known. So we set it to be $30\epsilon_0$. (In Ref. 21 we can find that Bi_2O_3 has about $40\epsilon_0$ at the room temperature.)

One of the candidates of the gate insulator is the strontium titanate, $SrTiO_3$, because of its large dielectric constant. To get a large response for the application of a voltage to the gate electrode, material with a large dielectric constant is preferable. The dielectric constant of $SrTiO_3$ depends strongly on the temperature and the quality.[22,23] Here $\epsilon_i = 10\,000\epsilon_0$,[22] and $d_i = 200$ Å are used. The kind of the gate metal is not explicitly decided. Large carrier density and large Fermi energy are implicitly necessary. Conventionally used metals, e.g., Au or Ag fulfill these conditions. It is assumed that there is no band bending at the nonbias condition. Even if there is a band bending caused by the work function difference between the gate metal and the superlattice, it can be compensated by applying a dc voltage. Let the insulating layer I_0 have the same thickness and dielectric constant as those of the insulating layers I_i ($i > 1$) in the superlattice. Before numerical calculations, the parameters to be used are summarized here; $\epsilon_i = 10\,000\epsilon_0$, $\epsilon_s = \epsilon_b = 30\epsilon_0$, $d_i = 200$ Å, $d_s = d_b = 12$ Å, $m = 3m_0$, $E_F = 0.12$ eV, and $n_s = 1.5 \times 10^{14}$ cm^{-2}.

Potentials at the metal layers were obtained by solving the coupled linear equations (4), (5), (9), and (11). The number of the depletion layers increases with the increase of the applied voltage V. Our computation program can select the proper cases in Eqs. (9a) or (9b) with the change of V. Inside the insulating layer, the electric field is constant and the potential is obtained by linearly connecting the potential of the metal layers of both sides. Figure 3 shows the potentials as a function of depth of the super-lattice. The number labeled in each curve is the applied gate voltage. The flat parts in the curves indicate the constant potential in the metal layers. Between them the potential changes linearly. The electric field in the gate insulator is 7.5×10^4 V/cm at $V = 6$ V, which is still smaller than the breakdown voltage of $SrTiO_3$.[9,10]

Figure 4 shows the dependence of the potentials at the metal layers upon the gate voltage. The curves labeled M_1, M_2, and M_3 represent the potentials of the metal layers M_1, M_2, and M_3, respectively. Let us look at the result of the first layer (curve M_1). The potential changes sensitively if it exceeds about 0.12 eV. Since the Fermi energy is 0.12 eV, this value corresponds to the boundary of the depletion or nondepletion condition. This result reveals that after the depletion condition the electric field penetrates toward the neighboring layer much more easily than before the depletion condition. In other words, on a nondepletion condition, the induced charge density increases with the increase of V. This weakens the increasing rate of the electric-field penetration further inside the superlattice.

Figure 4 also reveals the gate voltages providing the boundaries between the depletion and nondepletion conditions. They are 1.3 V for the first layer (M_1), and 3.7 V for the second layer (M_2). Note that these are sensitive to the dielectric constants of the insulating layers, I_0 and I_1 as well as the gate insulator, whose details will be discussed elsewhere. Figure 5 shows a three-terminal field-effect transistor. In this structure the conduction channel of the superlattice is expected to be conductive or non-
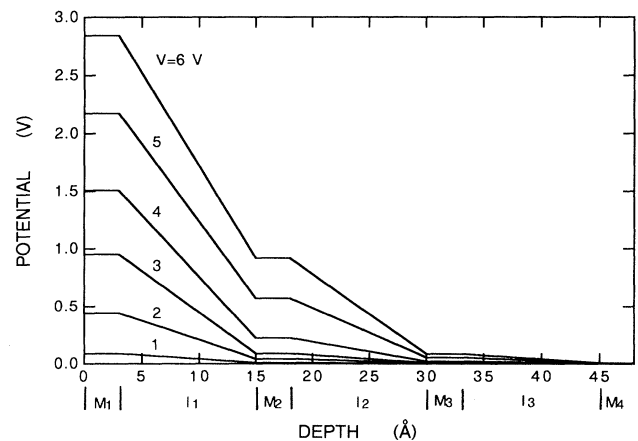
FIG. 3. Potential as a function of the depth measured from the surface in the superlattice. The number denoted in each curve indicates the applied voltage. The boundaries of the metal and insulating layers are marked below the bottom axis.
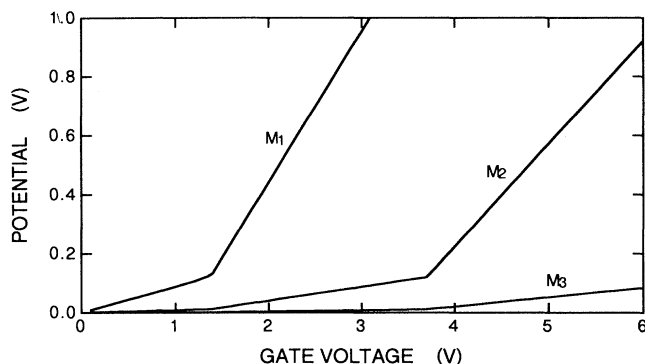
FIG. 4. Potential vs gate voltage in the metal layers M_1, M_2, and M_3.

conductive by depending on the gate voltage and the thickness of the superlattice. If the superlattice includes only one metal layer, the above-mentioned value, $V = 1.3$ V, is a measure of giving the nonconducting condition, and if it includes two metal layers, $V = 3.7$ V is the same measure. Note that in such cases the carriers move back and forth between the source and drain electrodes and the channel. Thus the analytical treatment is no more one dimensional, but in any case the above-mentioned values give good measures of the boundary of the conduction and nonconduction.

Induced charge density can be calculated from Eqs. (4), (5), and (8). The induced charge density at the gate electrode Q is shown in the solid curve in Fig. 6 as a function of V. The intersections of a few different gradients in the curve again correspond to the boundaries of the carrier depletion condition of the metal layers. The differentiation of the solid curve in Fig. 6 with respect to V provides a capacitance C ($=dQ/dV$). This is experimentally measurable. When a small ac voltage with a dc component, $V = V_{dc} + a \sin(2\pi f t)$, is applied, C can be measured as a function of the dc bias, using conventional ac capacitance or impedance meters.

The relationship between $1/C$ and V is shown in the dot curve in Fig. 6. We find the singularity of the curve, i.e., $1/C$ changes steplike with the dc voltage. This occurs with the changes of the number of the depletion layers. This originates from the present model where the superlattice is alternately stacked by the metal layers and the insulating layers. From Eq. (8), $C = C_g(1 - d\varphi_1/dV)$.
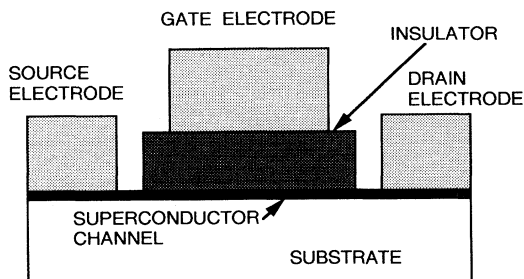

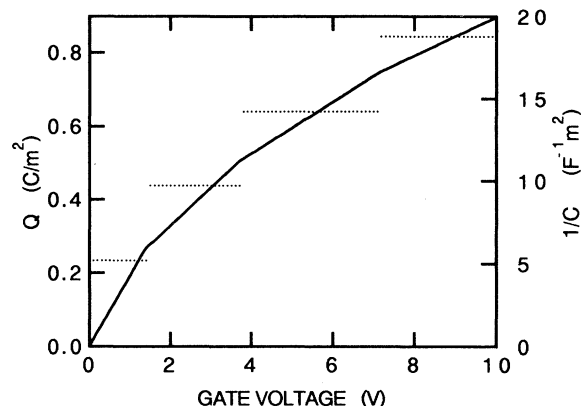FIG. 5. Structure of an electric-field-effect transistor.

FIG. 6. *Solid curve*: Induced charge density at the gate electrode as a function of the applied gate voltage. *Dot curve*: $1/C$ vs V. Jumps appear with the variation of the depletion layer number.

Thus C changes linearly with $d\varphi_1/dV$. In the coupled equations to solve a set of φ_i, the voltage V appears only in Eq. (4) as a linear term. So differentiating these coupled equations with respect to V provides a set of linear equations of $d\varphi_i/dV$ in which V is not included. Thus $d\varphi_1/dV$ is constant at each step, meaning that the curve in a step is perfectly flat. When the carriers in all metal layers are depleted fully, C is given exactly by the relation $1/C = 1/C_g + N/C_b$. This may be intuitively understood by an analogy from the series connection of a gate insulator and N insulating layers. Note that the amount of the step height change between two neighboring steps is not generally equal to the reciprocal of the insulating layer capacitance, $1/C_b$. However, if the ratio of the coefficient in Eq. (9a) to Eq. (6), $\beta \equiv (me^2/\pi \hbar^2)(d_b/\epsilon_b)$, is much larger than 1, it is proved that these jumps approach $1/C_b$. In fact, in the case of Fig. 6, β is about 11, and the appearing jumps are very close to $1/C_b$. If such a result is obtained experimentally for a metal-insulator-$Bi_2Sr_2CaCu_2O_8$ superconductor system, this will be a strong and clear evidence that the oxide superconductor, $Bi_2Sr_2CaCu_2O_8$, is a good model of the superlattice with the structure like Fig. 1(a). Furthermore, it is interesting to estimate $1/C_b = d_b/\epsilon_b$, because this is a significant physical quantity of the oxide superconductor $Bi_2Sr_2CaCu_2O_8$.

One interesting thing is whether or not we can get the depletion condition for any real systems of insulator-oxide-superconductor three-terminal devices. This is significant for the check of the present model as well as for device applications. Recent experiments for the system $SrTiO_3$-$YBa_2Cu_3O_x$ showed electric-field effects. $YBa_2Cu_3O_x$ is believed to be a three-dimensional material expressed by an anisotropic effective-mass tensor.[24] In this sense, it is not always a suitable example of the model, but similar carrier depletion properties may be expected. Mannhart et al.[9] made a three-terminal structure in which the $YBa_2Cu_3O_x$ layer was sputter-deposited and 4–10-nm thick. By application of 10-V gate voltage, corresponding to about 2×10^5 V/cm electric field in the

gate insulator, the modification of 50% supercurrent and a 24% change of the normal resistance were obtained. Xi et al.[10] made a similar structure where the $YBa_2Cu_3O_x$ was deposited by pulsed laser ablation technique. For a 2.4-nm thick $YBa_2Cu_3O_x$ sample, a 15% normal resistance change by application of 20-V gate voltage (5×10^5 V/cm electric field in the gate insulator) was obtained. In both cases, however, metal (or superconductor)-insulator transitions by the complete depletion of the metal layers were not observed. One of the probable reasons is that the deposited superconductor $YBa_2Cu_3O_x$ had still inevitable roughness in spite of using well-established technology, and another is the possibility of the presence of surface states at the insulator-superlattice interface. These diminish the effect of the voltage application. Sample fabrication by using the most careful technology about the epitaxy is important and necessary.

IV. CONCLUSIONS

A theory for describing electric-field effects to a metal-insulator-superlattice diode was presented. Here the superlattice consists of alternately stacked metal and insulating layers. By this, the penetration of the electric field and potential into the superlattice, and the induced charge density in the diode can be estimated. For a diode where the superlattice was an oxide superconductor $Bi_2Sr_2CaCu_2O_8$ and the insulator was $SrTiO_3$, numerical calculations were performed. The penetration length was several tens of Å. The applied voltage conditions, providing the states where the carriers in the topmost metal layer were fully depleted, were in an experimentally desirable range (less than 2 V), although they have not yet been confirmed by experiments. From the obtained induced charge density, the capacitance of the diode was evaluated. Jumps appeared in the relationship between the reciprocal of the capacitance and the gate voltage. This is ascribed to the fact that the number of the carrier depletion layers in the superlattice increases step by step. Quantitatively the jumps are closely related to d_b/ϵ_b, the thickness and dielectric constant ratio of the insulating layer in the superlattice. Thus, if such jumps are obtained experimentally for the system using $Bi_2Sr_2CaCu_2O_8$, it will be an evidence of the two-dimensionality of this superconductor, and a good probe to evaluate d_b/ϵ_b.

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