Structure and local dipole of Si interface layers in AlAs-GaAs heterostructures

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AlAs-Si-GaAs(001) and GaAs-Si-AlAs(001) heterostructures were synthesized by molecular-beam epitaxy. Transmission electron microscopy and *in situ* x-ray photoemission spectroscopy, together with x-ray interference measurements of model GaAs-Si-GaAs(001) structures and Si-GaAs(001) superlattices, indicate that pseudomorphic Si layers can be grown at the interface for layer thickness $\leq 4-8$ monolayers with no detectable dislocation or twin formation. While the band offsets for isovalent AlAs-GaAs heterostructures follow the commutativity rule, the presence of Si at the interface is found to give rise to deviations from the rule as large as ± 0.4 eV. Such deviations are associated with a Si-induced local dipole that can be established with high reproducibility within the interface region.

I. INTRODUCTION

Recent theoretical and experimental results on the electronic structure of semiconductor heterostructures and superlattices are highlighting the role of local interface dipoles in determining heterojunction band discontinuities. Andersen and co-workers,[1] based on linear-muffin-tin-orbital superlattice calculations, proposed that the correct heterojunction potential alignment can be obtained starting from an arbitrary alignment of the bulk potentials and minimizing the total energy with respect to a single parameter: the local interface dipole. The argument used to prove this result is based on linear-response theory,[2] although it can be generalized beyond linear response.[1] In this view, models of the heterojunction band offsets based on the alignment of "absolute" reference levels for the two semiconductors, such as the charge neutrality level,[3-8] the atom superposition,[9,10] or the cation-centered Wigner-Seitz cell model,[11] should be considered only as a zeroth-order approximation.

Recent linear-response-theory results treating the interface as a perturbation relative to a reference virtual crystal[2] indicate that at isovalent lattice-matched heterojunctions the band offsets should depend only on the bulk properties of the two semiconductor constituents, while polar interfaces between heterovalent heterojunctions may be charged,[2] and the interface charge gives rise to electric fields that alter the bulk energy of the system.[2] The possible formation of charged heterovalent interfaces, discussed earlier by several authors,[12-14] has recently been examined for IV/III-V heterojunctions and superlattices through a number of first-principles total-energy calculations.[15-18]

Baroni *et al.*,[2] and Muñoz, Chetty, and Martin,[15] and Peressi *et al.*[18] predicted large violations of the transitivity rule for GaAs-Ge-GaAs,[2,15] Ge-GaAs-Ge,[2] and AlAs-Si-GaAs (Ref. 18) structures in which the central region is comprised of a pseudomorphic atomic double layer playing the role of an n^+-p^+ microscopic capacitor and generating a large interface dipole.[19] Some of these predictions have been qualitatively confirmed,[20-22] although the magnitude of the deviation from the transitivity rule and its dependence on interface layer thickness and composition are not well reproduced by the theory.

The magnitude of the dipole can be substantially affected by the formation of defects at the interface. For example, Bylander and Kleinman[16] have calculated electrostatic fields of about 10^9 V/m as a result of the interface charge in Ge-GaAs (001)- and (111)-oriented superlattices, but Baroni *et al.*[2] suggested that in the same system neutral interfaces might be induced by the formation of mixed Ga/Ge or As/Ge planes. Dandrea, Froyen, and Zunger[17] proposed that the large fields in Si-GaAs(001) superlattices will be compensated by III/IV (cation) or V/IV (anion) swaps across the (001) interface, leading to neutral interfaces with widely different band offsets. At present, the magnitude of the interface dipole and the nature of the defects, if any, that are formed in such systems are a priority target of experimental investigations.

In this paper we focus on the stability of thin strained layers of Si within the interface region of AlAs-GaAs heterostructures, and on the local electrostatic dipole associated with the resulting interface. As far as IV/III-V device applications are concerned, the possibility to obtain large changes in band offsets using local interface dipoles would open a new way of tailoring carrier injection or confinement in heterojunction devices.[23] In addition,

other possible applications include GaAs/Ge/GaAs double heterojunction bipolar transistors,[24] Si layers in the interface region of SiO_2-GaAs junctions to reduce interface state densities,[25,26] and Fermi-level pinning,[25–27] and Si layers in the interface region of GaAs-metal junctions to unpin the Fermi level and modulate the Schottky barrier.[28–30]

In a previous Rapid Communication[20] we have shown that the presence of thin layers of Si in the interface region of AlAs-GaAs interfaces is associated with a local dipole that can change the band offsets. Here we expand on this initial report and address three main issues. First, we consider the natural (i.e., unmodified) value of the band offsets in AlAs-GaAs(001) and GaAs-AlAs(001) isovalent heterostructures by examining 49 heterostructures synthesized by molecular-beam epitaxy (MBE) with different types of doping for the two semiconductors. *In situ* monochromatic x-ray photoemission spectroscopy (XPS) studies show no evidence of deviations from the commutativity rule, but reveal a possible systematic discrepancy of 0.10 eV in the band offsets relative to recent optical results.

Secondly, we characterize by means of transmission-electron-microscopy (TEM) or x-ray-diffraction (XRD) measurements the structure of Si layers in AlAs-GaAs heterojunctions, GaAs-GaAs homojunctions, and Si-GaAs(001) superlattices. We find that pseudomorphic Si interface layers with no evidence of twins or dislocations can be fabricated for layer thicknesses as large as 4–8 monolayers (ML's) both in single-quantum-well structures and superlattices, using a combination of low-temperature and high-rate-growth conditions.

Finally, we gauge by XPS the value of the valence-band offset, its reproducibility, and the interface position of the Fermi level for 50 AlAs-Si-GaAs(001) and 30 GaAs-Si-AlAs(001) heterostructures for different values of the Si interface layer thickness and doping of the III-V substrate and overlayer. We find that the Si-induced local dipole yields maximum deviations from the transitivity rule of ± 0.4 eV, i.e., 27% of the theoretical value,[18] at a Si coverage of 0.5 ML. Although the interface position of the Fermi level varies from heterostructure to heterostructure and is affected by the growth conditions and doping, the reproducibility of the maximum local dipole is better than 15% for AlAs-Si-GaAs(001) and better than 10% for GaAs-Si-AlAs(001). For Si interface layer thicknesses of 2 ML's the dipole decreases, and the reproducibility markedly degrades, suggesting that an increasing number of anion or cation swaps may take place in order to reduce the local electrostatic field at the interface. For larger Si layer thicknesses (2–4 ML's) constant deviations from the transitivity rules and asymmetries in the behavior of AlAs-Si-GaAs(001) and GaAs-Si-AlAs(001) may be related to the establishment of inequivalent neutral IV/III-V and III-V/IV interfaces rather than the long-range electrostatic fields expected for charged interfaces.

II. EXPERIMENTAL DETAILS

Heterostructures and superlattices were synthesized by conventional solid source MBE in a multichamber facility that includes a Riber 32P growth chamber for the growth of III-V and IV semiconductors, and an analysis chamber equipped with a Surface Science Laboratories SSX-100-03 small spot monochromatic XPS spectrometer. All chambers are connected by an ultrahigh vacuum (UHV) transfer line that also allows fast introduction of wafers from a class 100 custom-modified clean room, and wafer heating prior to MBE growth.

Heterostructures and superlattices were grown on undoped GaAs(001) wavers etched in a $5NH_4OH{:}2H_2O_2{:}10H_2O$ solution, heated at 300 °C in the UHV heating station and then at 580 °C in the MBE growth chamber to remove the oxide. Heterostructures for XPS measurements were comprised of a III-V substrate layer (GaAs or AlAs) grown epitaxially on the GaAs(001) wafer, a Si interface layer of variable thickness, and a thin (10-30-Å thick) III-V overlayer (AlAs or GaAs) grown epitaxially on top of the Si interlayer. GaAs(001) substrate layers were typically 0.5-μm-thick buffer layers grown at 580 °C with an As partial pressure of 4×10^{-6} Torr and an As_4/Ga flux ratio of 10-15. The growth rate was calibrated by means of reflection high-energy electron diffraction (RHEED) intensity oscillations. Typical GaAs growth rates employed were in the 1-μm/h range. The GaAs(001) surfaces examined by RHEED exhibited the As-stabilized 2×4 surface reconstruction. AlAs(001) substrate layers were obtained as 200-1400-Å-thick epitaxial layers grown at 620 °C on GaAs buffers, and exhibited the As-stabilized 3×1 surface reconstruction.[31] We examined n-type (Si doped, $n=6\times10^{17}$ cm^{-3}), p-type (Be doped, $p=1\times10^{18}$ cm^{-3}), as well as undoped III-V layers. In what follows, the corresponding results will be specified as pertaining to n-, p-, or i-type substrates or overlayers.

Si interface layers were fabricated with two alternate procedures. In most cases, the growth of the substrate material was stopped by closing the group-III-element shutter and leaving the As shutter open, as customarily done during δ doping of GaAs. In selected cases both the As and Ga shutters were closed and the source power lowered in order to reduce the As partial pressure below 4×10^{-10} Torr. The substrate temperature was then lowered to 500 °C, and the shutter of the Si effusion cell opened for a calibrated time interval. The two Si deposition procedures (with and without As flux) yielded different Si surface reconstructions, as indicated by RHEED, but totally consistent XPS determinations of the band offsets. For example, upon Si deposition on GaAs(001) in the presence of As flux, we observed an intermediate 2×1 reconstruction (at a Si coverage of 0.1-0.2 ML) followed by a transition to a sharp 3×1 pattern.[32] Without As flux we observed an initial 2×1 reconstruction (Si coverages of 0.5-1.0 ML) followed by a 2×2 reconstruction at coverages above 6–8 ML's.[33] The different Si layer surface reconstruction had no detectable effect on the XPS value of the valence-band offset for the final structures.

Upon completion of the desired Si interlayer thickness, final AlAs-Si-GaAs(001) and GaAs-Si-AlAs(001) heterostructures for XPS band offset determination were obtained by closing the Si shutter, raising the substrate tem-

perature to 580 °C in about 2 min, and growing thin III-V overlayers by opening the appropriate shutters. Overlayers as thin as 10 Å and as thick as 30 Å were examined with consistent results, and the typical overlayer thickness employed for XPS measurements was 15 Å. The XPS spectrometer uses Al $K\alpha$ radiation (1486.6 eV) monochromatized and focused by a bent crystal monochromator. Photoelectrons are collected at an average exit angle of 55° from the sample normal and energy analyzed by means of a hemispherical electrostatic analyzer. An overall energy resolution (electrons plus photons) of 0.69 eV could be achieved for sampled areas 150 μm in diameter. The photoelectron escape depth for Ga $3d$ photoelectrons excited by Al $K\alpha$ radiation was estimated as 26.6 Å for normal emission in Ref. 34. Because of our collection geometry, the effective escape depth in our experiment was only 15 Å. The variation of the escape depth in going from Ga $3d$ to Al $2p$ photoelectrons is only a few percent and will be neglected here.[35]

Heterostructures for TEM cross-sectional analysis were obtained by growing a 0.5-μm-thick updoped GaAs substrate layer, a Si interlayer of variable thickness (nominal Si coverages of 0, 2, 4, 8, and 14 ML's with 1 ML defined as 6.25×10^{14} atoms/cm^2) deposited at 500 °C under As flux, a 100-Å-thick AlAs overlayer, and a final 100-Å-thick GaAs cap layer grown at 580 °C. After Si deposition, the total growth time to complete the heterostructure ranged from 2 to 8 min. Specimens were cut and prepared by conventional ion thinning. A Philips CM30 microscope operated at 300 kV was used for all TEM investigations, with cross sections imaged along the [110] direction.

GaAs-Si-GaAs(001) heterostructures for x-ray diffraction (XRD) analysis were obtained by growing a 2.5-μm-thick undoped GaAs buffer layer at 580 °C and depositing 1 and 2 nominal monolayers of Si under As flux at 500 °C, followed by 2500 Å of GaAs at 580 °C. After Si deposition, the total growth time to complete the structure was about 10 min. We also fabricated for comparison a 15-period $(Si)_3(GaAs)_{50}$ superlattice, with superlattice composition determined by XRD, in 5 h at 540 °C on GaAs. X-ray interference measurements were performed using a high-resolution double-crystal diffractometer and Cu $K\alpha_1$ radiation ($\lambda=1.540\,562$ Å). An x-ray beam incident on the sample with 11-μrad angular divergence was obtained using an asymmetric Ge(100) crystal and the (400) reflection.[36] The x-ray-diffraction patterns were recorded in all cases in the vicinity of the symmetric (400) GaAs reflection, which has an intrinsic full width at half maximum (FWHM) of 40 μrad, and, for the superlattice, also in the vicinity of the asymmetric (422) GaAs reflection.

Throughout the paper, nominal Si coverages are given in monolayers, in terms of the GaAs(001) atomic density. Nominal coverages were obtained from flux calibrations. We set a constant Si effusion cell temperature and used the constant Si flux to homogeneously dope GaAs layers. Resistivity and Hall mobility measurements at liquid-nitrogen temperature were used to determine the doping density. Flux calibration was performed for cell temperatures in the 1000–1160 °C range and yielded a linear dependence of the flux on cell temperature in the range explored. During the experiment Si deposition was performed with a cell temperature of 1240–1300 °C, and the nominal coverage was obtained by linearly extrapolating the flux measured at lower temperatures. The resulting estimated flux was $3.6\pm0.8\times10^{12}$ atoms/cm^{2}s at 1300 °C. The growth time required to complete 2 ML's of Si at 1300 °C was 5′ and 45″. For all silicon coverages ≥ 2 ML's the silicon cell was operated at 1300 °C. The Si thickness was checked *a posteriori* through XPS studies of Si growth on both GaAs(001) and AlAs(001) substrates, and XPS and flux-derived coverages were found to be consistent within an uncertainty of about 15% (Ref. 37). Growth of a 15-Å-thick III-V overlayer on top of the Si interlayer for XPS determination of the offset, was completed in 5–11 s. Correspondingly, photoemission showed little variation of the cation/Si integrated intensity ratio, suggesting that the Si interlayer thickness remains constant at least during such short growth times.[20]

III. RESULTS AND DISCUSSION

A. Natural AlAs-GaAs heterostructure band offsets

A number of recent photoemission results on the natural, unmodified band discontinuities for AlAs-GaAs exist in the literature. The valence-band offset ΔE_v is usually measured[38–42] from the position E_b of the Ga $3d$ and Al $2p$ core levels, the position of the valence-band maximum E_v in the two bulk materials, and the core-level separation at the interface $\Delta E_{\rm cl}$:

$$\begin{aligned}\Delta E_v &= [E_b(\text{Ga } 3d) - E_v(\text{GaAs})] \\ &\quad - [E_b(\text{Al } 2p) - E_v(\text{AlAs})] + \Delta E_{\rm cl} \\ &= \Delta E_{\rm cl} - \Delta E_b \ . \end{aligned} \tag{1}$$

The most recent photoemission results are summarized in Table I. In the first column we give the number of samples measured in each experiment, in the second column the overlayer-substrate growth sequence, in the third column the overlayer-substrate doping type, in the fourth column the interface core-level separation $\Delta E_{\rm cl}$, in the fifth column the difference in bulk core binding energies ΔE_b, and in the sixth column the valence-band offset ΔE_v. The values of ΔE_v in Table I are in the 0.36–0.46 eV range and reportedly carry an uncertainty of 50 meV. However, recent optical determinations of the valence-band offset[43,44] support a somewhat larger value of 0.56 eV. The issue is further complicated by the existence of different theoretical predictions. The most recent predictions for the offset from all electron calculations within the local-density approximation yielded values of 0.37 (Ref. 45), 0.41 (Ref. 46), and 0.48 eV (Ref. 2). Recent work on many-body corrections to the local-density approximation, however, indicate that the inclusion of such effect should modify the offset, and new corrected values of 0.53 (Ref. 46) and 0.58 eV (Ref. 2) have been proposed. In view of these possible discrepancies, and the relatively small number of samples examined to date by photoemis-

TABLE I. Literature results for the valence-band offset in AlAs-GaAs(001) and GaAs-AlAs(001) heterostructures. First column: number of samples examined. Second column: overlayer-substrate type. Third column: overlayer-substrate doping type. Fourth column: Al 2*p*-Ga 3*d* interface core-level separation. Fifth column: bulk core binding energy difference. Sixth column: valence-band offset. Last column: reference.

No. measured	Growth sequence	Doping	ΔE_{cl}	ΔE_b	ΔE_v	Ref.
4	AlAs-GaAs(001)		54.41	53.95	0.46	38
4	GaAs-AlAs(001)		54.31	53.95	0.36	38
3	GaAs-AlAs(001)		54.65	54.27	0.39	39
2	AlAs-GaAs(001)		54.65	54.27	0.39	39
2	AlAs-GaAs(001)	*n*/*n*	54.45	53.99	0.46	40
3	GaAs-AlAs(001)	*n*/*n*	54.43	53.99	0.44	40
2	AlAs-GaAs(001)	*i*/*n*	54.42	53.97	0.45	41
2	GaAs-AlAs(001)	−/*i*	54.42	53.97	0.45	41

sion (see Table I), we elected to conduct a new systematic study of the photoemission-determined value of the natural valence-band offset.

In photoemission, the uncertainty on the numerical value of the offset derives mostly from the uncertainty on the determination of the position of the valence-band maximum relative to the Fermi level for each bulk material. The position of E_v is usually determined either from a linear extrapolation of the leading valence-band edge[47] or through a least-squares fit of the data[42] to a suitably broadened theoretical electronic density of states (DOS) near E_v. The first method is in principle less accurate, although it is likely to be adequate for deriving the valence-band offset for common anion systems such as AlAs-GaAs due to the cancellation of systematic errors that follows from the similarity of the anion-derived DOS features. Most authors who use the second method[38,40] employ the same theoretical GaAs DOS to fit both GaAs and AlAs data, and therefore make an assumption equivalent to that implicit in the first method. In general, sources of uncertainty in the determination of E_v with the second method are related to matrix elements and surface-related effects, the accuracy of the theoretical DOS, as well as the numerical value of the broadening parameter.[48]

The interface core separation ΔE_{cl} can be measured with high accuracy, and is independent of overlayer and substrate doping if the sampling depth is negligible relative to the Debye lengths of the two semiconductors comprising the junction. It will also be independent of overlayer thickness if the overlayer is thick enough so that the contribution from the first layer atoms is negligible. The apparent core position reflects then the average "bulk" electrostatic potential of the overlayer rather than possible chemical shifts. One should, in principle, verify that such conditions are met. Variations in the apparent value of ΔE_{cl} with doping or overlayer thickness, as well as asymmetric broadening of the substrate or overlayer core-level line shapes, are expected if one or the other of the two conditions is not met.

Our results for the AlAs-GaAs core-level separation[49] are exemplified in Fig. 1 and summarized in the first row of Table II. In the rightmost inset of Fig. 1 we show

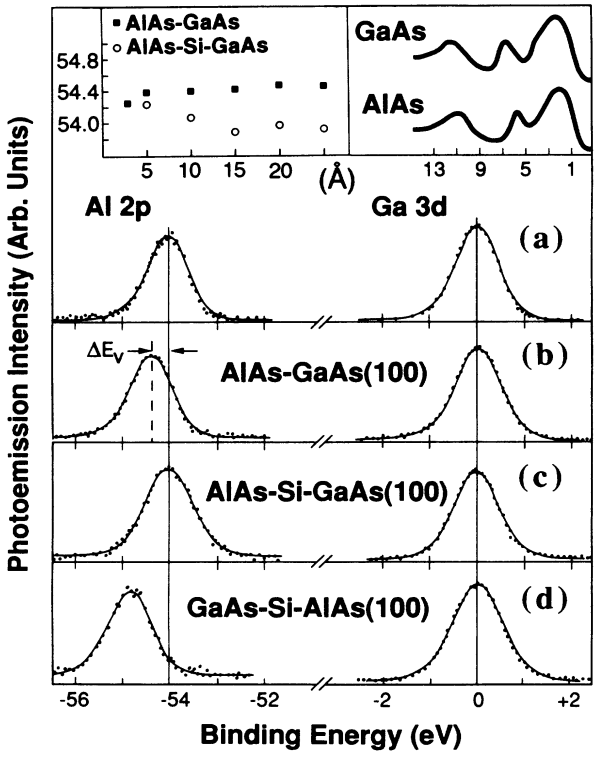

FIG. 1. Leftmost inset: Al 2*p*-Ga 3*d* core-level separation at the interface as a function of AlAs overlayer thickness for AlAs-GaAs(001) (squares) and AlAs-Si-GaAs(001) (circles). Rightmost inset: valence-band emission from thick AlAs(001) and GaAs(001) epitaxial layers. (a) Al 2*p* and Ga 3*d* core-level emission from bulk AlAs(001) and GaAs(001) samples. The zero of the energy scale was taken at the position of the Ga 3*d* cores in GaAs and the apparent core separation is that expected for a hypothetical heterojunction with zero valence-band offset (ΔE_b). (b) Al 2*p* and Ga 3*d* core emission from an actual AlAs-GaAs(001) heterostructure. (c) Al 2*p* and Ga 3*d* core-level emission from an AlAs-Si-GaAs(001) heterostrucutre with a Si layer 0.5 ML thick. (d) Al 2*p* and Ga 3*d* core-level emission from a GaAs-Si-AlAs(001) heterostructure with a Si layer 0.5 ML thick.

TABLE II. Core-level and valence-band offset measurements for different III-V/III-V and III-V/IV/III-V heterostructures. First column: sample type (overlayer-interlayer-substrate). Second column: number of heterostructures examined. Third column: overlayer-substrate doping types examined. Fourth column: range of positions observed for the Ga 3*d* core levels (Ref. 49) relative to the Fermi level E_F at the interface. Fifth column: range of positions observed for the Al 2*p* core level (Ref. 49) relative to E_F at the interface. Sixth column: average interface core level separation ΔE_{cl}. Seventh column: experimental uncerainty on ΔE_{cl}, taken as the standard deviation or $\frac{1}{2}$ of the dispersion of the experimental values (rows 7 and 8). Eighth column: resulting average values of the valence-band offset ΔE_v. Epitaxial III-V substrates and overlayers were all grown at 580 °C, and the typical thickness of the III-V overlayers was 15 Å. The pseudomorphic Si interlayers were all grown at 500 °C.

Sample	No. measured	Doping	E(Ga 3*d*)	E(Al 2*p*)	ΔE_{cl}	σ	ΔE_v
AlAs-GaAs	40	*p*/*p*,*n*/*n* *n*/*p*,*p*/*i* *n*/*i*,*i*/*i* *i*/*n*	18.97–19.69	73.37–74.10	54.42	0.04	0.42
GaAs-AlAs	9	*i*/*i*	18.99–19.59	73.29–74.15	54.46	0.03	0.46
AlAs-0.5 ML Si-GaAs	41	*p*/*p*,*n*/*n* *n*/*p*,*p*/*i* *n*/*i*,*i*/*i* *i*/*n*,*i*/*p* *p*/*n*	19.56–20.22	73.64–74.22	54.02	0.05	0.02
GaAs-0.5 ML Si-AlAs	10	*i*/*p*,*i*/*i*	18.92–19.50	73.70–74.47	54.77	0.03	0.77
AlAs-2 ML Si-GaAs	7	*i*/*i*	19.23–20.09	73.72–74.19	54.23	0.15	0.23
GaAs-2 ML Si-AlAs	16	*i*/*i*	18.92–19.68	73.47–74.60	54.77	0.15	0.77
AlAs-4 ML Si-GaAs	2	*i*/*i*	19.79–19.85	74.11–74.12	54.30	0.03	0.30
GaAs-4 ML Si-AlAs	4	*i*/*i*	19.39–19.59	74.11–74.50	54.77	0.05	0.77

valence-band spectra for a 0.5-μm-thick GaAs epitaxial substrate (top) and a 200-Å-thick AlAs epitaxial layer (bottom). The binding energy scale is referenced to the valence-band maximum E_v as derived from a least-squares linear fit of the leading valence-band edge. Photoelectron energy distribution curves (EDC's) for the Al 2*p* and Ga 3*d* core emission from these two samples are shown below the inset in Fig. 1(a). The core binding energies were measured relative to E_v for each sample, and the zero of the energy scale was taken at the position of the Ga 3*d* centroid in GaAs. The corresponding core binding energy difference ΔE_b is that expected from a hypothetical heterojunction with zero valence-band offset.[50] In Fig. 1(b) we show core EDC's from an AlAs-GaAs(001) heterostructure fabricated by growing a 15-Å-thick AlAs overlayer at 580 °C on top of the GaAs substrate. The corresponding interface core-level separation ΔE_{cl} is 54.42±0.03 eV. The core separation is independent of overlayer thickness in the coverage range 10–25 Å. This is illustrated in the leftmost inset of Fig. 1, where we plot the Al 2*p*–Ga 3*d* core separation at the interface as a function of overlayer thickness for an AlAs-GaAs(001) heterostructure (squares).

In the first row of Table II we summarize measurements for 40 AlAs-GaAs(001) heterostructures fabricated by growing 15-Å-thick AlAs layers at 580 °C on top of GaAs(001) substrate layers. In the first column we give the sample type (overlayer-substrate), in the second column the number of heterostructures examined, in the third column the overlayer-substrate doping type examined, in the fourth column the range of measured positions of the Ga 3*d* core level[49] relative to the Fermi level at the interface, in the fifth column the measured position of the Al 2*p* core level relative to the Fermi level at the interface, in the sixth column the average interface core separation ΔE_{cl}, in the seventh column the corresponding uncertainty σ, obtained as the standard deviation of the distribution, and in the last column the resulting average value of the valence-band offset ΔE_v obtained by using previously measured core-level binding energies in bulk GaAs and AlAs standard materials ($\Delta E_b = 54.00 \pm 0.05$ eV, Ref. 50) and Eq. (1).

In the second row of Table II we summarize measurements for nine GaAs-AlAs(001) heterostructures fabricated by growing 15-Å-thick GaAs layers at 580 °C on top of AlAs(001) substrate layers. The meaning of the symbols is the same as in the first row of Table II. The average values of ΔE_{cl} for AlAs-GaAs(001) and GaAs-AlAs(001) heterostructures are 54.42±0.03 and 54.46±0.03 eV, respectively. The interface core separation ΔE_{cl} is therefore independent of the growth sequence, so that the valence-band offset ΔE_v for isovalent GaAs/AlAs heterostructures follows the commutativity rule within experimental uncertainty (0.05 eV). The values of the valence-band offsets 0.42±0.07 and 0.46±0.06 eV for AlAs-GaAs(001) and GaAs-AlAs(001), respectively, are in agreement with most of those listed in Table I, and indicate that there may indeed be a systematic discrepancy of up to 0.10 eV between the lower, photoemission-determined value of the offset and the value derived from optical studies. We tentatively associate the difference to the final state involved in the two processes. In principle, the effect of the core-hole potential on the photoemission electron states may modify such states relative to the ground state of the system and affect differently GaAs and AlAs derived states.[46]

From the apparent position of the Ga 3*d* and Al 2*p* core levels relative to the Fermi level, we can extract the

position of the Fermi level at the interface using the measured core binding energies relative to the valence-band maximum.[50] In general, we observe a wide (0.6-eV) scatter in the values of the interface position of the Fermi level (see Table II), which contrasts with the very limited scatter in the values of the interface core separation ΔE_{cl}. The position of the Fermi level at the interface is therefore likely to be strongly affected by small differences in the growth procedure, while the band offsets are quite insensitive to the same variations. This is in agreement with recent linear-response-theory results[2] that indicate that in isovalent heterostructures the band offsets are essentially a bulk property of the two semiconductors involved, and are largely independent of orientation, interdiffusion, and defect formation. The pinning position of the Fermi level at the interface is not, instead, a bulk property of the two materials, and may therefore be affected by the detail of the growth procedure. The Fermi-level pinning positions range from about 0.1 eV above the top of the valence band in GaAs (or about 0.6 eV above the top of the valence bands in AlAs) to about the midgap position in GaAs and AlAs, indicating that a wide range of defect concentrations or types may be generated for small variations in the growth parameters.

B. Structural properties of the Si interface layers

In Fig. 2 we show high-resolution cross-sectional TEM photographs of the interface region of AlAs-Si-GaAs(001) heterostructures for nominal Si interlayer thicknesses of 2, 4, and 8 ML's. Only limited contrast between the III-V and Si lattice could be achieved, but the pseudomorphic character of the interlayer is quite clear for coverages of 2 and 4 ML's, with no evidence of twins, or of the edge and 60° dislocations observed during GaAs growth on bulk Si(001) substrates.[51]

In the case of the sample with 8-ML Si interlayer thickness, the photograph unambiguously shows the presence of microtwins on the (111) planes, indicating that partial strain relaxation may have begun. Strain relaxation is exemplified in Fig. 3, where we show dark-field cross-sectional TEM, $\mathbf{g}=200$, photographs of AlAs-Si-GaAs(001) structures for nominal Si interlayer thickness of 2 (top) and 14 ML's (bottom). At the very top of each photograph, a dark horizontal feature corresponds to a GaAs cap layer used to protect the heterostructure during sample transfer and processing. The AlAs layer below appears bright due to the difference in the F_{200} structure factor for the two semiconductors.[52] The Si interface layer is located at the boundary between the AlAs layer and the GaAs buffer directly below. The results for the 2-ML Si interlayer show high-quality interfaces, with no evidence of dislocations, twins, antiphase domains, or stacking faults. Results for the 14-ML Si interlayer show clear

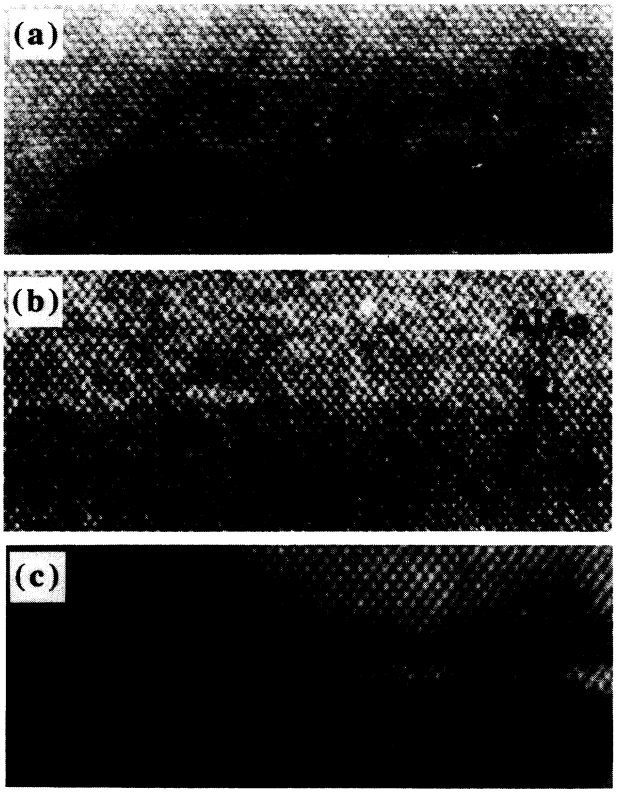

FIG. 2. High-resolution transmission-electron microscopy photographs [(110) cross section] of AlAs-Si-GaAs(001) heterostructures with a Si interface layer thickness of 2 (top), 4 (center), and 8 ML (bottom).

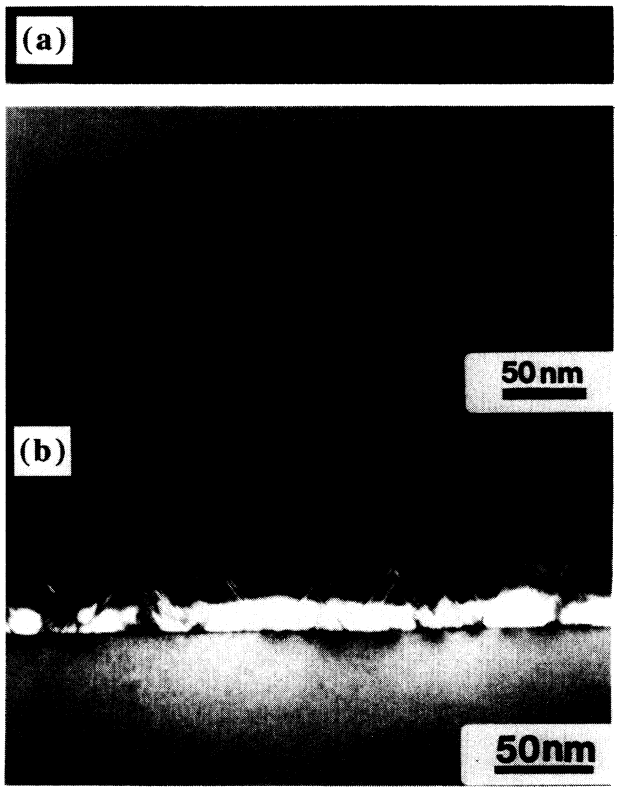

FIG. 3. Dark-field, $\mathbf{g}=200$, image [(110) cross section] of a GaAs-AlAs-Si-GaAs(001) heterostructure with a Si interface layer thickness of 2 (top) and 14 ML (bottom). The AlAs layer appears bright because of the difference in the F_{200} structure factor for the two semiconductors. The Si interface layer is located at the boundary of the AlAs layer and the GaAs buffer directly below.

evidence of dislocations and stacking faults in the AlAs layer, indicating strain relaxation of the Si layer. We are not aware of any previous microscopy study of AlAs-Si-GaAs(001) structures, but the results of Fig. 3 are qualitatively consistent with recent TEM studies of GaAs-Si-GaAs(001) heterostructures by Adomi *et al.*,[53] who have reported a 9-Å Si interface layer to be pseudomorphic, and an 18-Å interlayer to be at least partially relaxed.

A more quantitative analysis was performed for a number of GaAs-Si-GaAs test structures. In Fig. 4 we show x-ray-diffraction patterns recorded in the vicinity of the symmetric (400) GaAs reflection for samples involving Si interface layers with nominal thickness of 1 and 2 ML's [Figs. 4(a) and 4(b), respectively, solid circles) and GaAs overlayers about 2000 Å thick. Due to the different lattice constant of the Si and GaAs crystals, the Si unit cell in the samples is tetragonally distorted, so that the wave field scattered by the GaAs lattice planes in the overlayer is not exactly in phase with that scattered by the lattice planes of the GaAs substrate. The interference between the two waves gives rise to characteristic fringes in the x-ray-diffraction pattern, in which the intensity of the fringes depends strongly on the product of thickness and strain of the embedded Si layer, and the angular distance between the fringes depends on the thickness of the GaAs overlayer.[36] For Si pseudomorphic layers (+4.1% in-plane strain), the strain normal to the interface plane can be calculated from elastic theory as −3.07%, and it is therefore possible to determine the average thickness of the embedded Si layer and of the GaAs overlayer by comparing the experimental diffraction pattern and simulated patterns obtained from dynamical scattering theory for distorted crystals. We also show in Figs. 4(a) and 4(b) simulated interference patterns (solid line) from dynamical scattering theory.[36] The closest match was obtained in Fig. 4(a) for a Si interface layer thickness of 0.8 Å (0.6 ML) and a GaAs overlayer thickness of 1900 Å, and in Fig. 4(b) for a Si thickness of 2 Å (1.4 ML's) and a GaAs thickness of 2050 Å. We emphasize that no Debye-Waller broadening or smoothing was used in the comparisons of Fig. 4, so that the agreement between theory and experiment is especially significant and supports an abrupt and coherent nature of the interfaces and good crystalline quality of the overlayers.[54]

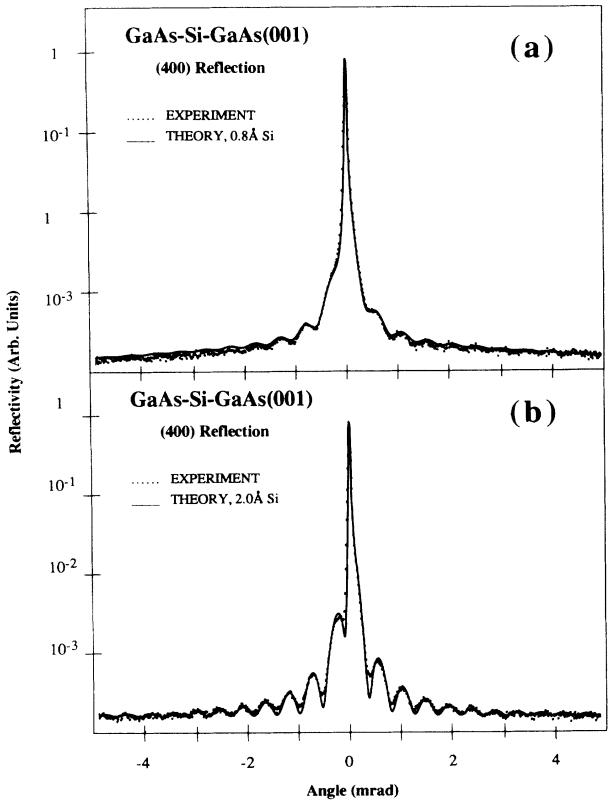

FIG. 4. Cu $K\alpha$ x-ray-diffraction patterns (closed circles) near the symmetric (400) GaAs reflection from GaAs-Si-GaAs(001) structures for nominal Si interlayer thicknesses of 1 (a) and 2 ML (b). We also show the result of a dynamical scattering simulation (solid line). Best agreement with experiment is found for a Si interface layer thickness of 0.8 (top) and 2 Å (bottom). Data for larger Si interface layer thicknesses also support an actual Si coverage of about 80% of the nominal coverage obtained from flux calibration.

The very existence of interference patterns in Figs. 4(a) and 4(b) indicates that most of the Si atoms remain localized within a pseudomorphic interface layer rather than diffusing in the bulk. Analogous studies of thicker Si interface layers produced average layer thicknesses ranging from 70% to 90% of the nominal values. Together, the results of Figs. 2–4 demonstrate that the combination of temperature-rate deposition conditions employed for Si results in well-localized Si layers with relatively abrupt interfaces. The observed reduction in Si interlayer thickness relative to the values estimated from flux calibration or XPS studies[20,37] may, in principle, indicate that diffusion of a fraction of the deposited Si atoms in the III-V substrate or overlayer may occur during the longer growth times employed to synthesize the multilayer samples used for TEM and XRD analysis. Preliminary studies indicate, however, that it is still possible to grow high-quality Si-GaAs superlattices by this method.

In Fig. 5 we show the experimental [Fig. 5(a)] and simulated [Fig. 5(b)] diffraction pattern in the vicinity of the symmetric (400) GaAs reflection from a 15-period Si-GaAs(001) superlattice. The dominant feature is the GaAs substrate peak. The experimental pattern exhibits satellite peaks up to the third order. The closest match between experiment and dynamical simulations was obtained for an average superlattice composition $(Si)_{3.2}(GaAs)_{50.5}$, where the noninteger number of monolayers for Si reflects thickness fluctuations across the structure. We emphasize that satellite peaks are affected by interface disorder, and high-order peaks are more sensitive than low-order peaks.[36] The remarkable agreement between experiment and the simulation for ideal structures underscores that ideal pseudomorphic strain and fairly abrupt interfaces can be obtained even in superlattice structures grown in several h.[55]

Previous studies of Si redistribution during III-V growth have mostly examined Si coverages of a few percent of a monolayer obtained during growth interruption (under constant As flux) of homogeneous GaAs or Al-

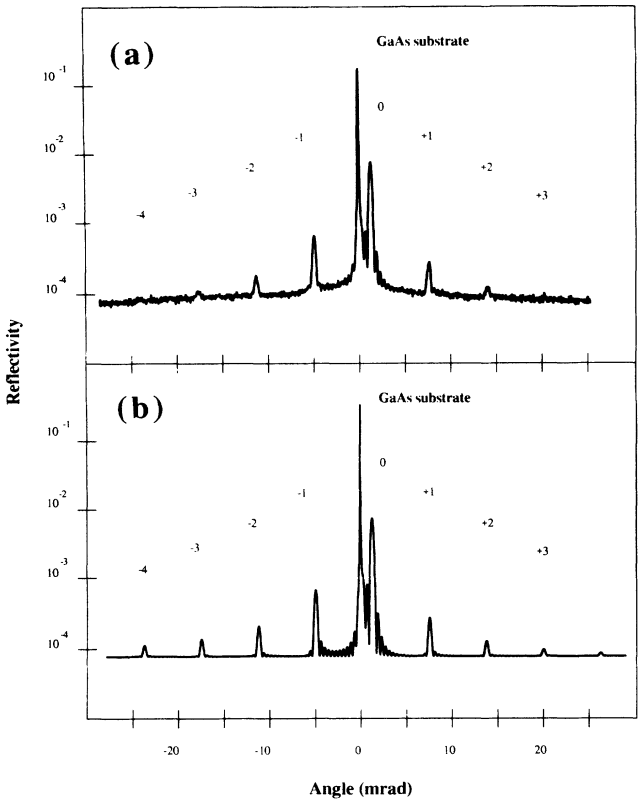

FIG. 5. Experimental (a) and calculated (b) x-ray-diffraction pattern in the vicinity of the symmetric (400) GaAs reflection for a 15-period Si-GaAs superlattice. Satellite peaks up to the third order are clearly observed. Best agreement between the experimental and calculated patterns was obtained for an average superlattice compositon $(Si)_{3.2}(GaAs)_{50.5}$.

GaAs layers. Lower Si deposition rates and higher growth temperatures are usually employed. Final Si distributions with FWHM from 35 to 53 Å in GaAs and 51–118 Å in AlGaAs have been reported,[32,56] the asymmetry of the distribution suggesting preferential redistribution toward the surface. We suggest that the more abrupt profiles we are able to obtain are due to the combination of the higher Si deposition rate and lower growth temperature. A word of caution is required, however, when comparing Si spatial distributions determined with different techniques. TEM, XRD, and XPS (Ref. 20) indicate that most of the deposited Si atoms are localized in pseudomorphic interface layers irrespective of their charge state, but cannot rule out long-range diffusion of a fraction of such atoms. Conversely, transport techniques[32,56] provide information only on the location of Si-related donor species.

C. Si-induced local dipole

We have determined the effect of Si interface layers on the valence-band offset by means of XPS *in situ* by monitoring the variation in the interface core separation ΔE_{cl} as a function of interface layer thickness. As an example, we show in Figs. 1(c) and 1(d) the Ga 3*d* and Al 2*p* core levels for AlAs-GaAs(001) and GaAs-AlAs(001) heterostructures in the presence of 0.5 ML of Si deposited at the interface. The corresponding measured ΔE_{cl} in Figs. 1(c)–1(d) were 54.02±0.03 and 54.78±0.03 eV, respectively. In the leftmost inset of Fig. 1 we show for AlAs-Si-GaAs(001) that ΔE_{cl} (open circles) is independent of AlAs overlayer thickness in the coverage range of 15–30 Å. This result, together with the relatively short photoemission sampling depth employed, indicates that the observed change in ΔE_{cl} reflects an actual variation in band offset and not doping-induced band bending variations or interface reactions.

The reproducibility of these results is illustrated in the third and fourth rows of Table II, where we summarize measurements of ΔE_{cl} for 41 AlAs-Si-GaAs(001) heterostructures and ten GaAs-Si-AlAs(001) heterostructures for a Si interface layer 0.5 ML thick. We observe average values of $\Delta E_{cl}=54.02\pm0.05$ and 54.77 ± 0.03 eV, corresponding to $\Delta E_v=0.02\pm0.08$ and 0.77 ± 0.08 eV for AlAs-Si-GaAs(001) and GaAs-Si-AlAs(001), respectively. The average values of ΔE_{cl} measured as a function of Si interface layer thickness in the 0–2-ML range are summarized in Fig. 6 (Ref. 57), with error bars reflecting the standard deviation of the distribution (thick vertical bars) or the uncertainty on a single measurement (thin vertical bars).

The effect of the Si interface layer is to increase the valence-band offset for GaAs-Si-AlAs(001) heterostructure and decrease the offset in AlAs-Si-GaAs(001). This is the behavior expected from the theoretical models of Refs. 2, 15, and 18 for charged interfaces provided that a Si bilayer develops gradually between an As-terminated substrate and a cation-initiated overlayer. In fact, calculations by Peressi *et al.*[18] quantitatively reproduce the data in Fig. 6 up to a Si interface layer thickness of 0.5 ML. The calculations were performed assuming that the

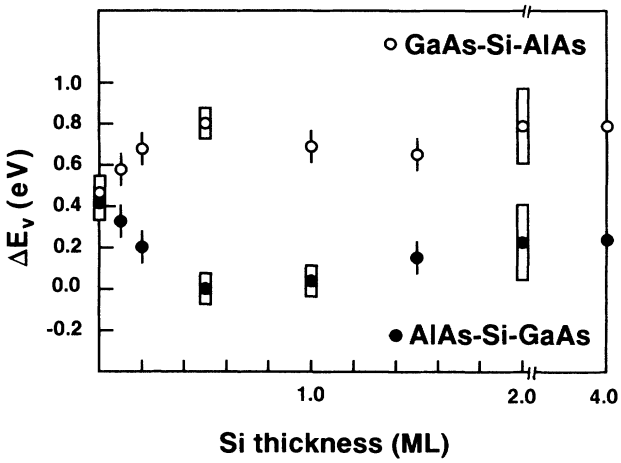

FIG. 6. Valence-band offset for AlAs-Si-GaAs(001) (closed circles) and GaAs-Si-AlAs(001) heterostructures (open circles) as a function of the thickness of the pseudomorphic Si layer at the interface. Thick vertical bars show the standard deviation of the data from a series of samples (see Table II). Thin vertical bars show the uncertainty on a single measurement.

Si atoms are uniformly spread over two consecutive atomic layers even at coverages less than two monolayers in order to ensure local charge neutrality, the appropriate effective inverse dielectric constant is that of a hypothetical bulk alloy, with the same composition as the doped bilayer, and the III-V overlayer growth is cation initiated also on top of the Si layer.[18] In this picture the two interfaces are charged with opposite polarity, and the electrostatic field formed across the Si layer is at the origin of the interface dipole that modifies the band offsets.

Although the interface dipole observed in Fig. 6 is consistent in direction and order of magnitude with the above simple model, theory would predict a dipole increasing monotonically with Si thickness, while a maximum dipole of about 0.4 eV is observed experimentally (Fig. 6) at a Si coverage of only 0.5 ML. At higher coverages, the Si-induced change in offset saturates or decreases slightly in magnitude, for GaAs-Si-AlAs(001) and AlAs-Si-GaAs(001) structures, respectively. The maximum observed dipole (0.4 eV), although reduced relative to theory, still accounts for the widest range of tunability (0.8 eV) ever reported, to our knowledge, for any semiconductor heterostructure.

As far as the Si thickness dependence of the dipole is concerned, several authors[2,12–14,15,17,18] emphasize that the presence of a field across a Si layer confined by two ideal charged Si/III-V interfaces would yield a divergence in the total energy of the system with increasing Si thickness. Consequently, the establishment of neutral interfaces through the formation of appropriate defects should be thermodynamically favored. If the formation of charged substitutional defects is responsible[2,12–14,17,18] for the decrease in interface dipole observed in Fig. 6 at high Si coverages, small unintentional variations in growth conditions may affect severely the resulting dipole. In the fifth and sixth rows of Table II we summarize XPS measurements for seven AlAs-Si-GaAs(001) heterostructures and 16 GaAs-Si-AlAs(001) heterostructures for a nominal Si interface layer thickness of 2 ML's. The average values of the interface core separation $\Delta E_{\rm cl}$ are 54.23 ± 0.15 and 54.77 ± 0.15 eV, respectively. The standard deviation of the distribution is three to five times larger than that observed for Si interface layer thicknesses of 0.5 ML, indicating that unavoidable small fluctuations in growth parameters do affect more severely the resulting interface dipole.

If the formation of charged substitutional defects leads to the establishment of neutral interfaces, in the high-Si coverage limit the Si-induced dipole should saturate to a constant value determined by the individual IV/III-V and III-V/IV interfaces. If the commutativity rule is satisfied for Si-GaAs and Si-AlAs junctions, then the Si-induced dipole should tend to zero. In the seventh and eighth rows of Table II we summarize XPS measurements for AlAs-Si-GaAs(001) and GaAs-Si-AlAs(001) heterostructures with nominal Si interface layer thicknesses of 4 ML's. The corresponding average values of the overall valence-band offset are 0.30 ± 0.08 and 0.77 ± 0.08 eV, respectively, values that are consistent with those observed for a Si interface layer thickness ~ 2 ML's. The implication is that in the high-Si-coverage limit the Si-induced dipole does saturate to a constant value different from zero, as expected in the presence of neutral asymmetric IV/III-V and III-V/IV interfaces. Rather than in terms of an interface dipole, this result could be described more appropriately as a Si-induced deviation from the transitivity rule of $0.42-0.30=+0.12\pm0.10$ eV for AlAs-Si-GaAs(001) and $0.46-0.77=-0.31\pm0.10$ eV for GaAs-Si-AlAs(001).

The observed deviations could be quantitatively correlated to violations of the commutativity rule for Si-GaAs and Si-AlAs if the corresponding IV/III-V and III-V/IV valence-band offsets were to be measured individually. Such measurements would require reliable determinations of the interface core separation for the Si $2p$ and group-III core levels, and estimates of the effect of pseudomorphic strain on the core binding energy in Si. The latter has been recently estimated by a number of authors,[37,58,59] but the former is difficult to obtain because of the small critical thickness of pseudomorphic Si layers on GaAs. In these conditions we only mention here that the observed deviations are of the same order of magnitude of those expected from recently reported asymmetries in other IV/III-V interfaces. For example, valence-band offsets of 0.23 ± 0.05 and 0.46 ± 0.05 eV have been reported for GaAs-Ge(110) and Ge-GaAs(110) interfaces, respectively.[60,61] The consequent predicted deviation from the transitivity rule for a hypothetical GaAs-Ge-GaAs(110) heterostructure would be $0.23-0.46=-0.23\pm0.07$ eV, if entirely due to the asymmetry of the two neutral interfaces present in the system. Since effects similar to those reported here for AlAs-Si-GaAs and GaAs-Si-AlAs structures are also observed for AlAs-Ge-GaAs and GaAs-Ge-AlAs structures (Ref. 21), this argument seems to us especially relevant.

We also mention that valence-band offsets of 0.35–0.45 eV have been recently reported in Ge-Ge(111) and Si-Si(111) *homojunctions* involving amorphous overlayers[22,62] as a result of the fabrication of GaAs and GaP layers, respectively, at the interface. Such offsets are sensibly smaller than those predicted by theory[2,15,18,22] for charged IV/III-V and III-V/IV interfaces, and this may indicate that individual neutral interfaces are formed also in IV/III-V/IV structures.

In the past, monolayer coverages of metallic impurities have been shown to cause changes in band offsets in several heterojunction systems involving nonpolar substrate surfaces and amorphous Si or Ge overlayers.[63,64] Proposed explanations involved an electronegativity-induced asymmetric charge transfer from the interface species to the two semiconductors,[63] or a Schottky-like correction to the heterojunction band lineup determined by the local work function of the metallic interface species.[64] In the case of AlAs-Si-GaAs(001) and GaAs-Si-AlAs(001) heterostructures, the same nonmetallic amphoteric interface chemical species is found to decrease or increase the band offset depending on the growth sequence, and the maximum interface dipole is observed at a Si coverage well below a monolayer. This phenomenology is difficult to reconcile with the simple models of Refs. 63 and 64 without introducing new parameters such

as a local electronegativity or work function dependent on orientation and Si coverage, which would be difficult to determine independently.

A different method to control band discontinuities through the fabrication of δ-doped layers close to the interface has been recently proposed by Shen *et al.*[65] A *p*-type δ-doped layer grown by MBE in GaAs 50 Å away from a *n*-isotype InAs-GaAs heterojunction was found to increase by 0.56 eV the effective barrier height for electron injection across the junction. This effect is reportedly due to the modulation of the conduction-band–Fermi-level separation on the scale of 2000–3000 Å in the presence of the *p*-type δ-doped layer in the *n*-type matrix. This mechanism cannot be invoked to explain our results for AlAs-Si-GaAs for three main reasons. First, our sampling depth is determined by the photoelectron escape depth and probes the valence-band offset on an atomic scale rather than the long-range electrostatic potential. Secondly, the δ-doping mechanism[65] is expected to increase the effective barrier height in isotype heterojunction with opposite doping, while our results indicate (Table II) that an identical change in valence-band offset is detected for *n*-isotype as well as *p*-isotype heterojunctions. Finally, the position of the Fermi level at the interface does not appear to correlate with the presence of a δ-doped layer in one or the other of the two III-V semiconductors comprising the junction. For example, from the core binding energies relative to the Fermi level, we see that in AlAs-Si-GaAs(001) heterostructures (0.5 ML Si) the position of the Fermi level varies as much as 0.6 eV from sample to sample, with the average position being some 1.1 eV above both E_v(GaAs) and E_v(AlAs). In GaAs-Si-AlAs(001) heterostructures (0.5 ML Si), the position of the Fermi level varies by as much as 0.6 eV also, with the average position being some 1.3 eV above E_v(AlAs) and 0.5 eV above E_v(GaAs).

Several authors suggested that the growth of a Si interface layer in a III-V MBE system may give rise to a highly doped Si layer because of residual As in the growth chamber, and that the Fermi level at the junction may be pinned near the Si conduction-band minimum.[26–30] For a fully developed strained Si layer, E_v(Si) would lie 0.39 ± 0.10 eV above E_v(GaAs) in Si-GaAs(001) structures, and 1.02 ± 0.10 eV above E_v(AlAs) in pseudomorphic Si-AlAs(001) structures.[37,66] People[67] calculated that the band gap of coherently strained Si layers on Ge (and therefore also on GaAs) would be reduced by 45% (0.61 eV). Consequently, the conduction-band minimum E_c(Si) would lie 1.0 ± 0.2 eV above E_v(GaAs) on GaAs(001) substrates and 1.6 ± 0.2 eV above E_v(AlAs) on AlAs(001) substrates. Such locations can be compared with the average positions of the interface Fermi level derived above of 1.1 and 1.3 eV from the substrate valence-band maximum, respectively. The comparison would suggest that the Fermi level at the interface tends to be pinned near the position of the Si conduction-band minimum at the Si-substrate junction. However, we caution the reader that the position of the Fermi level varies by as much as ±0.6 eV from sample to sample, and that in the 0.5–2.0-ML Si coverage range the Si band structure is unlikely to be fully developed.

IV. CONCLUSIONS

Pseudomorphic Si interface layers can be grown by a suitable combination of high-rate and low-temperature deposition in AlAs-GaAs heterojunctions as well as GaAs-GaAs homojunctions by molecular-beam epitaxy. The onset of strain relaxation is observed for Si thickness of 4–8 ML's, with large relaxation observed at 14 ML's.

While GaAs-AlAs(001) and AlAs-GaAs(001) heterojunction band offsets follow remarkably well the commutativity rule, GaAs-Si-AlAs(001) and AlAs-Si-GaAs(001) structures exhibit deviations from the transitivity rule of up to 0.4 eV. The magnitude of the deviation varies nonmonotonically with Si interface layer thickness, and is maximum at a Si coverage of 0.5 ML.

Heterojunction models in which Si/III-V interfaces are charged account for the direction and order of magnitude of the observed deviation, provided that the Si interface layer is fabricated on an As-terminated substrate, and that the growth of the III-V overlayer is cation initiated in all cases. The observed saturation of the interface dipole at Si coverages of 2–4 ML's, however, suggests that, at least in the high-Si-coverage limit, the deviations from the transitivity rule may reflect asymmetries in neutral Si/III-V and III-V/Si interfaces. Such neutral individual junctions may be formed through cation or anion swaps across the interfaces, as suggested by several authors.

Whatever the actual charge state of the individual interfaces might be, the fabrication of group-IV pseudomorphic layers at the interface offers a reproducible way of tailoring AlAs-GaAs band offsets in an unprecedentedly wide range of energies (0.8 eV). The position of the Fermi level at the interface is approximately consistent with the location of the conduction-band minimum in pseudomorphic Si layers on GaAs or AlAs substrates, although it is difficult to see how fully developed n^+-Si/III-V heterojunctions may already exist at Si coverages well below 1 ML.

Preliminary x-ray-diffraction studies indicate that Si-GaAs(001) superlattices and multiple-quantum-well structures can be fabricated with the same methodology. This will make it possible to probe by optical methods the neutral versus charged state of IV/III-V interfaces and the existence of macroscopic electrostatic fields.

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[50]The linearly extrapolated position of E_v yielded bulk core-binding energies (Refs. 20 and 37) relative to E_v of 18.86±0.05 eV for the Ga 3*d* core levels in GaAs, and 72.86±0.05 eV for the Al 2*p* core levels in AlAs. Such values may be slightly different from author to author, depending on the experimental energy resolution, and, when a fit to the theoretical DOS is employed, on the broadening parameter. However, the relevant quantity for the determination of ΔE_v is only the binding energy difference ΔE_b, which is consistent among most authors: 54.00 eV in Refs. 20 and 37, 53.95 eV in Ref. 38, 53.99 eV in Ref. 40, and 53.97 eV in Ref. 41.

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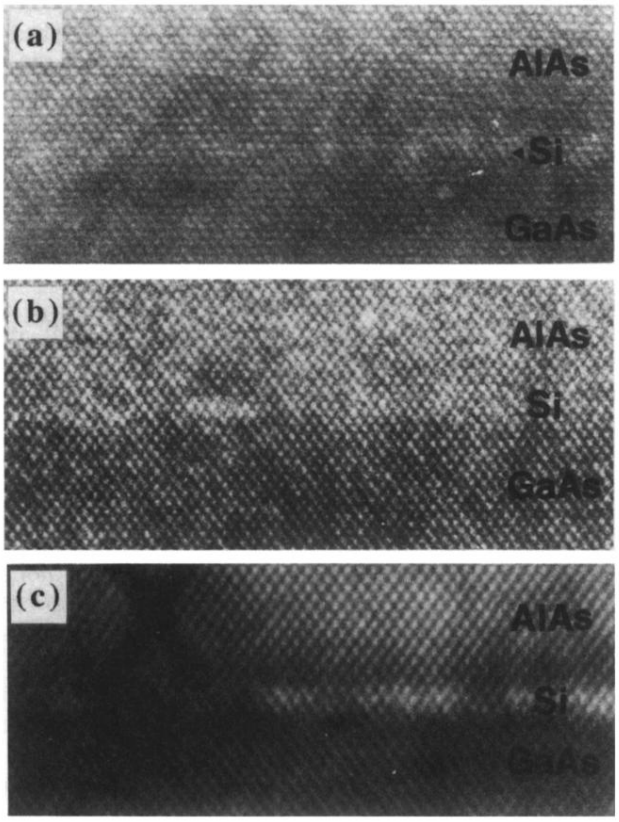

FIG. 2. High-resolution transmission-electron microscopy photographs [(110) cross section] of AlAs-Si-GaAs(001) heterostructures with a Si interface layer thickness of 2 (top), 4 (center), and 8 ML (bottom).

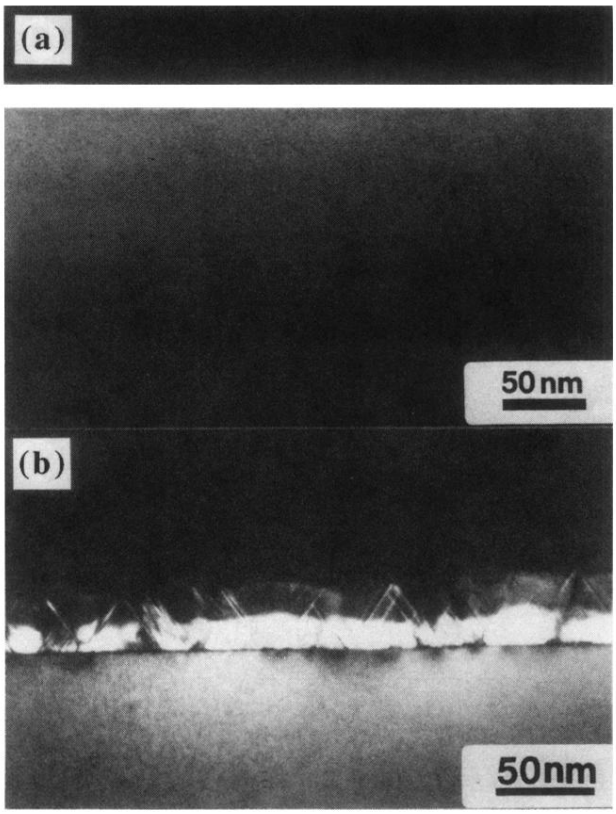

FIG. 3. Dark-field, $\mathbf{g}=200$, image [(110) cross section] of a GaAs-AlAs-Si-GaAs(001) heterostructure with a Si interface layer thickness of 2 (top) and 14 ML (bottom). The AlAs layer appears bright because of the difference in the F_{200} structure factor for the two semiconductors. The Si interface layer is located at the boundary of the AlAs layer and the GaAs buffer directly below.