Tunneling in all-high-T_c edge junctions with deposited barriers

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All-high-T_c-material edge junctions consisting of laser-ablated Y-Ba-Cu-O electrodes and an *in situ* rf-sputter-deposited MgO barrier have been fabricated whose *I-V* characteristics show tunneling-related effects. These include a junction resistance with an exponential dependence on the nominal-barrier thickness, gaplike structure observed in the conductance curves, and Josephson effects. These properties are very sensitive to the choice of materials-processsing method for the junction interfaces.

Tunneling is a powerful technique for studying the physical properties of superconductors and has also led to many interesting applications.[1,2] Since the advent of high-T_c materials, many attempts have been made to study tunneling in these materials both by scanning tunneling microscopy (STM),[3] and by building a variety of tunnel junction structures[4–7] including point contracts.[8] While most of this work has concentrated on transport from high T_c to low T_c or to a normal metal, there has been some work on all-high-T_c junctions. However, due to the numerous materials problems encountered in high-T_c work, it has been difficult to achieve all-high-T_c junctions[9–11] with some control over the junction characteristics and, in particular, the barrier region. For example, if tunneling is the dominant mode of transport across the barrier, then the resistance of the junctions should depend exponentially on the barrier thickness. In this paper we report on the *in situ* fabrication of all-high-T_c (Y-Ba-Cu-O) edge junctions in which sputter-deposited MgO barriers are used in the thickness range of 0.5–2 nm. In this range the junction resistances are observed to change by about four orders of magnitude. These junctions also exhibit a variety of tunnel-related effects such as gaplike structure in the higher-resistance samples and Josephson effects in the low-resistance samples.

The junctions studied consisted of two laser-ablated, epitaxial films of Y-Ba-Cu-O separated by a sputter-deposited barrier of MgO. The junctions were fabricated on substrates of $SrTiO_3$ and were made in the edge junction configuration[12] which is shown schematically in Fig. 1. Typical Y-Ba-Cu-O film thicknesses were about 0.3 μm. After deposition of the first or base electrode a thick insulating film of MgO was deposited, often *in situ*[13] to protect the top of this electrode. This bilayer was then removed from the vacuum system and patterned photolithographically using ion milling to expose the edges.[12] Alternatively, the protective MgO layer was deposited through a lift-off stencil and then used as a self-aligned ion milling mask. While both vertical and angular edges were studied, the junction described below had edges made at an angle of about 35 degrees with the substrate. After removing the resist the sample was replaced in the fabrication system for the formation of the barrier and deposition of the counterelectrode. However, before the barrier material was deposited, an *in situ* ion milling of the exposed edges was performed to remove damaged regions from the edges. This cleaning step which consisted of a 4-min Ar ion milling at 350 V was performed on each set of junctions to insure that the initial condition of the edge surface was the same each time a barrier was formed. Variations in the treatment of these edges generally resulted in large changes in the subsequent devices.[13] The above treatment was held constant for the series of junctions described in this work. In this way properties of the subsequent junctions were dependent mainly upon the thickness of the deposited barrier and the "constant" interface between the barrier and the superconductors. After this cleaning step and without breaking vacuum, barriers of MgO were sputtered onto the samples to the desired thickness as indicated in Fig. 1. The substrate temperature was 400 °C and 50 W of rf power were used in an Ar pressure of 45 mT. The deposition rate for the sputtered MgO was determined separately on flat surfaces to be about 1 nm/min. Immediately after deposition of the MgO the samples were brought to 750 °C and the counter-electrode Y-Ba-Cu-O was deposited. Before removing the sample from the deposition chamber, Ag contacts were also deposited. A final *ex situ* photolithographic patterning and ion milling of the counterelectrode pattern completed the devices. As indicated in Fig. 1 the Y-Ba-Cu-O counterelectrode is deposited onto the $SrTiO_3$ substrate, which is covered by the very thin MgO barrier. The electrical properties (T_c and J_c) of these films remained quite good and, in general, were very close to those of the base electrode.

A complete chip or sample contained about 60 junc-

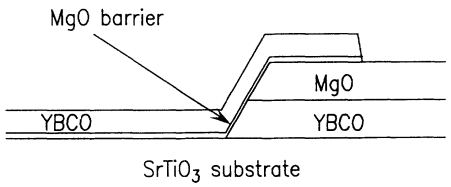

FIG. 1. Schematic cross sectional view of an all-high-T_c edge junction fabricated on a $SrTiO_3$ substrate using vapor-deposited barriers of MgO

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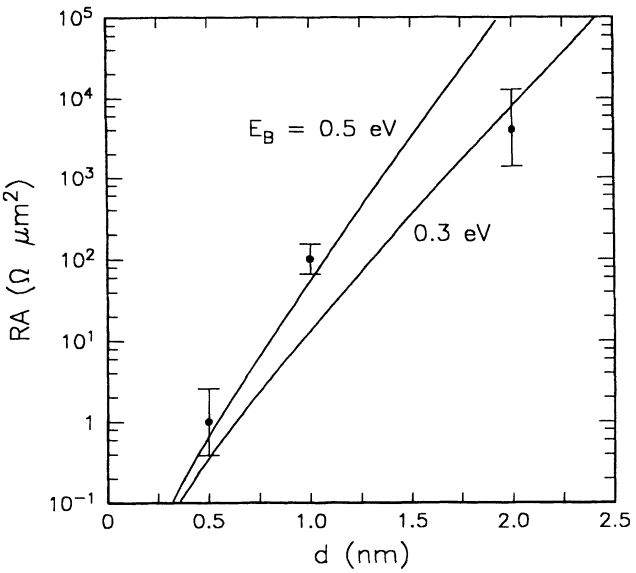

FIG. 2. Resistance area product RA the nominal thickness of the deposited MgO barrier d. The solid lines are derived using Eq. (1) and the indicated barrier height in eV.

tions and superconducting quantum interference devices (SQUID's) as well as straight-line segments to independently measure T_c and J_c. The junction areas were determined by the slant height of the edge (about 0.5 μm), constant for all junctions and by the linewidths of the counterelectrodes, which were varied from 2 to 40 μm. The current-voltage characteristics of the junctions were measured and the low-voltage (ohmic) resistance of each device was determined at 4.2 K. This resistance multiplied by the junction area (RA) is plotted in Fig. 2 as a function of the deposited barrier thickness. Each data point in Fig. 2 represents several single junctions of different areas taken from the same central region on each chip. It can be seen that at least four orders of magnitude change in RA is obtained by varying the nominal barrier thickness from 0.5 to 2 nm. Such a large change in resistance is indicative of a tunneling mechanism. Some curvature is evident in Fig. 2. It is to be expected that for the thinnest barriers, the coverage by the deposited barrier may not be totally uniform, resulting in some shunting of the barrier. In fact some junctions did exhibit shorts which were easily identified and these are not included in this plot. The actual resistances for the thickest barriers as shown in Fig. 1 may also be higher than indicated due to the possibility of leakage through the thick protective layer of MgO deposited on top of the base electrode From Fig. 2 it can be seen that a change in barrier thickness of about 0.5 nm results in a two-orders-of-magnitude change in the junction resistance. An approximate barrier height Φ_0 can be determined from the data using the WKB approximate formulation[14] for the resistance R of a rectangular barrier of height Φ_0 at low voltages (in the ohmic range) as shown in Eq. (1),

$$RA = 4\pi \frac{h}{e^2} d^2 \frac{e^{2Kd}}{1+2Kd} , \quad (1)$$

where $K = (2m\Phi_0/\hbar^2)^{1/2}$, d is the nominal deposited barrier thickness, A is the junction area, and m is taken as the free-electron mass. A fit to the data using Eq. (1) is shown in Fig. 2 and results in a barrier height in the range 0.3–0.5 eV. Barrier heights of about 1 eV have been measured for deposited MgO on Nb and NbN surfaces.[15] These metallic surfaces are much smoother and expected to be more stoichiometric than Y-Ba-Cu-O surfaces. This comparison and the realization that we are dealing with barrier thicknesses of about 1 nm, indicates that while the barrier coverage and interface quality may not yet be ideal, some real control of the junction properties has been achieved.

The error bars in Fig. 2 are an indication of the size of the deviation from the scaling of the junction resistance with area. The data for the junctions with a nominal 1 min barrier show excellent scaling with area, as shown in Fig. 3 as conductance versus junction length ($\sim$ area). Junctions for the 0.5 and 2.0 nm barriers show much greater spread as a function of area. If all the junctions on a given sample are included, deviations are also larger, indicating that there are real nonuniformities over about 0.25 cm^2. As mentioned above, all junctions in this report are taken from a central area about 0.05 cm^2. Such deviations from scaling also occur if we attempt to correlate G versus area for the SQUID's on the chip. However, in that case we believe that the local geometry, which is different for a single junction as compared to a SQUID, may be the cause of additional variability. At this point this spread in device parameters is not surprising in view of the laser-based fabrication processes. It is interesting to note that the junctions are a very sensitive means for determining process uniformities.

First derivative (conductance, G) and second deriva-

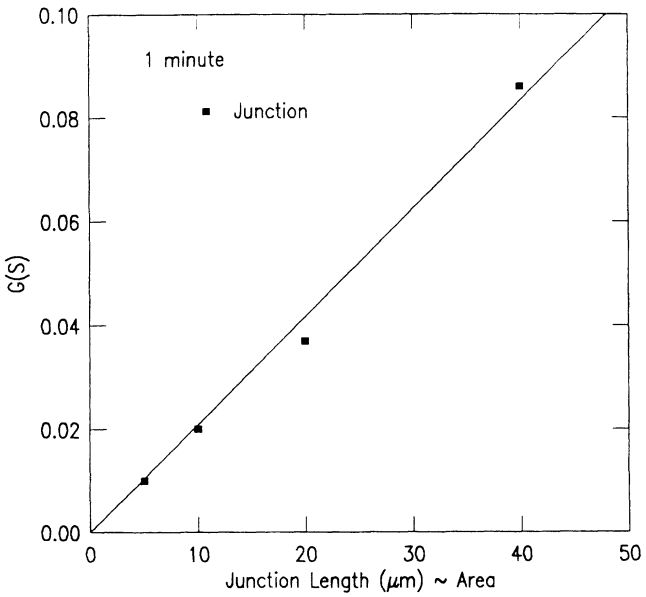

FIG. 3. Conductance G as a function of the junction area, which is proportional to the junction widths. The data are shown for the junctions whose barriers are formed using a 1 min deposition of MgO.

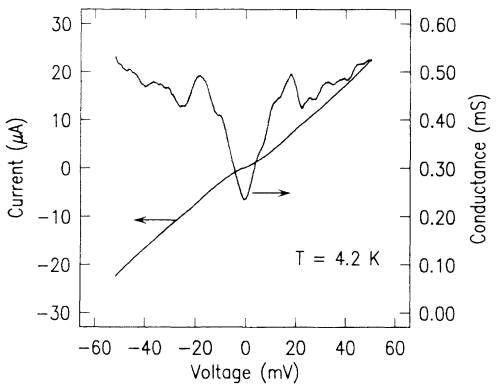

FIG. 4. Current and conductance voltage for a 20-μm wide junction measured at 4.2 K.

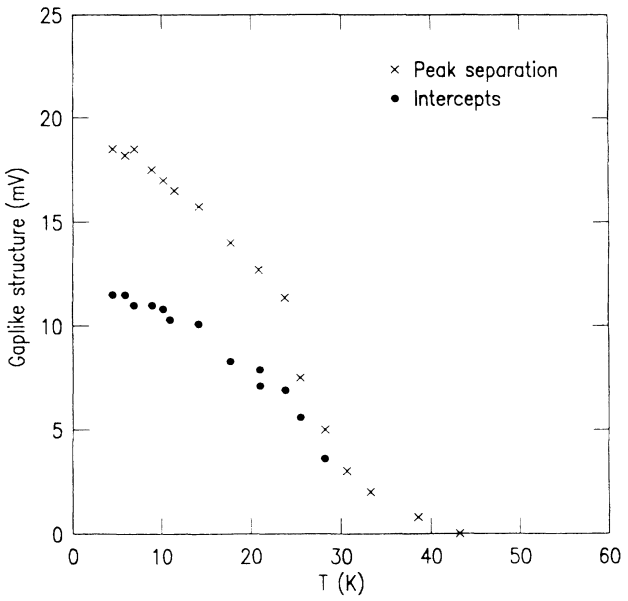

FIG. 5. Temperature dependence of the gaplike structure of Fig. 4. The $\times$'s represent the data for one half of the conductance peak separation, while the solid circles represent the intersection of the high-voltage (linear) background with the low-voltage conductance.

tives of the I-V characteristics of the junctions were measured to study in detail gap-related and other tunneling phenomena. Such structure could also be seen in some of the I-V curves themselves, indicative of the improving quality of the barrier regions. An example of such a junction measured at 4.2 K is shown in Fig. 4, where both the I-V and the G-V curves are shown for a 10-μm wide junction with a nominal 2-nm thick barrier. The low-voltage (ohmic) resistance of this junction is about 2000 ohms. The major features of interest in the G-V curves are a linear background conductance, common to many high-T_c junctions,[7,16] prominent gaplike conductance peaks at ± 18.6 mV, a lower conductance at lower voltages, and reasonably good symmetry around zero-bias. The gaplike feature has been seen in many junctions from this chip. Junctions with thinner MgO barriers tended to show less prominent peak structure but still showed a significant conductance dip at about the same voltages and centered around the origin. It should also be observed that compared to high-quality, low-T_c junctions, these junctions are quite lossy in that they exhibit large excess currents at low voltages below the gap.

In an attempt to better understand the junction characteristics, we have studied the temperature dependence of the gaplike peaks in the conductance. Figure 5 is a plot of two of these features. One feature is the voltage position of the conductance maxima (half the peak-to-peak separation). The other plots the point of intersection of the linear high-voltage conductance with the measured low-voltage conductance. It was not possible to follow the latter to zero. These features would normally be expected to reflect the energy gap in an SIS (superconductor- insulator-superconductor) tunnel junction. From the figure we see that the voltages of both features decrease monotonically with temperature with the peaks disappearing at about 43 K. If we associate 18.6 meV with $2\Delta(0)$ and 43 K with the tunneling T_c, a ratio of $2\Delta/kT_c$ of about 5 is obtained, which is a reasonable value for these materials.[3] The T_c's of the electrodes of the junctions were well above 80 K while the tunneling T_c's are reduced. This together with the nonideal conductance characteristics appear to indicate that the junction interfaces consist of regions of lower-T_c material, perhaps due to oxygen depletion or ion milling damage during fabrication. We have also attempted to fit the conductance data to various theories, both SIS and SIN (superconductor-insulator-normal metal).[3] Fits to conventional SIN theory are not satisfactory, as it is not possible to fit both the pronounced overshoots and the large conductance inside the gap region with, for example, a lifetime broadened, density-of-states model,[17] or a Gaussian distribution of gap energies model.[3] Moreover, our conductance peak data do not show the distinct asymmetries for positive and negative biases that have appeared in high-T_c data.[3,4] Standard SIS theory[1] with a lifetime broadened density of states does produce qualitative agreement with the observed features. In addition, reasonable agreement is also achieved using an Arnold proximity-effect model[1] for each electrode, assuming a 2Δ value about 21 mV. As has been noted above, the barrier heights obtained from Fig. 2 are somewhat low. Tunneling via impurities and defects (localized states) in the barrier is a possible explanation for such low apparent barrier heights. One predicted feature of such junctions is a current deficit[18] which can be obtained for junction in the superconducting state by comparing that portion of the conductance (dI/dV) which lies above the normal-state characteristic to that which lies below. If the area below is greater, a current deficit exists, while if the areas are equal, there is no current deficit. Our devices exhibit a linear background conductance, a common feature of high-T_c junctions.[3] Extrapolating a linear fit to this conductance from $\simeq 20-50$ mV back to zero bias to approximate the normal-state curve,we find that the areas above and below this line are roughly equal. Therefore, at present, the data appear to be inconsistent with a current

deficit. However, detailed comparisons of our devices with theory, including also the thickness dependence of the conductance, fits of the I-V to obtain gap values, studies of the subgap structure, and possible deficit currents will require improved device characteristics.

The junctions exhibit other behavior which is also consistent with tunneling. The junction resistance for the higher-resistance junctions is essentially independent of temperature from room temperature to 4.2 K. As mentioned above, Josephson effects have also been observed in these samples, e.g., the low resistance junctions shown to the left in Fig. 1 have significant Josephson supercurrents, which will be discussed elsewhere.[13] Quantum interference has been observed in these devices to about 76 K and Shapiro steps have been observed at both 12 and 96 GHz. While the rf coupling has not yet been optimized, the steps have been observed out to voltages of about 0.6 mV and can account for about one half of the supercurrent. Second derivative measurements on these samples have shown a variety of interesting effects, presumably related to scattering events in the barrier region (tunneling spectroscopy). More work is needed to understand these effects.

Although the junctions described above are not yet optimized, particularly those with the thinnest barriers, they show much evidence for tunneling, i.e., a resistance that is exponential in electrode separation and roughly independent of temperature, temperature-dependent gap-like structure, and Josephson effects. Much additional work remains to be accomplished in further refining of the barrier region and in understanding the complex structure in the G-V curves.

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