Observation of tunneling phenomena and the charging effect through small constricted regions in semiconductors fabricated with a focused ion beam at 4.2 K

Shunji Nakata*
NTT Basic Research Laboratories, Musashino-shi, Tokyo 180, Japan
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Small tunnel barriers were formed on $Al_xGa_{1-x}As/GaAs$ by focused-ion-beam implantation. The samples were then measured with dc current at 4.2 K, and the *I-V* curves revealed two distinct regions depending on applied bias: a tunneling region at small bias voltage and a region where thermal current over the barrier is dominant at large bias voltage. A dip in the dI/dV curve was observed in the tunneling region in the source-drain voltage (V_{SD}) range from -5 to 5 mV. In a different sample, periodic and reproducible staircaselike steps with a periodicity ΔV_{SD} of 35 mV were observed. This phenomenon is related to the Coulomb staircase, which occurs when the capacitance of a quantum dot is very small.

The tunneling phenomenon is a quantum mechanism that occurs when an electron tunnels through a barrier which has a greater potential height than the energy of the electron. The classical model, where all particles are reflected by the potential, is of no avail to explain such a phenomenon.

With recent advances in microfabrication technology, we now have the ability to fabricate submicrometer-order semiconductor structures that exhibit a range of interesting phenomena.[1,2] Of particular interest is the phenomenon of tunneling. For example, the *I-V* characteristics of zero-dimensional (0D) tunnel diodes fabricated by different methods[3] exhibit spikelike oscillations peculiar to 0D confinement.

Tunneling has been attracting much attention in solid-state physics, but many issues remain unresolved. One such issue is the charging effect of a single electron, which has been studied using a metal-insulator-metal junction. Since the capacitance in the small junction is very small, the charging energy e^2/C becomes extremely large. In such a small junction, a double-capacitance system exhibits the Coulomb blockade where electron tunneling is prohibited.[4] In another study, clear staircaselike steps were observed by scanning tunneling microscopy (STM) in the tunneling current of a double-capacitance system.[5] The steps are formed when the tunneling rate of each junction differs, and electrons accumulate in the center region during the dynamic transport process.

Single-electron tunneling is interesting not only in metals, but also in semiconductors. Scott-Thomas[6] and Staring *et al.*[7] observed periodic current oscillations when varying the upper gate voltage in a low mobility wire ($\mu = 2-8\times 10^4$ $cm^2/V\,s$). They attributed this phenomenon to the formation of a quantum dot structure in part of a quantum wire that created the periodic oscillations. Meanwhile, Meirav, Kastner, and Wind fabricated a double-constriction structure using a split-gate method,[8] and they also observed periodic oscillations when they varied the gate voltage. Tunneling through a quantum dot has been well investigated theoretically,[9] but experiments have not yet led to a clear understanding of the Coulomb staircase in semiconductors with changes in V_{SD}.

This paper discusses tunneling phenomena in small-constriction structures fabricated using a focused ion beam (FIB), an important technology in microsemiconductor fabrication. The transport properties of the constriction are studied across a wide range of applied voltages. Charging effects at small-bias regime are also investigated in some detail. We would note that the Ga ion implantation technique employed here is better suited than the split-gate technique to study the transport properties. This is because the deep levels formed by Ga ion implantation act as acceptors, which results in steep potential profiles. This could result in a small capacitance systems, in which the charging energy is very large and periodic characteristics can be observed at higher temperatures.

We started with a modulation-doped structure grown by molecular-beam epitaxy (MBE). An undoped GaAs buffer layer (1 μm), an undoped $Al_xGa_{1-x}As$ spacer layer (20 nm), a Si-doped $Al_xGa_{1-x}As$ layer (80 nm), and a Si-doped GaAs capping layer (20 nm) were then successively grown on a semi-insulating GaAs substrate. A schematic of the sample structure is shown in Fig. 1(a). Two constrictions are formed by Ga ion implantation. The distance between constrictions is 0.6 μm and their width is 0.4 μm. The depletion length extends nearly 0.2 μm from the implanted region. A schematic energy-level diagram is shown in Fig. 1(b). The samples were annealed after implantation at 720 °C for 20 s in the Ar-based 5% H_2 gas. Ohmic contacts were formed with alloyed Au-Ge-Ni on the source and drain.

Figure 2 shows the relative resistance change of the Ga-implanted sample. This sample was fabricated from a 100-nm-thick *n*-GaAs epilayer growth by MBE. The line widths (*L*) of the implanted region were 1 and 10 μm. the horizontal axis represents the Ga-ion dose implanted in the samples, and the vertical axis is the relative resistance change. As apparent from the figure, the value increases rapidly when the number of implanted Ga ions exceeds a critical value. The implanted Ga ions exceeded this criti-

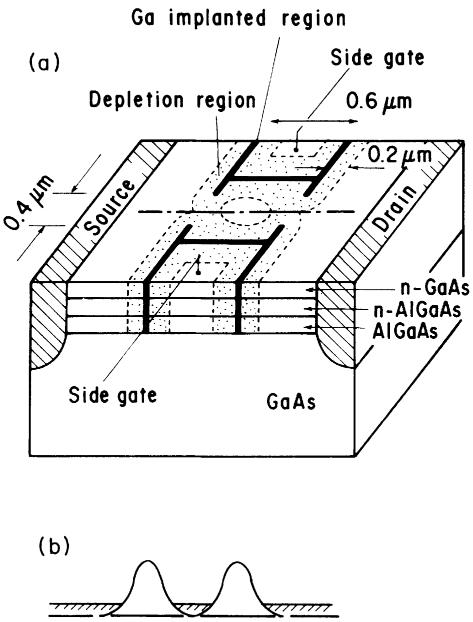

FIG. 1. (a) Sample fabricated by Ga focused-ion-beam implantation. Depleted regions are shown by dotting, and the points where side-gate voltage is applied are indicated. (b) Schematic energy-level diagram.

cal value in the fabricated samples.

Next turn to a consideration of the I-V characteristics of the two-constriction samples. Under dark conditions, current did not flow because the depletion regions were expanded. In this case, therefore, measurements were taken after slight illumination by a light-emitting diode (LED). After this initial illumination, the LED was switched off and no longer used during measurements. Carrier density was increased and depletion regions were diminished so that electrons could tunnel through the barrier, which was induced by Ga-ion implantation. At this time, the structure of the I-V characteristics was as stable and reproducible as they were under dark conditions even when the side-gate voltage and source-drain voltage were varied. The measurement temperature was 4.2 K and dc current was used. Current was driven by the constant external voltage. A simple schematic diagram of the measurement circuit is depicted in Fig. 3.

The I-V curve and the derivative one are shown in Fig. 4. V_{SD} was changed from -120 to 120 mV, while the side-gate voltage (V_g) was set to 0 V. A magnification of the I-V curve for V_{SD} ranging from -20 to 20 mV is shown in the inset. Resistance in the tunneling region is almost 3 MΩ. A drastic change in the I-V characteristics is observed at a threshold voltage (V_{th}) of 40 mV, as shown in Fig. 4. The dI/dV above V_{th} is 30 times larger than that below V_{th}. The implication of this abrupt change is that the electron transport below V_{th} is mainly dominated by tunneling and electron transport above V_{th} is dominated by thermal current over the barrier. It is also clearly demonstrated by this experiment that electron tunneling is possible through a potential barrier fabricated by Ga FIB.

At the bias regime below threshold voltage, dI/dV first increases but then immediately saturates and becomes constant (0.4 μA/V) until the voltage reaches about 40 mV. The dip observed at the V_{SD} origin differs from the usual tunneling behavior in which dI/dV typically increases monotonically.

The I-V characteristics were measured again after changing side-gate voltage V_g ($V_g = -0.3$ V) and expanding the depletion region (Fig. 5). Here again, the dip in the I-V curve around zero bias was observed, but V_{th} increased to 60 mV because the carrier density decreased and the barrier height increased.

The reason for the appearance of the dip around zero bias remains unclear. A number of explanations can be proposed. For example, one is the pinning effect of the charge-density wave,[10] and another is tunneling suppression due to a Coulomb blockade.[11] In the present experiments, electrons tunnel through the small region, so the charging effect cannot be neglected. In this system, the sample has two constrictions (i.e., two capacitances) so a Coulomb blockade might be observed under the constant-voltage bias condition. When the two tunneling rates are approximately equal, only the Coulomb blockade around zero bias should be observed.[14] However, further experiments will be needed to characterize the

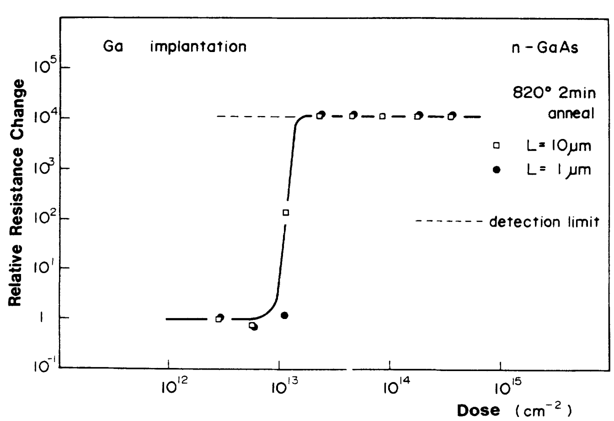

FIG. 2. Resistance change of Ga implanted samples.

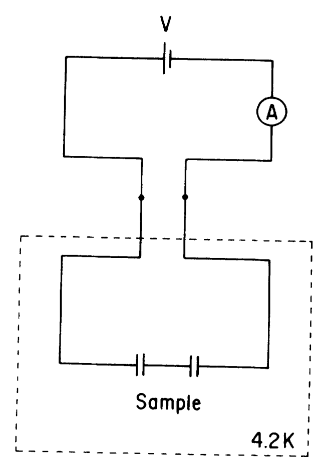

FIG. 3. Schematic diagram of measurement circuit.

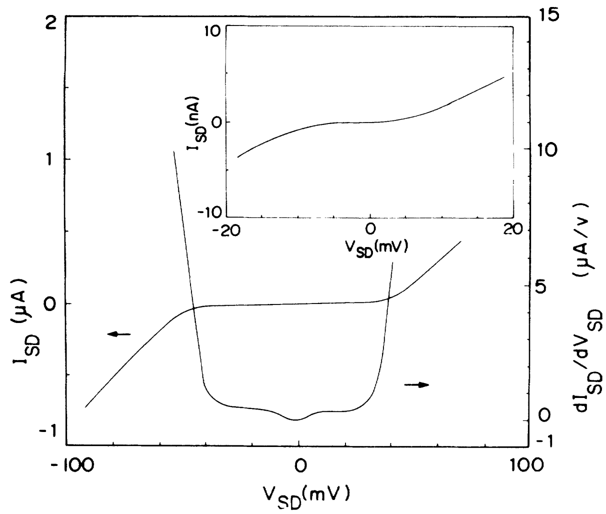

FIG. 4. *I-V* curve and dI/dV curve at 4.2 K. The inset shows the magnification of the *I-V* curve.

dip around the origin.

A second *I-V* curve for a different sample is shown in Fig. 6. Again, the measurement temperature was 4.2 K. In this case, V_{SD} was changed from 0 to 140 mV, and the side-gate voltage V_g was changed from 0 to 1.2 V in 0.3-V increments. Initially, V_g was set to 0 V and V_{SD} was changed from 0 to 140 mV. Next, V_g was set to 0.3 V and V_{SD} was again varied from 0 to 140 mV. This measurement procedure was repeated for the gate voltage up to 1.2 V. The depletion length in the central region decreases to 0.1 μm when V_g is increased to 1.2 V. In this case, markedly different periodic structures were observed from those in Figs. 4 and 5, and the characteristics were reproducible. The *I-V* curves for $V_g=0$ and 1.2 V are shown in Fig. 6. Periodicity ΔV_{SD} is 20 mV. This periodic structure is probably due to the charging effect through a small quantum dot. I_{SD} increases rapidly in the tunnel region as V_{SD} becomes larger. This is because the effective barrier height is lowered with increasing V_{SD}. Similar results were obtained in an STM experiment conducted by Wilkins, Ben-Jacob, and Jaklevic[5] where an indium droplet on an Al oxide plane was scanned by an STM tip.

After finishing the sequential measurements, a large

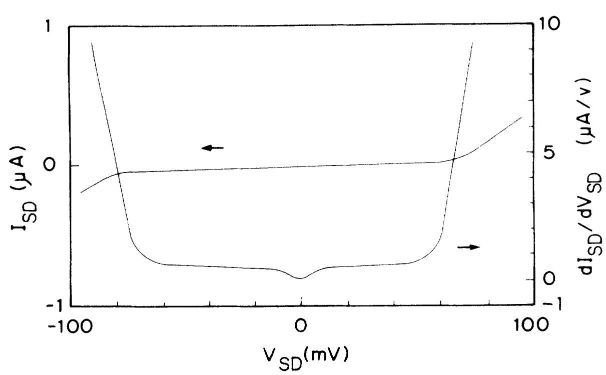

FIG. 5. *I-V* characteristics after changing side-gate voltage.

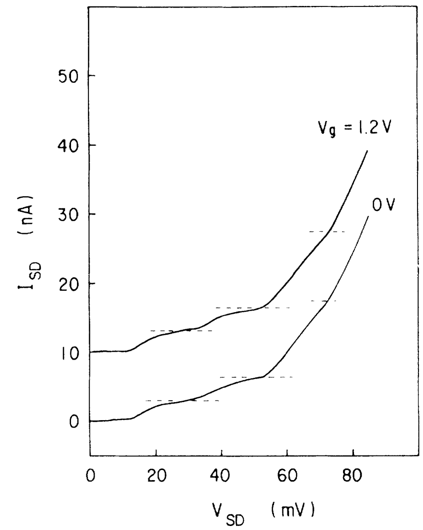

FIG. 6. *I-V* curve for a different sample at 4.2 K. *I-V* curves for different V_g are plotted by shifting each curve by 10 nA.

negative side-gate voltage of about 2 V was applied to deplete the channel and to change the charged state of impurities. Next, the sample was illuminated and measured once again at almost the same bias condition as in Fig. 6. But in this case, V_{SD} was changed from -220 to 220 mV. Here again, a well-defined periodic staircase was observed as shown in Fig. 7. Here ΔV_{SD} is 35 mV and ΔI_{SD} is 10 nA. The observed Coulomb staircase was little affected by changes in V_g, although $|V_{th}|$ did decrease as V_g was increased since the carrier density increased. (V_{th} is about 180 meV in Fig. 7.) The manifestation of the Coulomb staircase is attributed to a quantum dot structure, whose capacitance is estimated to be 5×10^{-18} (F) from the ΔV_{SD} of 35 mV. This small capacitance[12] and its independence of the side-gate voltage suggest that a quantum dot has been formed in one constriction in this case (Fig. 8).

The periodic structures might result from resonance in the zero-dimensional subbands. We can rule out this possibility, however, for three reasons: First, the tunneling current does not exhibit spikelike peaks but rather assumes the shape of a staircase. If a 0D tunneling had occurred, one would anticipate spikelike peaks when the Fermi energy in the emitter region is consistent with the 0D subband energy. Second, the barrier potential is formed by impurities implanted by the focused ion beam. This means the potential profile is not perfectly parabolic, and the energy separation will not be equal between the quantum levels. Yet the observed *I-V* characteristic is periodic and no additional structures are present. The third reason resonance in the 0D subband can be ruled out becomes apparent if we assume a parabolic confining potential[13] of $V_B=\frac{1}{2}m\omega^2(x^2+y^2)$ with an energy separation of 17 meV (half the value of ΔV_{SD}). The potential profile is considered to have a barrier height of $V_B=90$ meV, which results in a distance between origin and barrier peak of 26 nm. This assumption is based on the fact that the V_{th} for thermal current flows is 180 meV (V_B is

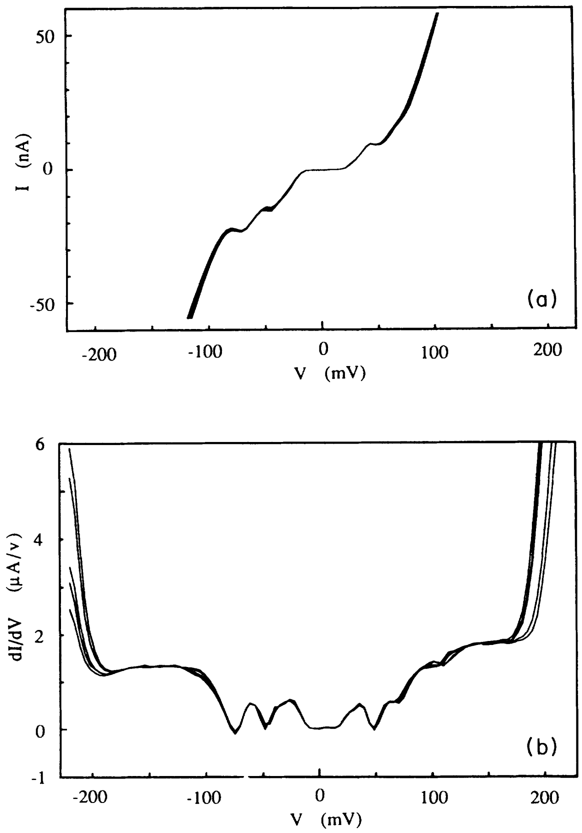

FIG. 7. (a) I-V curve after changing the potential profile at 4.2 K. A number of reproducible steps are clearly observed. (b) The derivative curve of (a).

half of V_{th}). Conductance is written as $G=(2e^2/h)T$. Using the WKB approximation, transmission coefficient T can be calculated. We find that the tunneling resistance is larger than 500 MΩ, a value that is not consistent with the experimental value. Therefore, it is possible to conclude that these characteristics are due to the charging effect.

It is known[14–16] that the I-V characteristics of small double barriers form a staircase with a voltage periodicity ΔV of e/C as shown in Fig. 9. These characteristics are induced by Coulomb blockade. If the size of the central region (i.e., capacitance) is small, the voltage change in the central region is very large when an electron accumulates in it. This means that if an electron tunnels into the central region, then another electron cannot tunnel into it because of the large voltage change e/C. But it becomes possible for two electrons to accumulate in the central region after source-drain voltage is increased. The current increases almost in proportion to the number of accumulated electrons in the central region. The staircase characteristics are known to be peculiar to small double-barrier structures.

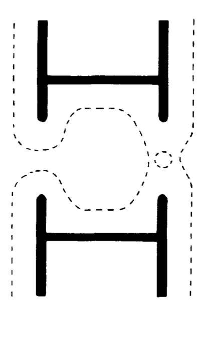

FIG. 8. Schematic image of a quantum dot in one constriction.

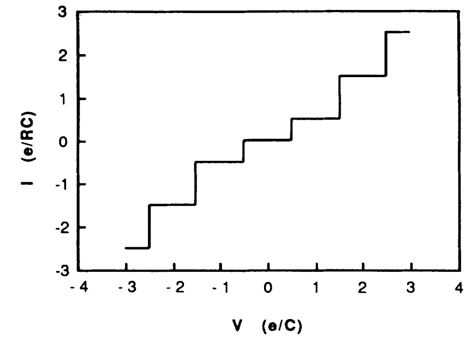

FIG. 9. I-V characteristics according to orthodox theory.

The experimental results with staircase structures are generally consistent with the above orthodox theory. There are some experimental findings, however, that are not completely consistent with the generally accepted theory. For example, there is the slight offset around the origin in the I-V curve of Fig. 7(a). In the orthodox theory, such an offset is not expected. As indicated in Fig. 8, a quantum dot is formed in part of one constriction. This means there are many random potential profiles neighboring the quantum dot, creating a pinning effect on the charge-density wave that prevents the electron from moving.[10] Current flows when applied voltage exceeds the pinning threshold voltage. This effect may account for the wide low-conductance region.

Only gentle slopes between each step were observed in Figs. 6 and 7, which contrast with the sharply defined steps in Fig. 9. This difference is most difficult to explain by the simple four-parameter theory presented in Refs. 14–16. Also, some characteristics of semiconductors differ from metal. For example, band bending which results from electron accumulation neighboring the barrier exists and the barrier height is much smaller than that of metal. These factors affect the resistance and capacitance values (that is, the tunneling rate through the barrier) when V_{SD} is changed. To bring measured results into close agreement with theory, these effects should be taken into consideration.

The periodicity in V_{SD} of 35 mV might be somewhat large when the quantum dot is formed in a semiconductor. It might be that all the applied voltage is not consumed between the edges of the quantum dot because the many impurities form the narrow channel adjacent to it. If this is the case, then the actual periodicity might be smaller than 35 mV, and the actual capacitance might be larger than the estimated value of 5×10^{-18} (F).

In conclusion, we have demonstrated that small constriction structures fabricated by FIB have two regions: a tunneling region and a region related to thermal current. In a sample thought to contain a quantum dot, a reproducible staircase is observed in the tunneling region. Considering the non-spike-like and periodic *I-V* characteristics, the staircase is attributed to the charging effect.

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*Present address: NTT LSI Laboratories, Atsugi-shi, Kanagawa 243-01, Japan.

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