Defect pool in amorphous-silicon thin-film transistors

M. J. Powell, C. van Berkel, and A. R. Franklin
Philips Research Laboratories, Redhill Surrey RH1 5HA, England

S. C. Deane and W. I. Milne
Cambridge University Engineering Department, Cambridge CB2 1PZ, England
(Received 12 August 1991)

Amorphous-silicon thin-film transistors show a threshold voltage shift when subjected to prolonged bias stress. For transistors made with silicon oxide as the gate dielectric, the threshold shift induced under positive bias is due to the creation of dangling-bond states in the a-Si:H at low energy (D_e states). The threshold shift induced by negative bias stress is due to the creation of dangling-bond states at a higher energy (D_h states). In transistors made with silicon nitride as the gate dielectric, positive bias stress causes an increase in the density of D_e states, but negative bias stress causes mainly a *reduction* in the density of D_e states. Positive bias annealing of both oxide and nitride transistors leads to an increase in the density of D_e states and a reduction in the density of D_h states. Negative bias annealing leads to a reduction in the density of D_e states and an increase in the density of D_h states. The magnitude of each change depends on the initial Fermi-level position, which is the main difference between our oxide and nitride transistors. The results are explained by a defect-pool model for the dangling-bond states in a-Si:H. Dangling bonds are formed by a chemical equilibration process, resulting in the formation of dangling bonds in each of the possible charge states. This leads to a density of states in a-Si:H consisting of coexisting components *formed* as negatively charged dangling bonds (D_e states), positively charged dangling bonds (D_h states), and neutral dangling bonds (D_0 states). Fitting the calculated density of states to the experimental results determined from the transistor characteristics leads to the conclusion that the density of D_e and D_h states dominates over the D_0 states, for all Fermi-level positions. We therefore conclude that there must be substantial densities of charged dangling bonds, even in undoped a-Si:H. Because of the wide energy separation of the D_e, D_0, and D_h states, virtually *all* the states in the lower part of the gap are D_e states and *all* the states in the upper part of the gap are D_h states. Raising the Fermi level increases the density of D_e states and lowers the density of D_h states, but the density of D_0 states remains the same. Lowering the Fermi level increases the density of D_h states and reduces the density of D_e states. Bias stress of nitride transistors, at much higher fields, leads to larger threshold voltage shifts, due to charge trapping in the nitride. Subsequent annealing leads to a new zero-bias thermal-equilibrium density of states. Transistor characteristics can be optimized in this way.

INTRODUCTION

Amorphous-silicon thin-film transistors (a-Si TFT's) are important electronic devices with widespread commercial applications in liquid-crystal displays, page-width printers and matrix image sensors. In addition to the practical applications, amorphous-silicon thin-film transistors are of great interest for the insight they provide on the fundamental physics of amorphous silicon. The ability to move the Fermi level through most of the band gap, by applying a gate voltage, without the complication of introducing dopant atoms, allows important information to be gained. This dual role is particularly significant when it comes to the study of the instability mechanisms in TFT's.

The most important instability in a-Si TFT's is a threshold voltage shift that is observed after the prolonged application of a gate voltage (bias stress). This threshold voltage shift can limit the use of the devices in some demanding applications and has therefore been studied extensively in order to identify the physical mechanisms responsible.

The technologically most important TFT currently uses silicon nitride as a gate insulator, and early work interpreted the threshold voltage shift solely as charge trapping in the gate nitride, which is known to contain a large number of traps.[1] Later work showed that there were two distinct mechanisms responsible for the threshold voltage shift, namely charge trapping in slow states in the nitride and the creation of additional fast states in the a-Si:H.[2] Detailed studies of the time, temperature, and bias dependence of the threshold shift showed that the state creation dominated at low positive bias and exhibited a power-law time dependence and a thermally activated temperature dependence, while the charge trapping dominated at high positive bias and showed a logarithmic time dependence and a weak temperature dependence.[3,4]

Further experiments showed that state creation was the only significant mechanism in transistors made with thermal silicon oxide as the gate insulator. States were created for both positive and negative bias and, furthermore, the *energy* of the created states were different when

the states were created under electron accumulation or hole accumulation.[5] In addition, we have recently studied the equilibration of deep states in TFT's, using the technique of bias annealing, and interpreted the results in terms of a defect-pool model for Si dangling bond-states involving the creation and annealing of dangling-bond states at different energies in the band gap.[6,7] Detailed investigations by Jackson have suggested that the equilibration mechanism is associated with the diffusive motion of hydrogen,[8,9] due to the observation of stretched exponential time dependence, as originally reported for a-Si:H by Kakalios, Jackson, and Street.[10] However, Crandall[11] proposed a model not requiring long-range diffusive hydrogen motion, which also produces stretched exponential behavior.

The mechanism responsible for the threshold shift in nitride transistors under negative bias stress is less clear. Negative bias induces a negative threshold shift, which we and others had associated with positive charge trapping in the nitride.[2,8] However, recently, Gelatos and Kanicki[12] have noted a similar time and temperature dependence of the positive and negative shifts and associated both with charge trapping. In this paper, we present results of the time, temperature, and bias dependence of the threshold shift for both positive and negative bias. We find that for low negative bias the dominant mechanism is the bias-stress-induced removal of states. Charge trapping dominates at high negative bias in the same way as it does for high positive bias.

We present a unifying description of the state creation and state removal processes in terms of a defect-pool model involving states at different energies in the band gap. The model is applied to both oxide and nitride transistors. The main difference between our oxide and nitride transistors is the positive fixed charge in the nitride, giving an electron accumulation at zero bias, which affects the initial equilibrium density of states. For nitride transistors, further charge trapping in the nitride alters this "quasi-fixed" charge and we show how the interplay between charge trapping and the creation and removal of states in different parts of the band gap can be used to produce optimum transistors for device applications.

BIAS STRESS

The key method used to identify the different mechanisms in a bias stress experiment is the simultaneous measurement of the transfer characteristics before and after the bias stress on an n-channel and a p-channel transistor.[2,5-7] The expected observations are summarized in Fig. 1. Creation of states in the upper part of the band gap (above the zero-bias Fermi level) leads to a positive shift of the electron threshold voltage (V_T^e), an increase of the electron prethreshold slope ($dV_g/d\log_{10}I_{SD}$) and a negative shift of the hole threshold voltage (V_T^h). Creation of states in the lower part of the band gap leads to a positive shift of the electron threshold voltage, a negative shift of the hole threshold voltage, and an increase of the hole prethreshold slope. Charge trapping in the gate insulator under positive bias leads to a positive shift
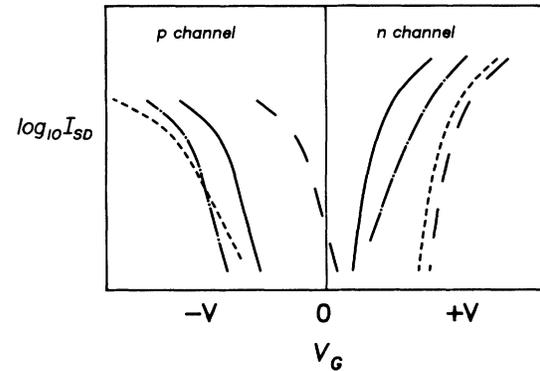

FIG. 1. Schematic representation of the effect of state creation and charge trapping on the transfer characteristics of a-Si:H TFT's. Solid line—initial characteristic; short dashed line—state creation in the lower part of the band gap; chain line—state creation in the upper part part of the band gap; long dashed line—negative charge trapping in the gate dielectric.

of both electron and hole threshold voltages, with no change in either prethreshold slope. The removal of fast states in the a-Si:H and charge trapping in the gate dielectric under negative bias lead to the inverse effects. The clear distinction between the effects requires simultaneous measurements on n- and p-channel TFT's.

A detailed analysis of both transfer characteristics can give the energy-dependent density of states throughout the band gap, using the field-effect method.[13,14] The separation of the electron and hole threshold voltages gives an indication of the integrated density of states in the amorphous silicon (cm^{-2}), provided the Fermi level is swept through all the deep states between the two threshold voltages.[2,7]

Figure 2 shows examples of experimental results for positive and negative bias on oxide and nitride transistors. In this figure, we plot the normalized transfer characteristics, as the sheet conductance $(\Omega/\square)^{-1}$ against the total-induced charge density (electrons/cm^{-2}). The sheet conductance is proportional to the source-drain current and the induced charge density is proportional to the gate voltage,

$$G = I_{SD}/V_{SD}(W/L)$$

$$Q = V_G\epsilon_{ins}/qd_{ins} ,$$

where I_{SD} is the source-drain current, V_{SD} is the source-drain bias, W/L the TFT channel width-to-length ratio, V_G is the gate bias, ϵ_{ins} the gate insulator dielectric constant, and d_{ins} is the gate insulator thickness. Plotting the results in this way normalizes them for different gate insulator materials and TFT geometrical parameters.

For oxide transistors, Fig. 2(a) shows that state creation dominates for both positive and negative bias. States are created in the lower part of the gap for positive bias and in the upper part of the gap for negative bias. For nitride transistors at low bias [Fig. 2(b)], the results show that state creation in the lower part of the gap dominates for low positive bias, while at low negative bias the dominant mechanism is the removal of states from the lower part of the band gap. However, at higher bias, Fig.
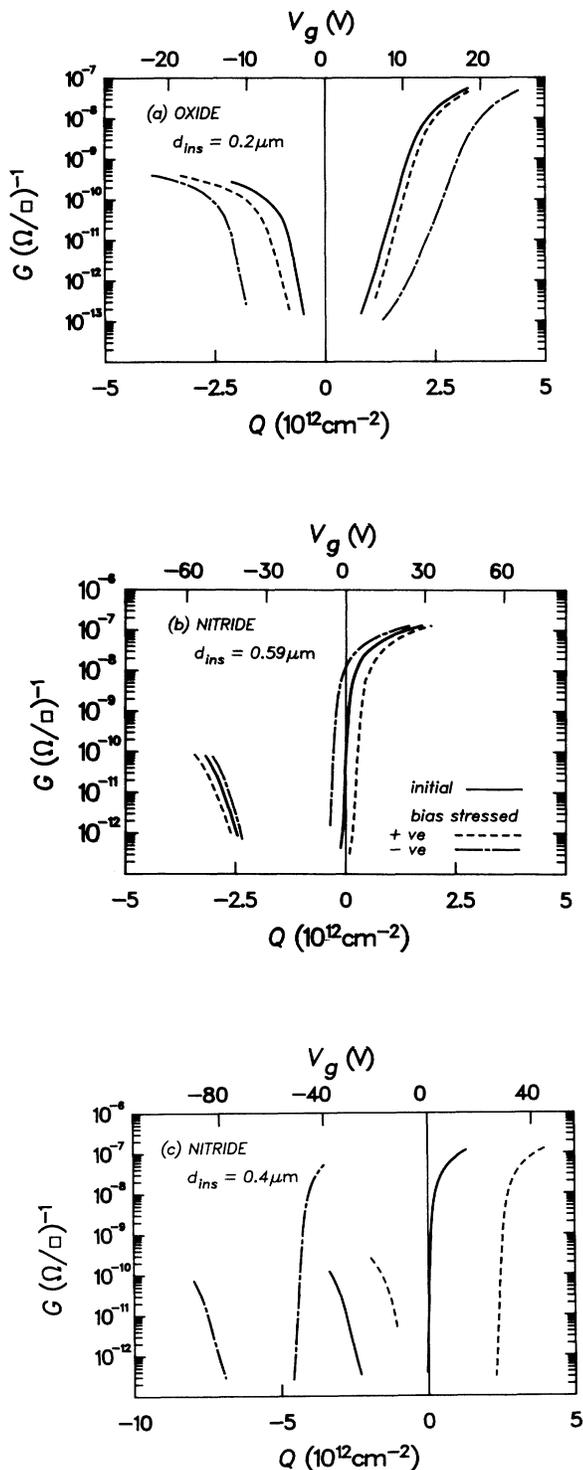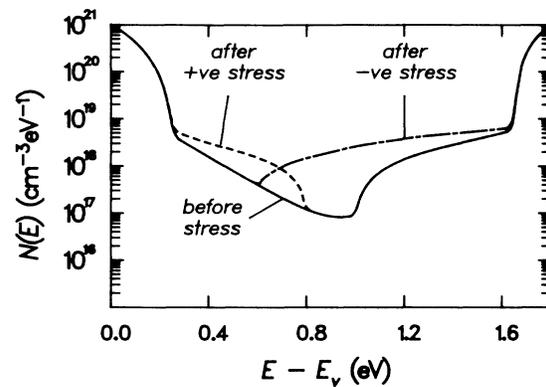
FIG. 3. Energy-dependent density of states for an oxide transistor, before (solid line) and after (dashed line) positive bias stress and negative bias stress (chain line) (Ref. 3).

2(c) shows that charge trapping becomes the dominant mechanism and that this occurs for both high positive and high negative biases.

Figure 3 shows the calculated density of states for oxide transistors, using the conventional field-effect analysis, before and after positive and negative bias stress. Clearly, the states are created at different energies.[5]

Having identified the fact that each mechanism dominates in different bias ranges, we can gain more information by measuring the time, temperature, and bias dependence of each mechanism independently. Figures 4–6 show examples of the bias, temperature, and time dependence of the threshold voltage shift for n-channel TFT's with a silicon nitride gate insulator. These transistors were made in a different growth system to those reported earlier,[2–4] but the results for positive bias show the same general trends as previously reported. The new observations are the state reduction for negative bias and the transition to a charge-trapping regime at high negative bias.

In Fig. 4, we plot the threshold voltage shift as a function of the applied gate bias, which is maintained constant during the stress time. The stress time and temperature are fixed at 10^3 s and 25 °C, respectively. For positive bias, the threshold shift increases roughly linearly
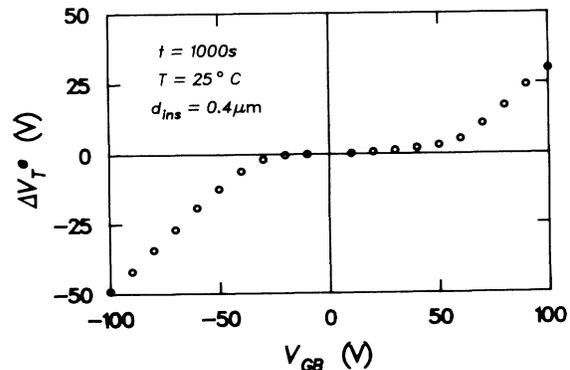

FIG. 2. The effect of bias stress on the normalized transfer characteristics of a-Si:H TFT's. Solid lines—before bias stress; dashed line—after positive bias stress; chain line—after negative bias stress. (a) oxide transistors, (b) nitride transistors at low bias, (c) nitride transistors at high bias. The stress conditions were as follows: (a) positive stress, +25 V, 25 °C, 6×10³ s; negative stress, −25 V, 25 °C, 6×10³ s; (b) positive stress, +60 V, 40 °C, 4×10³ s; negative stress, −20 V, 80 °C, 1×10⁵ s; (c) positive stress +100 V, 25 °C, 1×10³ s; negative stress −100 V, 25 °C, 1×10³ s.

FIG. 4. The bias dependence of the threshold voltage shift for an n-channel nitride transistor. For each point the threshold shift is measured for a constant bias V_{GB} maintained for a fixed constant time $t = 10^3$ s and temperature $T = 25$ °C.

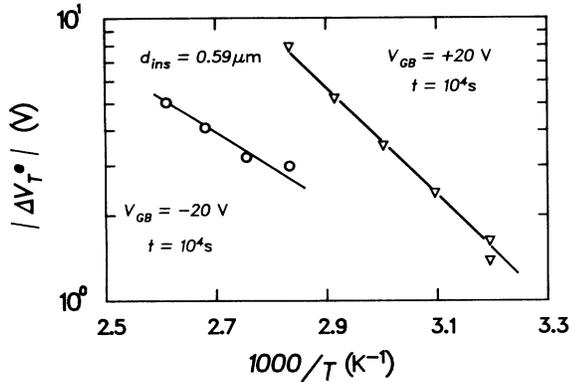FIG. 5. The temperature dependence of the threshold voltage shift for an n-channel nitride transistor, for the low bias region. Triangles—positive bias stress; open circles—negative bias stress. The threshold shift is measured for a fixed time $t = 10^4$ s and fixed bias $V_{GB} = +20$ V (positive stress) and $V_{GB} = -20$ V (negative stress). Note that ΔV_T^e is positive for positive bias and negative for negative bias.

with $V_{GB} - V_T^e$ up to about 50 V, then there is a transition at $V_{GB} = 55$ V, above which the threshold shift is dominated by charge trapping in the nitride. The charge-injection mechanism is strongly field dependent, so in a constant bias stress experiment the measured threshold voltage shift increases strongly above the transition voltage. For negative bias, we see a similar transition at about $V_{GB} = -30$ V, although some component of charge trapping is also measured at lower bias.

Figure 5 shows the temperature dependence of the threshold voltage shift measured for a constant time of 10^4 s and for a constant bias of either $+20$ or -20 V. The temperature dependence measured this way is thermally activated, with an activation energy $E_a' = 0.4$ eV for positive bias and $E_a' = 0.25$ eV for negative bias. Figure 6 shows the time dependence of the threshold shift measured for positive and negative bias, at constant temperature. The positive bias data is measured using the technique of constant-current bias stress, as previously described.[4] There is a power-law time dependence for both polarities. Clearly there is a similarity between the state creation mechanism for positive bias and the state
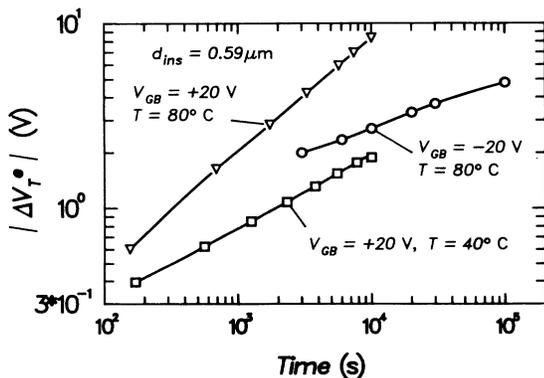

FIG. 6. The time dependence of the threshold voltage shift for an n-channel nitride transistor.

removal mechanism for negative bias. If we write the relation for the threshold shift as $\Delta V_T \sim (t/t_0)^\beta$, then the activation energy of the t_0 term is given by $E_a = E_a'/\beta$, which is found to be about 0.9 eV for positive bias and also about 0.9 eV for negative bias. These energies are associated with a barrier to defect formation or defect removal.

Similar experimental results were reported by Gelatos and Kanicki,[12] but they inferred there was charge trapping for *both* polarities and identified the barrier with some sort of activated charge injection. The results in Fig. 2(b) show clearly that there is mainly state creation and state reduction at these low biases.

BIAS ANNEALING

It is now well established that the density of states in a-Si:H is dependent on thermal-equilibrium processes and that a movement of the Fermi level away from midgap causes the density of states to increase.[15,16] In the bias-annealing technique, we apply a bias to the transistor, anneal to 200 or 240 °C and then cool to room temperature with the bias still applied. With this technique, we explore the thermal-equilibrium density of states and investigate how this is changed by annealing with a bias applied.[6,7] The bias moves the Fermi level in the interface region and the annealing causes the density of states to reequilibrate to the new Fermi energy. The integrated density of states (cm^{-2}) and the energy-dependent density of states, before and after the bias anneal, can be determined from n-channel and p-channel characteristics as before.

Figure 7 shows the integrated density of one-electron states, $N_{\text{tot}} = 2N_{\text{DB}}$ (cm^{-2}) $= C(V_T^e - V_T^h)$, as a function of the conductance activation energy after bias annealing (with the bias still applied). N_{DB} is the density of dangling bonds and the factor of 2 is because these are am-
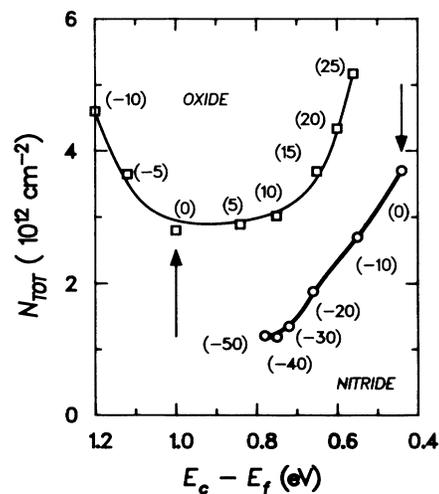

FIG. 7. The integrated density of states $N_{\text{TOT}} = 2N_{\text{DB}}$, given by $C(V_T^e - V_T^h)$, as a function of the conductance activation energy after bias annealing, for both oxide transistors (squares) and nitride transistors (circles). Vertical arrows indicate the zero-bias-anneal position. Figures in parentheses indicate the bias-anneal voltages.

photeric states. The conductance activation energy is a measure of the Fermi-level position at the gate insulator interface, under which the material has reequilibrated (a statistical shift has to be taken into account to give the true Fermi level). The figures in parentheses give the bias-anneal voltages. Positive and negative bias annealing of oxide transistors create more states, whereas negative bias annealing of nitride transistors *reduces* the integrated density of states. It is significant that the zero-bias integrated density of states is higher for the nitride transistor, yet by negative bias annealing, this can be reduced to a lower value than can be obtained on the transistor with a thermal oxide gate insulator.

Figure 8 shows the transfer characteristics for oxide and nitride transistors after various extreme bias-anneal voltages. For the oxide transistors there is an approximately symmetric shift of the threshold voltage with a clear increase or decrease in the prethreshold slopes. For the nitride transistor, negative bias annealing greatly reduces $V_T^e - V_T^h$, but the mean threshold voltage moves to a more negative value indicating some charge injection in the nitride as well. Nevertheless the hole threshold voltage still moves to a more positive value and the prethreshold slope $(dV_G/d \log_{10} I_{SD})$ is decreased.

Figure 9 shows the corresponding calculated energy-dependent densities of states. The field-effect analysis assumes a homogeneous density of states, but in reality the result represents an average density of states, which is weighted towards the interface and thus reflects the equilibrated density of states for the Fermi energy at the interface.[7]

Positive bias annealing increases the density of states in the lower part of the band gap and reduces the density of states in the upper part of the band gap. Negative bias annealing increases the density of states in the upper part of the band gap and reduces the density of states in the lower part. The overall effect depends on the initial starting condition and the new equilibrium Fermi energy. The low conductance activation energy at zero bias, for our nitride transistors, reflects the zero-bias electron accumulation layer in a-Si:H, which is present due to a positive fixed charge located in the silicon nitride. The reduction in the density of states for negative bias annealing simply reflects the reequilibration to a Fermi energy *nearer* to midgap.

In Fig. 7, we saw a similarity between the results for oxide and nitride transistors, when plotted against the conductance activation energy (a measure of the Fermi-level position). The difference in the absolute densities of states for the same Fermi-level position may reflect some real material differences in the structure of the a-Si:H
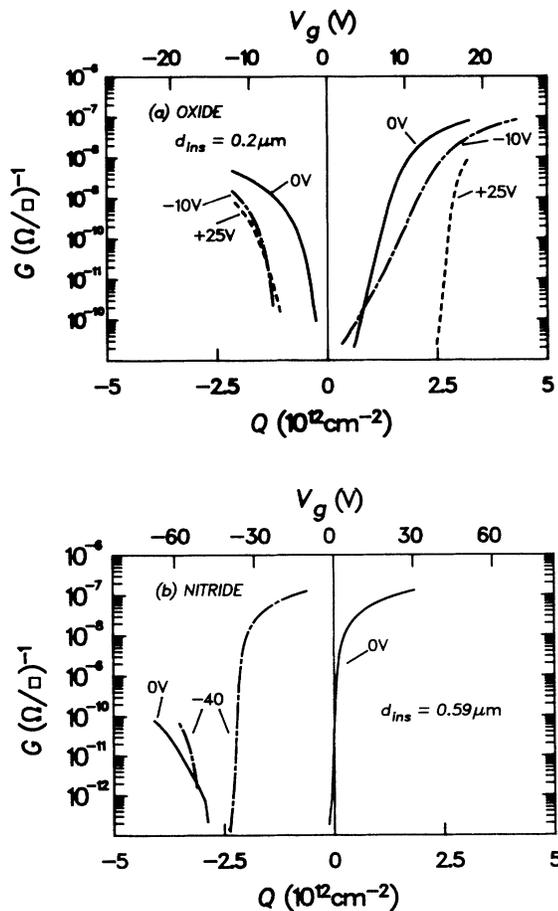
FIG. 8. Normalized transfer characteristics after bias annealing with various voltages for (a) oxide transistors and (b) nitride transistors. The curves are labeled by the bias-annealing voltage.
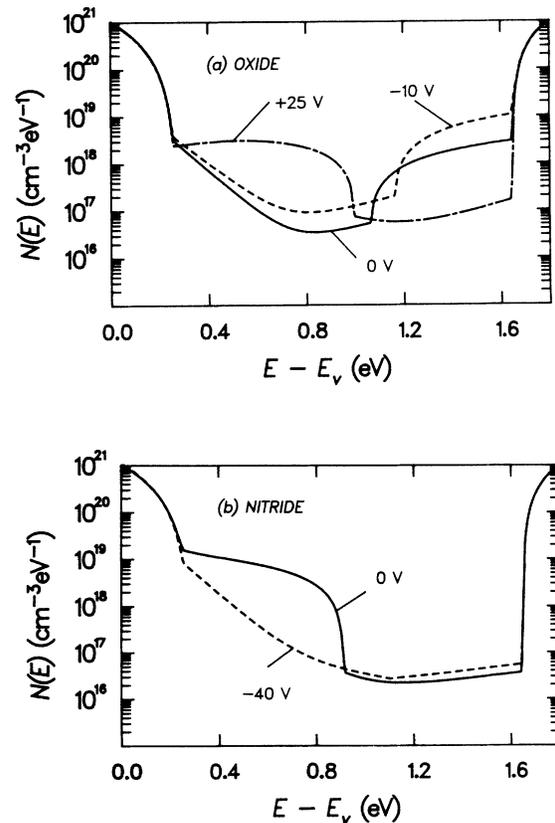
FIG. 9. The energy-dependent density of states after bias annealing with various voltages. The results are calculated from the transfer characteristics of Fig. 8: (a) oxide transistors, (b) nitride transistors.

near the interface. We are investigating this in a number of material systems and some preliminary results comparing different oxide transistors have been presented.[17] Further material systems are currently under investigation.

THE ROLE OF THE DEFECT POOL

In this section we discuss the physics of the state creation and state removal processes. We base our discussion on the model that the defects are all Si dangling bonds which are formed by the breaking of weak silicon-silicon bonds.[16,18] This may involve the diffusive motion of hydrogen,[8-10] although the specific microscopic mechanism is not essential to our discussion here.

The kinetics determining the rate of defect formation and the equilibrium defect densities can be understood with the aid of a configuration coordinate diagram such as that shown in Fig. 10. The weak bond state is converted to a dangling bond, which is either positively charged or negatively charged, depending on whether the states are created under electron or hole accumulation,

$$Si_4{}^0 + e \rightarrow Si_3{}^- , \tag{1}$$

$$Si_4{}^0 + h \rightarrow Si_3{}^+ . \tag{2}$$

The $Si_3{}^-$ and $Si_3{}^+$ states are the negatively and positively charged Si dangling-bond states, alternatively labeled D^- and D^+.

The diagram in Fig. 10 represents the situation for defects formed at a single energy under electron accumulation, i.e., with the Fermi level raised toward the conduction band. The barrier and formation energy for the D^+ state is higher than for the D^- state and, therefore, reaction (1) occurs. A separate diagram is needed for hole accumulation, when the barrier and formation energy is lower for the D^+ state and reaction (2) occurs.

The process during a bias-stress experiment is to convert weak bonds into dangling bonds by the above reactions. The rate of creation of dangling bonds depends on the density of weak-bond sites, the number of electrons, and the barrier to formation ϕ. We note that the density of dangling bonds is, in general, much less than the density of weak bonds, which can therefore be considered constant. The rate of formation does not depend on the formation energy E_{form}, since the bias used is large and the reverse transition rate is negligible in comparison. If there were a single value of ϕ for all sites, then the defect formation rate would be constant. Therefore, there must be a distribution of barrier heights, such that the sites with the lowest barriers convert first and as the stress time progresses, the barrier increases slightly, reducing the rate of defect formation.

The power-law time dependence observed experimentally in Fig. 6 is consistent with an exponential distribution of barrier heights.[9-11] The fact that β is different for the creation and reduction of dangling bonds implies that there is a different distribution of barriers for the forward and reverse reactions. However, the activation energy of the t_0 term is closely related to the maximum barrier accessible on the time scale of the experiment, which is similar for the forward and reverse reactions. We find the power β to increase with temperature, but it is not found to be proportional to absolute temperature as predicted for an exponential distribution of barrier heights.[10] For nitride transistors, β varies from 0.4 to 0.6 for temperatures increasing from 40 to 100 °C,[4] while for oxide transistors, we find β varies from 0.2 to 0.4 over a similar range, with the activation energy of the t_0 term again being about 0.9 eV. Further work is needed to properly account for the difference in β, while maintaining an apparently constant ϕ.

The process of bias annealing also interconverts weak bonds and dangling bonds. The key difference is that now the temperature is raised, increasing the rates of both the forward and reverse reactions. The equilibrium distribution depends on the formation energy E_{form}, but not on the barrier height ϕ. Only the time to reach equilibrium depends on the barrier height.

A crucial point, first pointed out by Bar-Yam and Joannopoulos,[19] is that the formation energy depends on the charge state of the defect and that the difference between the formation energy of a D^- or a D^+ state and a neutral defect depends on both the Fermi energy and the energy of the defect itself. These facts are the essential ingredients of the so-called defect-pool model.[20,21]

When a D^- state is formed, the defect formation energy is lowered from that a neutral defect by the energy of an electron falling from the Fermi level to the defect energy. When a D^+ state is formed, the formation energy is lowered by the energy of an electron falling from the defect to the Fermi energy. The difference in formation energy for a defect formed as a D^- or a D^+, at a *single* energy E^* for a given Fermi energy position (as in Fig. 10), is given by

$$\Delta E_{form} = 2(E_F - E^*) - U , \tag{3}$$

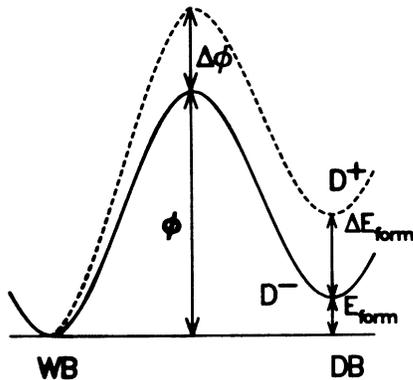where E_f is the Fermi energy, E^* is the defect energy,

FIG. 10. Energy configuration coordinate diagram indicating the interconversion of weak bonds (WB) and dangling bonds (DB). ϕ is the barrier to defect formation, E_{form} is the formation energy. $\Delta\phi$ and ΔE_{form} are the differences due to the charge state of the defects D^+ and D^-. $\Delta E_{form} = 2(E_F - E^*) - U$, where U is the correlation energy and E^* is the energy of the defect in the gap. ϕ and E_{form} also have a distribution of values over the different sites in the amorphous network.

POWELL, van BERKEL, FRANKLIN, DEANE, AND MILNE

i.e., the $+/0$ transition energy, and U is the correlation energy.[19]

If we identify the formation energy of the neutral defect with the one-electron energy difference between the valence-band states (the weak bonds) and the dangling-bond energy,[16,18] then the expressions for the formation energies of charged defects reduce to

$$E_{\text{form}}(D^+) = E_f - E_t , \tag{4}$$

$$E_{\text{form}}(D^-) = 2E^* - E_f + U - E_t , \tag{5}$$

where E_t is the valence-band energy.

If we now introduce the concept of a pool of potential defects, $P(E)$, which is the distribution of energies at which a defect could form, then the distribution of defects which are actually formed, $D(E)$, depends on the product of $P(E)$ and the probability of defect formation at an energy E.

$$D(E) = P(E)\exp(-E_{\text{form}}/kT^*) , \tag{6}$$

and there are separate contributions to $D(E)$ for each charge state. Because the formation energy for the D^- states depends on the energy of the defect, $D(E)$ for the D^- states has a peak which is shifted from the peak in $P(E)$. The peak for the D^+ states coincides with the peak in $P(E)$ at E_p, since the formation energy of the D^+ states does not depend on the defect energy. If $P(E)$ is taken to be a Gaussian, then Eq. (6) gives the product of a Gaussian and an exponential, which gives another Gaussian of the same width, but with the peak shifted. The energy shift of the peak in $D(E)$ for the D^- states is given by[19]

$$\Delta E = 2\sigma^2/kT^* - U , \tag{7}$$

where T^* is the equilibration temperature and σ is the width of the Gaussian distribution. Note that in the case of the D^- states, we have temporarily reverted to the notation that E is the energy of the $0/-$ transition, which is U higher in energy, than the $+/0$ transition.

If we associate the weak-bond energy with the specific valence-band tail states, which are exponentially distributed, then Eq. (6) is replaced by an integral over the tail states and the Boltzmann factor is replaced by a Fermi-Dirac-like distribution function.[20] Making the approximation, $E_0 > kT^*$, and because the integral of an exponential is also an exponential, this leads to expressions similar to Eqs. (6) and (7), with kT^* being replaced by E_0, the characteristic energy of the exponential tail-state distribution, and E_t replaced by $E_v = 0$. The density of states is still the product of a Gaussian and an exponential, leading to the same expression for the energy shift of the peak.[20]

In Fig. 11, we show the resulting density of states, calculated for each charge state. The coexistence of states formed in each charge state was pointed out by Schumm and Bauer.[22] In Fig. 11, we introduce the labeling of the states as D_e, for the states *formed* as D^-, under electron accumulation, and D_h, for the states *formed* as D^+, under hole accumulation. We also include in this figure the fact that some states can be formed *directly* as D_0,[20] here
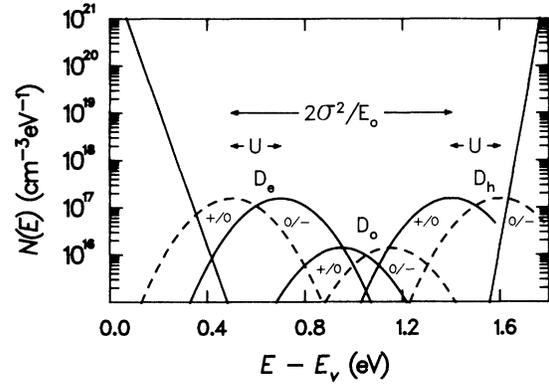

FIG. 11. The calculated density of states in a-Si:H. D_e, D_h, and D_0 are states initially *formed* as D^-, D^+, and D^0, respectively. States corresponding to the $+/0$ and $0/-$ transitions for each type of state are marked in each case. All states would be detected in any spectroscopy technique, like the field effect. The valence-band and conduction-band tail states are also indicated as exponential distributions. The valence-band tail corresponds to the E_0 used in the calculations.

labeled as D_0.

In this diagram, we also label all the states that would be detected in a field-effect experiment, i.e., each of the D_e, D_h, and D_0 states have $+/0$ and $0/-$ transition energies marking the position of the single- and double-occupancy levels, separated by U, all of which would be detected. Thus, for example, we can distinguish D_e^-, D_e^0, and D_e^+, being the different charge states of the D_e states. D_e^0 and D_e^+ are states which are formed as D_e^- states, but lose one or two electrons when the Fermi level is swept through them. We must remember that the states are frozen in on cooling and the shift of the Fermi level will not alter the density of states on the time sale of normal device operation at room temperature.

The correlation energy is positive for all states. The fact that the $D_e(0/-)$ energy is lower than the $D_h(+/0)$ energy results from the broad spread of possible dangling-bond energies. Physically we associate the different dangling-bond energies with different *sites* of the dangling bond and the spread in energies with the different local environments at each site. A D_e^- state becomes a D_e^+ when it loses two electrons, not a D_h^+, which is a different state at a different site.

In this picture, the density of states in a-Si:H is dominated by dangling bonds that are formed either as D_e states or as D_h states by one of the reactions (1) or (2). The additional states from the reaction that forms D_0 states directly,[20] are relatively fewer in number, even in undoped a-Si:H with the Fermi level near mid-gap.[22] In undoped a-Si:H there will, therefore, be substantial numbers of charged defects. We note, however, that some neutral defects come from D_e^0 and D_h^0 states and not just from D_0 states, while some D_0 states exist in their charged state (D_0^- or D_0^+).

In Fig. 12, we show the calculated effect of changing the Fermi level on the equilibrium density of states distribution. Lowering E_f leads to an exponential increase in

the density of D_h states and an exponential decrease in D_e states [Fig. 12(a)], whereas raising E_f does the opposite [Fig. 12(b)].

The energy position of the D_e and D_h states does not change. However, the nature and, hence, the energy position of the majority of the states changes from D_h to D_e as the Fermi level moves through the energy gap. Note that the directly formed D_0 states have a constant density. Refinements of the model to include the entropy considerations of specific microscopic mechanisms have been made, which affect the calculated absolute densities of states, but not the energy spectrum.[16,20,22] In fact, we used the full integral expressions with the entropy appropriate to one H atom involved in the microscopic mechanism,[20] in calculating the results in Figs. 11 and 12. However, this does not affect the spectral distribution or the relative magnitudes of each component in the density of states.

The results were obtained with $E_p = 1.4$ eV, $U = 0.2$ eV, $\sigma = 0.116$ eV, and $2\sigma^2/E_0 = 0.9$ eV, which were chosen to give the best fit to the experimental results. These values lead to an energy difference between the $D_e(0/-)$ and $D_h(+/0)$ peak positions of 0.7 eV, which
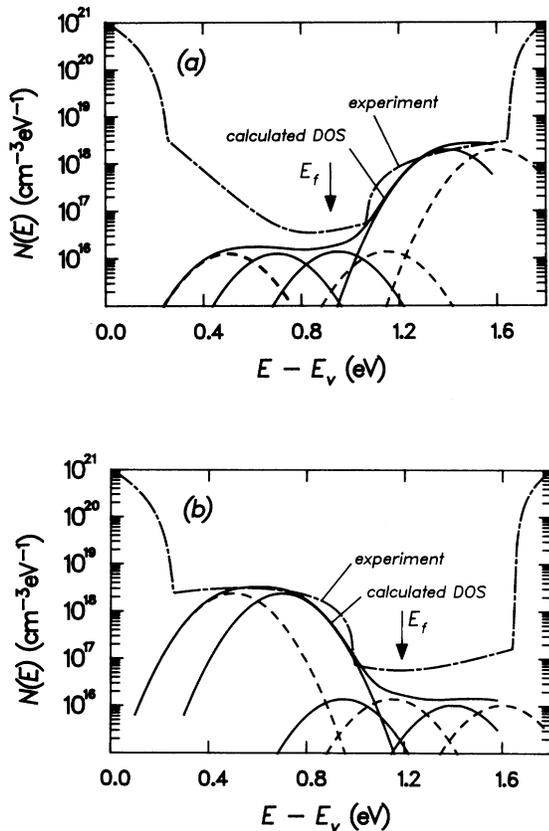

FIG. 12. The calculated effect of moving the Fermi level on the density of states, compared to experimental results. The latter are taken from the bias annealing of oxide transistors, from Fig. 9(a): (a) for zero bias anneal; and (b) for $+25$ V bias anneal.

is also in agreement with photoemission results.[23]

For undoped a-Si:H, the densities of D_e and D_h states are equal, while the density of D_e states exceeds the density of D_0 states, for any set of parameters that satisfy the inequality, $\sigma^2/E_0 > U$. Physically, this corresponds to the $D_e(0/-)$ energy being lower than the $D_0(+/0)$ energy. For the parameters used in our calculations, this energy separation is 0.25 eV and the D_e and D_h states dominate (Fig. 11). This conclusion is different from that stated by Winer,[20] but his analysis contained a slight error, which led to an underestimate of the density of D_e states. In fact, for the parameters used in his paper, the density of charged defects would also dominate in undoped a-Si:H.

Because of the energy separation of the D_e and D_h states, we can, to first order, identify all the states in the lower part of the gap as D_e states and all the states in the upper part of the gap as D_h states. This interesting result has great physical significance. It means that a dangling bond at a particular site with a particular energy will tend only to be formed either as a D_e (under electron accumulation) or as a D_h (under hole accumulation). In principle, a dangling bond at any energy could be formed as a D_e, D_0, or D_h state, but in practice only a few states near mid-gap can do this.

If we now compare the predictions of the defect-pool model with the experimental results (included in Fig. 12), then we can see that the key features are observed. The deep states are divided into two broad groups, one in the upper part of the gap and one in the lower part of the gap. We identify the states in the upper part of the gap as the D_h states and the states in the lower part of the gap as D_e states. The $+/0$ and $0/-$ states are not resolved with the parameters used in our calculations. We feel this does reflect the real situation, but in any case, the states are certainly not resolved by the field-effect technique.[13] Positive bias annealing increases the density of D_e states and decreases the density of D_h states. Negative bias annealing increases the density of D_h states and decreases the density of D_e states.

These experimental results give perhaps the best evidence for the validity of the defect-pool model for the Si dangling-bond defects in amorphous silicon. Furthermore, it shows that the vast majority of deep states in a-Si:H are part of this defect-pool and there is no distinction, for example, between metastable and stable defects. We suppose all dangling bonds have the same physical origin and are subject to the equilibration processes embodied in the defect-pool model.

Finally, there is an important point concerning the bias-stress experimental results. The results in Fig. 3 show that the energy of the created states is different for electron accumulation and for hole accumulation. It is important to remember that the rate of creating states in a bias-stress experiment does not depend on the formation energy, yet the results suggest that the created states can be divided into D_e and D_h distributions similar to the equilibrated density of states. This result is not obvious and it implies that the barrier to defect formation ϕ must depend on the charge state, the energy of the formed de-

fect E^*, and the weak-bond energy, in the same way as the formation energy itself.[24] This result has significance for the different possible microscopic mechanisms[9,11,25] and suggests that the barrier ϕ is associated with an elementary step involving the Si—Si weak bonds and resulting in the formation of a dangling-bond state.

OXIDE AND NITRIDE TRANSISTORS

The results presented in Fig. 7 show that there is a similar dependence in the density of states on the Fermi-level position in oxide and nitride transistors. There are two main differences between thermal oxide and nitride transistors. First, the Fermi level at zero bias is nearer to the conduction band in nitride transistors. This is a result of the finite band bending and electron accumulation layer at zero bias, due to a finite positive fixed charge in the nitride.[26] For thermal oxide transistors the Fermi energy at the interface is near midgap, with perhaps just a small electron depletion layer.[26] The second difference is that nitride transistors can show charge trapping in the nitride gate insulator, whereas no charge trapping has been detected in thermal oxide transistors.

The charge trapping is observed at high applied fields and we conclude that the mechanism for charge injection is by direct tunneling into defect states in the nitride or by tunneling into the silicon nitride conduction band, followed by trapping in the defect states, located in the nitride. These tunneling mechanisms account for the logarithmic time dependence and the temperature independence of the threshold voltage shift in this regime.[4] This charge trapping alters the density of charge in the nitride, which is not modified on the time scale of a field-effect experiment. This can therefore be regarded as fixed or quasifixed charge.

The density of states that is measured in an oxide or a nitride transistor reflects the thermal-equilibrium density of states to a particular Fermi energy position. In the case of nitride transistors, the band bending associated with the electron accumulation layer means that the separation of the Fermi energy from the conduction band varies continuously from the interface into the bulk a-Si:H, and so the equilibrium density of states will also vary. Thus the density of states is necessarily inhomogeneous.[7] In general, the measured density of states is dominated by the region with the higher density. This may, in part, explain the discrepancy between the measured and calculated densities of states in the low-density region. For example, the density of D_h states remains larger than that calculated when the Fermi level moves to higher energy. For extreme Fermi-energy positions, the density of one type of state is predicted to reduce to a very low value.[20]

The initial (as-grown) density of positive fixed charge in the nitride depends on the deposition conditions in the plasma-enhanced chemical-vapor deposition (PECVD) process. In our experience, this can vary, although there always seems to be a positive fixed charge in nitride transistors. Nitride transistors reported by other groups,

for example,[27] can apparently have lower fixed charges. The resulting equilibrium density of states then has a higher density of D_h states and a lower density of D_e states and the transistor characteristics can be closer to those of our oxide transistors. Similarly, we have been able to prepare oxide transistors with PECVD-deposited oxide layers that can be made to have variable fixed charges, from negative through to positive, causing electron depletion through to quite strong electron accumulation in the a-Si:H. The resulting transistor characteristics vary systematically in accord with our model. We therefore conclude that it is the magnitude and sign of the fixed charge that determines the density of states.

Charge trapping in the nitride dielectric, followed by zero-bias annealing, leads to a new equilibrium density of states. A fraction of the charge injected into the nitride under high field remains in the nitride after annealing and this causes the density of states to reequilibrate to a new Fermi energy.

Figure 13 shows the modification of our nitride transistors. Large negative bias stress, followed by zero-bias annealing, leads to positive charge trapping, an increase in the positive quasifixed charge density, and a new equilibrated density of states. The integrated density of states
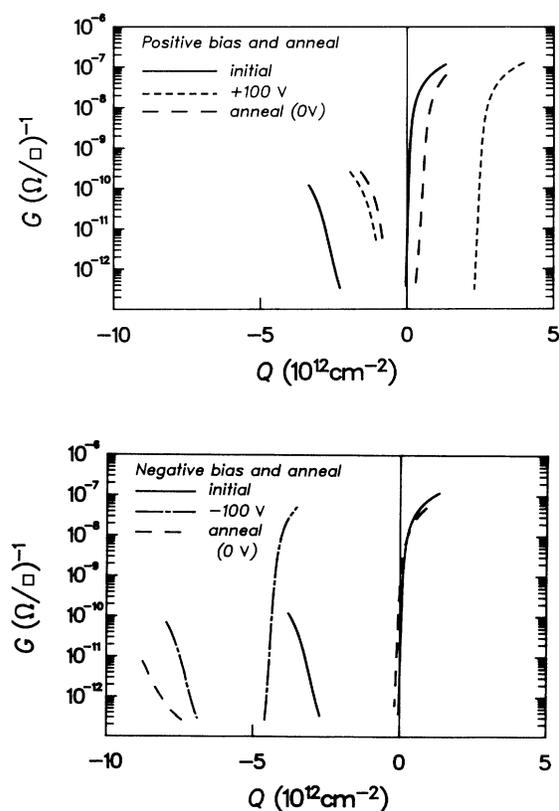

FIG. 13. The modification of nitride transistors by bias stress and annealing cycles: (a) solid line—initial characteristic; short dashed line—after $+100$ V, $t = 10^3$ s, positive bias stress; long dashed line—after subsequent zero-bias annealing; and (b) solid line—initial characteristic; chain line—after -100 V, $t = 10^3$ s, negative bias stress; long dashed line—after subsequent zero-bias annealing.

has increased (larger $V_T^e - V_T^h$) with more D_e and fewer D_h. Similarly, large positive bias stress followed by zero-bias annealing leads to a density of states with a decreased integrated density, with fewer D_e and more D_h, corresponding to a reduced positive fixed-charge density.

This interplay between the fixed charge in the gate insulator and the resulting equilibrium density of states gives us a means of optimization of transistor characteristics. Most current applications of a-Si:H TFT's use them as a simple switches, where we need a high on-off ratio for the lowest possible switching voltage. This means good n-channel transistors, with no hole conduction at moderate negative bias. For the lowest prethreshold slope ($dV_G/d \log_{10} I_{SD}$), we require a low density of D_h states and for the suppression of the hole conduction we require a large density of D_e states. A large equilibrium density of D_e states also makes the transistor more stable to subsequent positive bias-stress-induced-state creation.[24] These characteristics are ideally met by our nitride transistors, as deposited. However, in cases where the ideal characteristics are not met, as deposited, then a post-deposition cycle of bias stress and annealing can give improved transistor characteristics.

For example, in some transistors where there is unwanted hole conduction at negative gate biases, nega-

FIG. 14. The modification of the transfer characteristics of n-channel nitride transistors, by bias stress and annealing cycles: (a) $+100$ V positive bias stress followed by annealing, and (b) -100 V negative bias stress followed by zero-bias annealing (legend as in Fig. 13).

tive bias stress followed by zero-bias anneal causes the hole threshold voltage to be permanently shifted to a more negative value and the electron prethreshold slope is improved. Such procedures have been used in a real production process by a Japanese company, although we reveal here the underlying physical processes involved.

Figure 14 shows the modification of the characteristic of a single n-channel transistor, subjected to the same bias stress and annealing cycles as in Fig. 13. For transistors measured with $V_D = 15$ V, some finite hole conduction appears at negative bias, though V_T^h is displaced by the partially blocking contact. Nevertheless, the separation of V_T^e and V_T^h is reduced by positive bias stress followed by zero-bias anneal and increased by negative bias stress followed by zero-bias anneal, as observed in the separate n-channel and p-channel results in Fig. 13.

SUMMARY

We have shown how the threshold voltage shift that is observed in amorphous-silicon thin-film transistors is related to the creation and reduction of dangling-bond states in the amorphous silicon. The process can be understood in terms of a defect-pool model, involving a pool of potential dangling-bond states with a spread of energies, which extends across the entire band gap.

The displacement of the Fermi level toward the conduction band leads to the increase in density of dangling-bond states in the lower part of the band gap and the reduction of states in the upper part of the band gap. The displacement of the Fermi level toward the valence band leads to the increase in the density of states in the upper part of the gap and a decrease in the density of states in the lower part of the gap. The overall net effect depends on the initial starting conditions.

We label the states low in the gap as D_e states (formed under electron accumulation) and the states in the upper part of the gap as D_h states (formed under hole accumulation). This result is consistent with the defect-pool model for Si dangling-bond states and is a direct result of the defect formation energy being dependent on the defect energy itself, which has a spread of values due to disorder.

Bias annealing leads to the complete thermal reequilibration of the density of states to the new Fermi-energy position. Bias stress at room temperature leads to the creation of one type of defect and the removal of the other type at a rate determined by the barrier height and the density of the starting species. The fact that the energy separation of the D_e and D_h states is maintained in a bias-stress experiment means that the barrier to defect formation also depends on the defect energy in the same way as the formation energy.

The initial density of states measured in an a-Si:H TFT depends on the Fermi energy position at the gate-insulator interface and thus depends on the insulator fixed charge. For oxide transistors the Fermi level is near to midgap. Positive and negative bias stress and bias annealing lead to an overall increase in the density of states. Nitride transistors have electron accumulation at zero
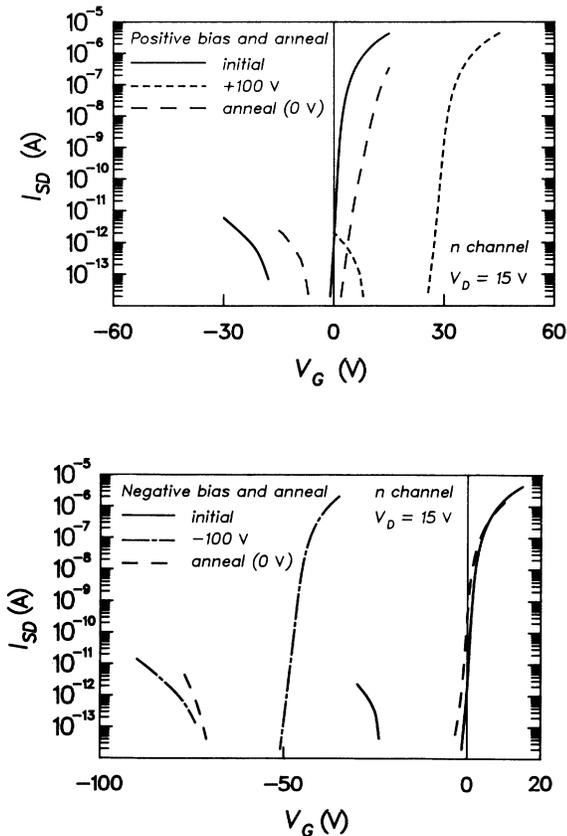
bias, and this leads to different behavior. Positive bias stress still leads to state creation, but negative bias stress and negative bias annealing both lead to an overall reduction in the density of dangling-bond states.

For nitride transistors, we can get charge trapping in the nitride, at high fields. Subsequent zero-bias annealing leads to reequilibration to a new density of states, with a certain fraction of the injected charge remaining in the nitride. This procedure can be used to optimize nitride transistor characteristics.

ACKNOWLEDGMENTS

[1]M. J. Powell, Appl. Phys. Lett. **43**, 597 (1983).

[2]C. van Berkel and M. J. Powell, Appl. Phys. Lett. **51**, 1094 (1987).

[3]M. J. Powell, C. van Berkel, I. D. French, and D. H. Nicholls, Appl. Phys. Lett. **51**, 1242 (1987).

[4]M. J. Powell, C. van Berkel, and J. R. Hughes, Appl. Phys. Lett. **54**, 1323 (1989).

[5]M. J. Powell, I. D. French, and J. R. Hughes, J. Non-Cryst. Solids **114**, 642 (1989).

[6]S. C. Deane, M. J. Powell, J. R. Hughs, I. D. French, and W. I. Milne, Appl. Phys. Lett. **57**, 1416 (1990).

[7]M. J. Powell, S. C. Deane, I. D. French, J. R. Hughes, and W. I. Milne, Philos. Mag. B **63**, 325 (1991).

[8]W. B. Jackson, J. M. Marshall, and M. D. Moyer, Phys. Rev. B **39**, 1164 (1989).

[9]W. B. Jackson, Phys. Rev. B **41**, 1059 (1990).

[10]J. Kakalios, W. B. Jackson, and R. A. Street, Phys. Rev. Lett. **59**, 1037 (1987).

[11]R. S. Crandall, Phys. Rev. B **43**, 4057 (1991).

[12]A. V. Gelatos and J. Kanicki, Appl. Phys. Lett. **57**, 1197 (1990).

[13]M. J. Powell, Philos. Mag. B **43**, 93 (1981).

[14]R. E. I. Schropp and J. F. Verwey, in *Amorphous Silicon Semiconductors Pure and Hydrogenated,* edited by A. Madan, M. Thompson, D. Adler, and Y. Hamakawa, MRS Symposia Proceedings No. 95 (Materials Research Society, Pittsburgh, 1987), p. 489.

[15]R. A. Street, J. Kakalios, C. C. Tsai, and T. M. Hayes, Phys.

Rev. B **35**, 1316 (1987).

[16]R. A. Street and K. Winer, Phys. Rev. B **40**, 6236 (1989).

[17]S. C. Deane, W. I. Milne, M. J. Powell, J. R. Hughes, and I. D. French, Extended Abstracts of the 22nd International Conference on Solid State Devices and Materials, Sendai (Japan Society of Applied Physics, Tokyo, 1990), p. 1031.

[18]M. Stutzmann, Philos. Mag. B **56**, 63 (1987).

[19]Y. Bar-Yam and J. D. Joannopoulos, J. Non-Cryst. Solids **97-98**, 467 (1987).

[20]K. Winer, Phys. Rev. B **41**, 12150 (1990).

[21]Z. E. Smith and S. Wagner, Amorphous Silicon and Related Materials, edited by H. Fritzsche (World Scientific, Singapore, 1989).

[22]G. Schumm and G. H. Bauer, Philos. Mag. B **64**, 515 (1991).

[23]K. Winer, I. Hirabayashi, and L. Ley, Phys. Rev. B **38**, 7680 (1988).

[24]S. C. Deane, W. I. Milne, and M. J. Powell, in *Amorphous Silicon Technology—1991,* edited by A. Madan, Y. Hamakawa, M. Thompson, P. Taylor, and P. LeCombes, MRS Symposia Proceedings No. 219 (Materials Research Society, Pittsburgh, 1991), p. 333.

[25]S. B. Zhang, W. B. Jackson, and D. J. Chadi, Phys. Rev. Lett. **65**, 2575 (1990).

[26]C. van Berkel, *Properties of Amorphous Silicon* (INSPEC, London, 1989), pp. 531 and 534.

[27]G. Fortunato, L. Mariucci, C. Reita, and P. Foglietti, IEEE Trans. Electron Dev. **ED-36**, 2825 (1989).