Atomic-step rearrangement on Si(100) by interaction with arsenic and the implication for GaAs-on-Si epitaxy

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The lowest-energy configuration of a class of vicinal Si(100) surfaces has equally spaced steps, each with a height of two atomic units. This results in a single-domain surface with the surface Si-Si dimers being aligned parallel to the step edges. The interaction of As with vicinal Si(100) surfaces is crucial for GaAs growth on Si and there have been several studies of this system, but results from several groups appear to be in contradiction. The results described here, which combine scanning tunneling microscopy, low-energy electron diffraction, and x-ray photoemission, yield a consistent picture of the interaction of As with vicinal Si(100). It is found that depending on the time order of (i) exposure to As and (ii) raising the surface temperature, the directions of the As-As dimers can reproducibly be made perpendicular or parallel to the step edge. In the latter case the step array on the Si substrate is completely rearranged. GaAs grown on one type of dimer arrangement is controllably oriented 90° with respect to that on the other type.

INTRODUCTION

The structures of clean Si and Ge surfaces are dominated by surface reconstructions that take place primarily in order to reduce the number of Si dangling bonds. Arsenic atoms can strongly interact with these surfaces because the extra valence electron on each As atom can replace dangling bonds with lower-energy doubly occupied lone-pair orbitals.[1] This effect causes removal of the reconstruction or alteration of the reconstruction geometry and also leads to strong passivation of the surface. On large terraces of Si(100), the Si-Si dimers of the clean surface reconstruction are broken and a monolayer of symmetric As-As dimers is simply added to the surface.[2] The effect is more complex in the case of As interaction with the Si(111) 7×7 surface, where there is significant movement of Si atoms within the first three atomic layers to allow a single monolayer of As atoms with a 1×1 symmetry to form the outermost layer.[3–6] In this paper we address the situation of As interaction with vicinal or off-axis Si(100) surfaces.

A silicon surface with its surface normal a few degrees away from [100] towards the [011] direction will consist of (100) terraces arranged in a staircase fashion. Usually, the step heights are one atomic layer high and thus each successive terrace will have its Si-Si dimer direction rotated by 90°, as shown in Fig. 1(a). By suitable preparation techniques and for sufficiently large offcut angles, it is possible to prepare surfaces that have step heights that are predominantly two atomic layers high (see Refs. 7–9, for example) with the majority of the terraces having their Si-Si dimers aligned parallel to the step edges, as shown schematically in Fig. 1(b). This occurs because the energy of a double step with this geometry is lower than the sum of the single height steps with dimers parallel and perpendicular to step edges that it replaces.[8] The low-energy electron diffraction (LEED) or reflected high-energy electron diffraction (RHEED) pattern of these surfaces shows a predominance of half-order spots along $[01\bar{1}]$. It is the interaction of As with these "single-domain" vicinal surfaces that is of interest here. The first study[10] showed that after interaction with As, the As-As dimer direction became perpendicular to the step edges, as shown in Fig. 1(c) (we denote this as the $As_\perp$ orientation), and thus the As atoms added to the surface in the same way as they do on on-axis Si(100) surfaces. Several subsequent studies[11–15] showed results indicating that it was possible to create surfaces with As-As dimers oriented parallel to the step edges, as shown in Fig. 1(d) (we denote this as the $As_\parallel$ orientation). As the following summary shows, many of these results were apparently contradictory and it was not clear under what situations surfaces could be made reproducibly with the $As_\parallel$ or $As_\perp$ orientations.

In experiments carried out on bare, single-domain Si(100) where As_4 exposures were made at a substrate temperature T_e and then measurements were made after the samples were cooled back to room temperature, Kawabe *et al.*[11] found the $As_\parallel$ orientation for T_e below 500 °C and $As_\perp$ for temperatures above 500 °C. With a similar experimental sequence, Becker *et al.*[13] found an apparently opposite sequence with $As_\perp$ at $T_e=400$ °C, $As_\parallel$ at 600 °C, and mixed domains and surface faceting at 700 °C. Uneta *et al.*[16] also found the $As_\perp$ orientation for $T_e=200$ °C in contradiction with the results of Kawabe *et al.*[11] Experiments carried out at temperature on single-domain Si(100) by Varrio *et al.*[14] showed that the $As_\parallel$ orientation occurred for temperatures below 600 °C and $As_\perp$ for temperatures above 650 °C. In contrast, the results of Ohno and Williams[15] for measurements made at temperature with As_2 exposure of single-domain Si(100) showed $As_\perp$ for T_e less than about 750 °C and the appearance of facets at temperatures between 600 °C and 800 °C. This latter result is consistent with the results of Pukite and Cohen[12] on vicinal Si(100) surfaces that were not originally single domain.

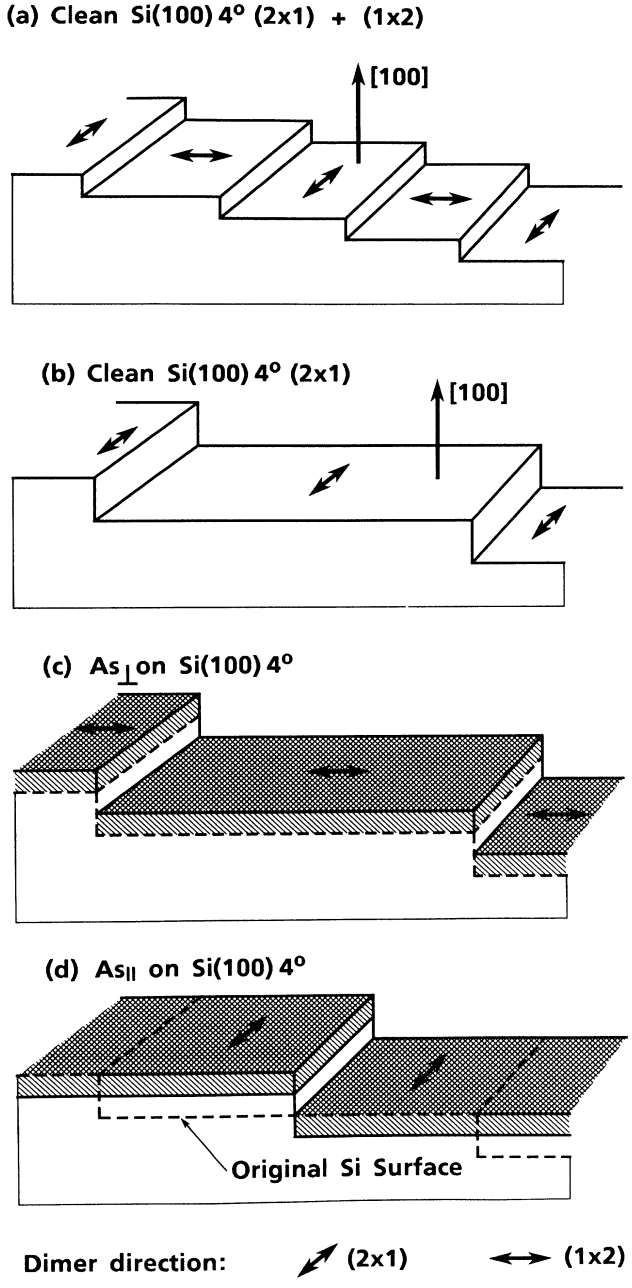

FIG. 1. Schematic drawing of step structures for vicinal Si(100) surfaces which have their surface normal a few degrees away from [100] towards the [011] direction. An array of single-height steps is shown in (a) and successive terraces have Si-Si dimers arranged parallel and then perpendicular to the step edge. Under suitable conditions, the arrangement in (a) can be replaced by the lower-energy structure in (b) in which all steps are two atomic layers high and all Si-Si dimers have the same orientation (single-domain surface). The addition of arsenic to the single-domain surface results in a coverage of a single monolayer of As-As dimers. As discussed in the text, the orientation of these dimers is found to be perpendicular to the step edge, as shown in (c), or parallel to the step edge, as shown in (d). In the latter case, some of the Si atoms in the substrate must move laterally.

In the present paper we describe a detailed investigation of the interaction of As with vicinal surfaces. The results provide us with new insight into the interaction of atoms with semiconductor surfaces. The results are also important for the understanding of heteroepitaxial growth on Si which is commonly carried out on vicinal Si(100) surfaces. In particular, the first stage in molecular-beam-epitaxy (MBE) growth of GaAs on Si is the interaction of As atoms with the substrate. Variations in the quality and orientation of GaAs grown on Si have been found to occur with different treatments of the first stage of the growth (see Refs. 11, 12, 14, and 17–19, for example). We will describe how the atomic structure of the As atoms relative to the steps on vicinal Si(100) influences the way that GaAs grows on these substrates. Specific procedures for initiating single-domain growth are then provided.

I. EXPERIMENTAL DETAILS

Samples were cut from Si wafers (n type, 0.01 Ω cm) that had their surface normals oriented at an angle ϕ from the [100] direction towards [011]. For most of the results presented here, ϕ was 4°, but results obtained with $\phi=2°$ will also be described. Unless stated otherwise explicitly, the offcut angle should be taken to be 4°. The samples were cleaned by standard solvent and acid dips and oxidized with a uv-ozone technique.[20] After introduction into the ultrahigh-vacuum (UHV) environment, they were outgassed for several hours by resistively heating to 600 °C and then the oxide layer was removed and double-step formation was induced by annealing to 1030 °C for 2 min. Arsenic exposures were made using an As_4 source in an MBE chamber which has cryopumping and cryoshrouding. Temperatures during the exposure and any subsequent annealing were controlled with a silicon optical pyrometer. After arsenic exposure, samples were then transferred through an intermediate chamber held at pressures below 5×10^{-10} Torr to either a scanning-tunneling-microscope (STM) chamber or to an analysis chamber containing LEED and x-ray photoemission (XPS) systems.

LEED patterns were recorded photographically from a rear-view LEED system and the relative intensities of the diffracted spots were determined from the photographs using a digitized charge-coupled device camera. The $I[(2\times1)]/I[(1\times2)]$ ratios were determined by taking intensity ratios of adjacent half-order spots. The electronic aperture was set to integrate entire spots, and the background intensity to be subtracted from these spots was determined by integrating intensity within the same aperture after it had been translated to the midpoint between the two LEED spots to be compared. It was found to be most reliable to avoid the $\{0,\frac{1}{2}\}$ family of spots which are near the bright (0,0) beam and so the following four intensity ratios were measured: $I[(\frac{1}{2},1)]/I[(1,\frac{1}{2})]$, $I[(-\frac{1}{2},1)]/I(-1,\frac{1}{2})]$, $I[(-\frac{1}{2},-1)]/I[(-1,-\frac{1}{2})]$, and $I[(\frac{1}{2},-1)]/I[(1,-\frac{1}{2})]$. The geometrical mean of these ratios was taken to be the measure of the $I[(2\times1)]/I[(1\times2)]$ asymmetry. Using this method, clean Si(100)4° surfaces were found to be predominantly

single domain, with an anisotropy factor of around 5 and with Si-Si dimers aligned parallel to the step edges. It should be noted that the ratio estimated by eye tends to be considerably greater than that which is measured.

XPS measurements were carried out with a cylindrical mirror analyzer using Mg $K\alpha$ excitation. The intensities of the As $3d$ and Si $2p$ core levels were obtained by integrating the area under their respective photoemission peaks.

II. RESULTS

Previous results for As interaction with vicinal Si(100) surfaces have given a variety of results, many of them apparently contradictory. As a result, we have attempted to carry out exposures with a range of parameters, but, more importantly, with a number of distinctly different methods. The four main methods (shown schematically in Fig. 2) are the following.

(a) Raising the substrate temperature from room temperature (RT) to a fixed temperature T_e, holding at this temperature for a fixed time t_e, and then dropping the temperature back to RT. This is done with a constant As_4 pressure P_{As}.

(b) Holding the substrate temperature at a fixed value T_e while the As_4 pressure is brought from the base pressure up to a fixed pressure P_{As}, holding at this temperature for a fixed time t_e, and then dropping the temperature to RT.

(c) Dropping the substrate temperature from a high temperature T_h to a fixed temperature T_e, holding at this temperature for a fixed time t_e, and then dropping the temperature to RT. This is done with a constant As_4 pressure P_{As}.

(d) Carrying out an As_4 exposure at room temperature and then annealing the surface in vacuum at a temperature T_{ann}.

Most of the experiments on the interaction of As with vicinal Si(100) surfaces, and the first stage of GaAs growth on Si using MBE, use one of these four methods. As we will describe in detail in the remainder of this section, examining the effects of these different methods has allowed us to find ways to obtain surfaces reproducibly with either the $As_{\parallel}$ or $As_{\perp}$ orientations.

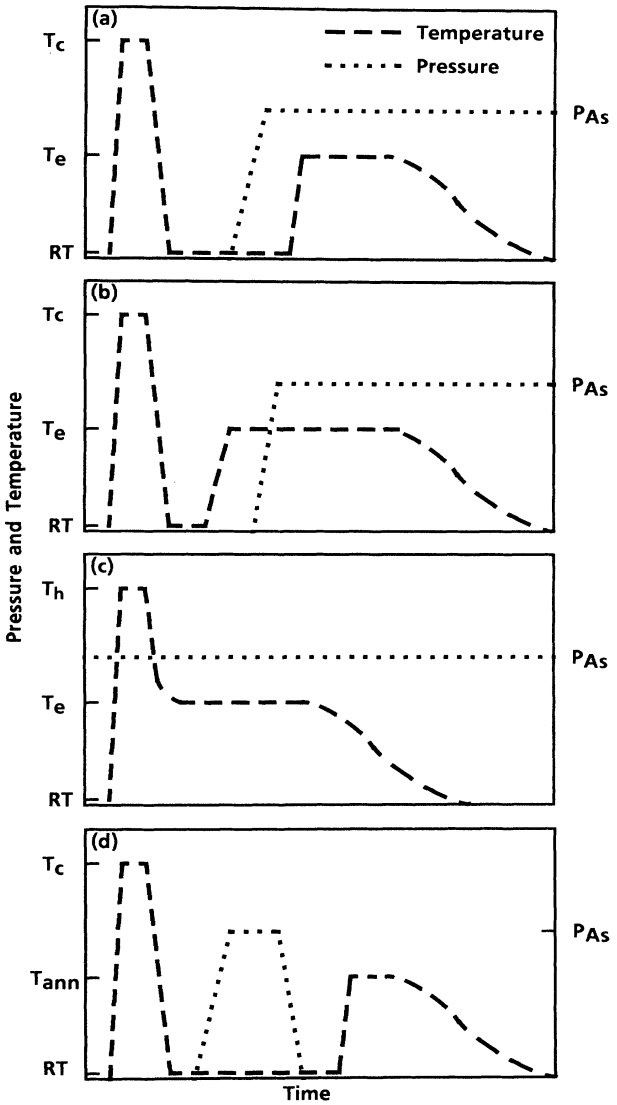

FIG. 2. Schematic illustration of the four main preparation methods for the Si(100):As4° surfaces. The substrate temperature and As_4 partial pressure are shown on an arbitrary scale as a function of time. For completeness, in (a), (b), and (d) we also show the cleaning step which consists of annealing the sample at a temperature T_c (usually 1030 °C).

A. Method (a): Substrate temperature raised in fixed As_4 flux

After the Si(100)4° sample was cleaned, it was examined with LEED to check that the surface was indeed predominantly single domain with Si-Si dimers aligned parallel to the step edges. The sample was then moved into the MBE chamber, the As_4 source was turned on, and once the system reached its intended ambient pressure of 10^{-6} Torr, the sample temperature was raised to the exposure temperature T_e at a rate of $\sim 5-10$ K/sec and held for a fixed time t_e. At the end of this time, the sample temperature was dropped to RT and then the As_4 source was turned off. We estimate that the effective pressure in the As_4 beam at the sample was $\sim 10^{-5}$ Torr during the exposures. After the ambient pressure dropped to around 10^{-8} Torr, the sample was annealed at 300 °C for 2 min to remove any loosely bound As on the surface, and quickly transferred out of the MBE chamber. LEED patterns and XPS spectra were recorded for each exposure. Experiments were carried out for a range of exposure temperatures and a variety of exposure times.

In all cases it was found that the As-As dimers added to the surface in predominantly the $As_{\perp}$ orientation. The quantitative LEED anisotropies (shown as ×'s in Fig. 3) were greatest for T_e in the range 650 °C to 750 °C where the $I[(2\times1)]/I[(1\times2)]$ ratios were close to $\frac{1}{10}$. The LEED patterns for both the clean Si(100)4° samples and

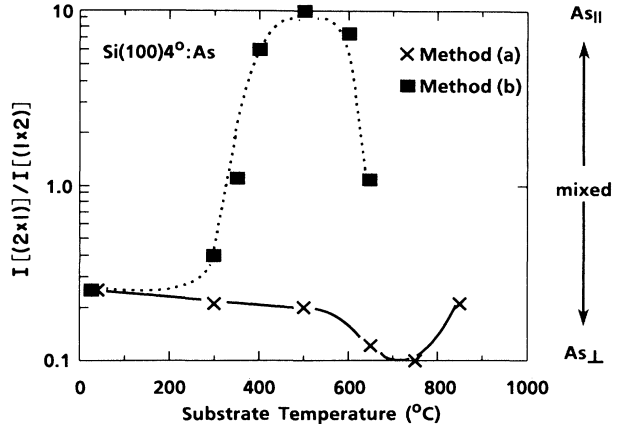

FIG. 3. Intensity ratio of the $I[(2\times1)]$ to the $I[(1\times2)]$ LEED spots for As exposure methods (a) and (b) as a function of exposure temperature T_e.

those produced using this method showed clear spot splittings for all of the integral and half-order spots in a number of ranges of the electron energy. In general, the sharpness of the spots improved when the measured asymmetry increased. The quantitative measurement of the LEED anisotropies was carried out at 55 eV, where the $\{0,1\}$ family of spots showed clear splittings corresponding to the separation between double-height steps. The LEED ratios were not found to be sensitive to the choice of electron energy used. The I(As $3d$)/I(Si $2p$) XPS core-level ratios measured on the same samples are shown in Fig. 4. A small decrease in the total As coverage can be seen as T_e increases, but the deviation from uniform composition (shown by the dotted line) is small for $T_e \geq 500\,^{\circ}\mathrm{C}$. The XPS ratio was found to be independent of t_e to within 2% for times between 5 sec and 5 min.

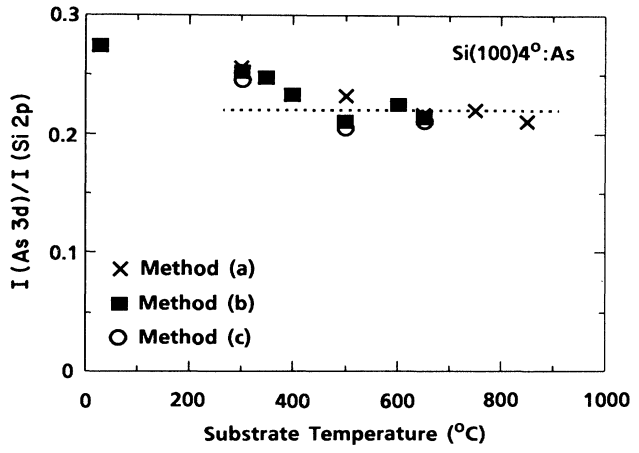

FIG. 4. The I(As $3d$)/I(Si $2p$) core-level ratios from an XPS measurement using Mg $K\alpha$ excitation. The data are shown for As exposure methods (a)–(c). The data for method (d) are not plotted, but are within 5% of those shown for temperatures $\leq 600\,^{\circ}\mathrm{C}$. The dotted line is a guide for the eye and has zero slope.

An STM image from a sample prepared in this way is shown in Fig. 5(a). The As-As dimers are visible as long rows which can be seen to lie parallel to the steps, which have smooth edges. Also visible are a small number of rows at right angles to the step edges, and two deep channels. The rows at right angles occur because of the presence of a small number of single-height steps and the channels occur at phase boundaries where the As-As dimers are offset by one surface lattice constant. It is most likely that the overlayer has nucleated at several different points. Where the domains meet, relatively straight phase boundaries are formed.

B. Method (b): As_4 flux raised with substrate temperature fixed

Whereas method (a) allows the *first* As atoms to impinge on the Si surface while it is at RT, method (b) only allows As atoms onto the surface after the surface has reached an elevated set temperature. After the clean sample was moved into the MBE chamber, its temperature was quickly raised to the fixed temperature T_e while the background As_4 pressure was kept below 2×10^{-9} Torr. The As_4 pressure was then increased from the background pressure up to an ambient pressure of 10^{-6} Torr, corresponding to a beam pressure of around 10^{-5} Torr at the sample surface. After an exposure time of typically 5 min, the sample was cooled in the As_4 ambient. A 2-min anneal at 300 °C was carried out after the ambient pressure dropped to around 10^{-8} Torr and then the sample was transferred out of the MBE chamber.

With this treatment we found that As-As dimers could be added to the surface with an orientation which was predominantly $As_{\parallel}$ for substrate temperatures T_e in the range 400 °C to 600 °C. The LEED anisotropy in this range was found to be close to 10 to 1 (Fig. 3). As was the case for method (a), the $\{0,1\}$ LEED spots were split by an amount consistent with the surface having predominantly double-atomic-height steps.

In the absence of any change to the step arrangement in the underlying substrate, the only possibilities for the As orientation are 0 or 2 monolayers. The XPS intensity ratios shown in Fig. 4, however, show that the As coverage is nearly identical to that obtained for surfaces with the $As_{\perp}$ orientation described in Sec. II A. This is strong evidence that the substrate step structure has been rearranged by the interaction with As.

An STM image from a sample prepared in this way is shown in Fig. 5(b). The As-As dimers are visible as rows which can be seen to lie perpendicular to the step edges. In contrast to the $As_{\perp}$ image, that for $As_{\parallel}$ has step edges which are not smooth. In addition, there is evidence that the double-height steps consist of very closely spaced single steps in some cases.

We note that above 600 °C, the asymmetry reverts to the $As_{\perp}$ orientation. We also point out that, as will be shown in Sec. II D, As atoms do not stick effectively to the surface for T_e above around 650 °C, so that method

(b) cannot be carried out for temperatures much above this value.

C. Method (c): Substrate temperature lowered in fixed As_4 flux

For GaAs growth on Si using MBE, a variety of techniques are used to begin the growth. One of these removes the initial oxide layer on the Si substrate by annealing to temperatures of the order of 1000 °C in the presence of an As_4 partial pressure (either molecular beam or ambient) and then lowering the substrate temperature before beginning growth. Because this technique is fairly widely used, we investigated the effect of this treatment on the orientation of As-As dimers on the surface. We were able to obtain either the $As_{\parallel}$ or $As_{\perp}$

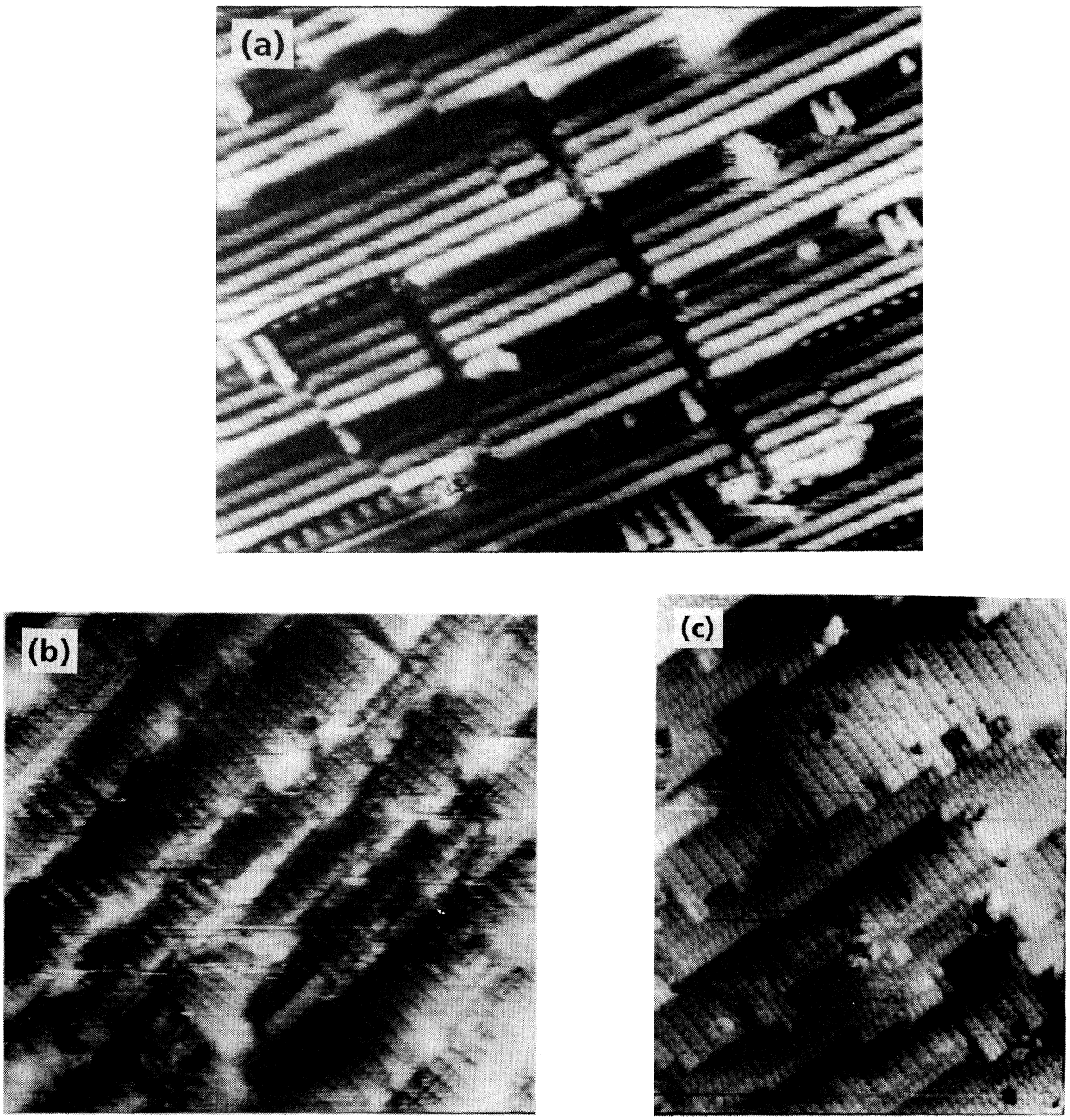

FIG. 5. STM constant-current images of Si(100)4°:As showing tunneling from filled states for (a), method (a) with $T_e = 650$ °C; (b) method (b) with $T_e = 500$ °C, and (c) method (c) with $T_e = 850$ °C. The tunneling current was 100 pA in all cases and the sample bias was −1.5, −2, and −2 V for (a), (b), and (c), respectively. The dimer rows are 0.76 nm apart and the image widths are 25, 24, and 18 nm for (a), (b), and (c), respectively.

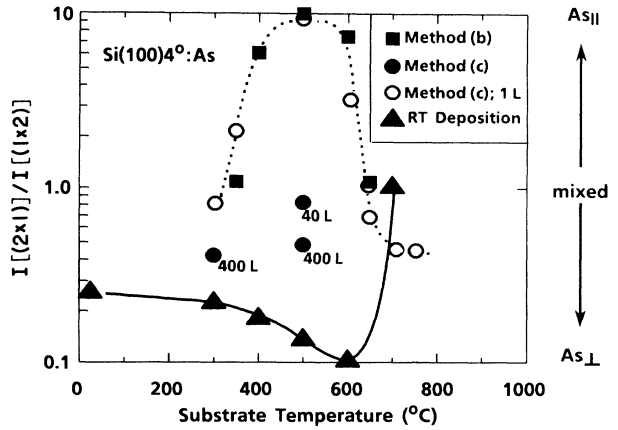

FIG. 6. Intensity ratio of the $I[(2\times1)]$ to the $I[(1\times2)]$ LEED spots for As exposure methods (b) and (c) as a function of exposure temperature T_e and for method (d) as a function of annealing temperature. Data for method (c) are shown as open circles for the case in which exposure during cooldown from T_h to T_e was ≤ 1 L and can be seen to be similar to those from method (b).

orientations, depending on the total As_4 dosage and cooling rate as the substrate was cooled from the cleaning temperature of 1030 °C to the exposure temperature T_e. For doses of less than about 1 langmuir (1 L$=10^{-6}$ Torr sec) during the cooldown, we obtained the same result as method (b), that is, $As_{\parallel}$ for T_e in the range 400 °C–600 °C and mixed or $As_{\perp}$ orientations for T_e outside this range. This can be seen in Fig. 6 where data for exposures of 1 L during cooldown are compared directly with the results of method (b). For exposures of more than about 10 L during the cooldown, we find an increasing fraction of $As_{\perp}$, as summarized in Fig. 6. The combination of these results indicates that for exposures of less than around 1 L during the cooldown from T_h to T_e, the As atoms do not disrupt the surface. The final surface structure in this case is thus the same as that obtained when bringing the surface to a temperature of T_e in the absence of any As_4.

D. Method (d): Room temperature deposition and annealing

A slightly different set of experiments was carried out by making an exposure at RT and then annealing the sample in a sequence of higher temperatures. The asymmetry data corresponding to this method are shown in Fig. 6 as a function of annealing temperature. The magnitude of the asymmetry reaches a maximum at 600 °C before decreasing. XPS measurements of the I(As $3d$)/I(Si $2p$) core-level ratio showed a gradual decrease to 600 °C, a sharp decrease at 700 °C, and no detectable As signal after annealing at 750 °C. For annealing temperatures in the range 300 °C–600 °C, the core-level ratios were the same as those for method (a) to within about 5%. These results show that the maximum asymmetry comes at the temperature at which As begins to desorb from the surface. The XPS results described above (but not shown in Fig. 4) indicate that this occurs at 600 °C in vacuum. Comparison with the data for method (a) in Fig. 3 suggests that the same effect may occur at around 700 °C in the presence of the As_4 flux used for those experiments. Although method (d) appears to give the same asymmetry as method (b), we do not expect the quality of the surface to be as good. We have found previously[21] that the surface states measured with angle-resolved photoemission are sharper and stronger for method (b) than for method (d) and the core-level peak shapes measured with photoemission are better defined for method (b). It is likely that this is due to a loss of As atoms in method (d) as the ordering on the surface improves. In method (b), on the other hand, As atoms are being continually supplied so that ordering can occur without a net loss of As from the surface.

E. GaAs on Si

GaAs films were grown on surfaces with well-established $As_{\perp}$ and $As_{\parallel}$ structures. The GaAs-on-Si layer was prepared with the standard two-step method in which a GaAs buffer layer was grown at 400 °C and the remainder of the film was grown at 600 °C. The $As_{\perp}$ structure was obtained with method (a) at $T_e=650$ °C and the $As_{\parallel}$ structure was obtained with method (b) at $T_e=500$ °C. After a film thickness of the order of 200 nm, the LEED patterns of the GaAs were observed. The $c(2\times8)$ reconstruction of GaAs(100) was observed in each case, with the $2\times$ direction being parallel to the step edge for the $As_{\parallel}$ initial surface and perpendicular to it for the $As_{\perp}$ initial surface. The $2\times$ direction for the GaAs(100) $c(2\times8)$ reconstruction is the As-As dimer direction on that surface.[22] This means that the As monolayer on the original As-terminated surfaces set the As sublattice site for the overgrowing crystal in each case. (This result was reproduced for films thicker than one micrometer grown with the standard two-step GaAs-on-Si method, where the orientations of the GaAs overlayers were determined by chemical etching experiments.) Dependence of the GaAs orientation on the substrate preparation method has been seen previously, but has not been as clearly related to the structure of the As-terminated surface. Kawabe *et al.*[11] found that the GaAs orientation depended on whether they grew on $As_{\parallel}$ or $As_{\perp}$, but as is discussed below, the conditions that they found necessary to obtain $As_{\parallel}$ and $As_{\perp}$ seem to be in contradiction with the results of our work and that of others. Fischer *et al.*[17] and Won *et al.*[19] found that the GaAs orientation could be altered by the use of a Ga prelayer. The present results, however, and the fact that As can displace Ga on the Si surface,[18] may indicate that the differing thermal treatments for the Ga and As prelayers which were used in Refs. 17 and 19 affected the way that As bonded to the Si substrate instead of changing the atomic species at the interface. Finally, for GaAs growth on double-domain Ge(100)6°, Pukite and Cohen[23] found that the use of As_2 or As_4 gave rise to different GaAs orientations despite the fact that both As-terminated surfaces had a combination of triple- and single-height steps

and were indistinguishable in RHEED. Our results suggest that some type of step motion may have occurred in this case also.

It should be noted that the absence of single-height steps is not necessary to obtain anti-phase-domain-free GaAs on Si.[14,24,25] Kawabe and Ueda[25] have described a mechanism in which one of the domains overgrows the other on a vicinal Si(100) surface. A similar suggestion has been made by Varrio *et al.*[14] The results of Pukite and Cohen[12] on vicinal, but double-domain surfaces are probably related to this mechanism.

III. DISCUSSION

The combination of the results described in Sec. II shows that the final structure of As-terminated Si(100)4° surfaces depends on the time order of raising the temperature of the clean Si substrate and raising the As_4 pressure as well as depending on the actual values of these quantities. Our results are consistent with those of Becker *et al.*,[13] who used only method (b) and made measurements at 400 °C, 600 °C, and 700 °C. The results of Varrio *et al.*[14] who appear to have used method (c) with different As_4 fluxes during the cooldown phase are also qualitatively consistent with ours. It is not clear whether the data of Kawabe *et al.*[11] correspond to our methods (a), (b), or (c), but the fact that they found that the $As_{\parallel}$ surface occurs at all temperatures below 450 °C and $As_{\perp}$ occurs at higher temperatures appears to be in contradiction with our data for all of these methods and with the data of Uneta *et al.*[16] Any method in which the substrate is cooled from temperatures above 750 °C in the presence of As could lead to unexpected results, as the comparison between the solid and open circles in Fig. 6 shows. It is therefore possible that the technique used by Kawabe *et al.*[11] approximated our method (c) and that they used some different type of cooling rate. The value of examining methods (a) and (b) in detail is that we have been able to obtain reliable pathways, which are rather insensitive to the exact temperatures (±100 °C) and the exact As_4 fluxes, to reproducibly achieve the $As_{\parallel}$ or $As_{\perp}$ structures. We have also made a more limited examination of the interaction of As_4 with substrates having the smaller offcut angle of $\phi=2°$. In all of the cases we looked at, we found no differences with the results described for the $\phi=4°$ case. In particular, it was found that method (a) with $T_e=650$ °C gave $As_{\perp}$ with a LEED asymmetry ratio of <0.1 and that method (b) with $T_e=500$ °C gave $As_{\parallel}$ with a LEED asymmetry ratio of >10.

The dependence on the time order of raising the temperature of the clean Si substrate and raising the As_4 pressure which we have found suggests that one of the $As_{\parallel}$ or $As_{\perp}$ orientations has the lower total energy, whereas the other is arrived at because of kinetic limitations, as was first suggested by Becker *et al.*[13] Because the $As_{\perp}$ orientation requires no rearrangement of the underlying substrate, it is most likely the one determined by kinetic limits. Alerhand *et al.*[26] have found theoretically that the total energy of the $As_{\parallel}$ arrangement is indeed lower than that for $As_{\perp}$ by an amount of 0.180 eV per atomic unit length along the step. This energy lowering is due to step energy differences similar to the differences found for clean Si surfaces.[8] The loss of the low-energy configuration at higher T_e is, however, unexpected.

Let us first consider the case of $T_e=400$ °C. We have found that raising the substrate temperature to 400 °C in a fixed As_4 flux gives predominantly $As_{\perp}$, whereas holding the substrate at 400 °C as the As_4 pressure is raised gives predominantly $As_{\parallel}$. This suggests that the $As_{\perp}$ orientation is locked in at temperatures well below 400 °C. It should be pointed out that once the $As_{\perp}$ or $As_{\parallel}$ orientations are locked in, we have found them to be stable to annealing at temperatures of up to about 650 °C–700 °C. The contrast between the results of dosing the surface with method (a) or method (b) is therefore caused by the different substrate temperature when the *first* As atoms reach the surface.

The $As_{\perp}$ orientation can occur by adding an As monolayer to the Si surface without any changes being required to the structure of the substrate, i.e., without any Si mass transport. The question of how the $As_{\parallel}$ orientation arises is more difficult. The XPS results show that it also corresponds to a single arsenic monolayer and therefore the underlying substrate must have rearranged. The rearrangement necessary to give the surface structure observed requires that each step moves by at least one-half of the terrace length. In other words, half of the surface Si atoms need to move an average distance of 1 nm. This can be seen schematically by comparing Figs. 1(b) and 1(d). The remainder of this section will consider how the $As_{\parallel}$ orientation can occur.

Movement of Si atoms during interaction with As has been inferred previously for the Si(111) 7×7 surface[3–6] and for stepped Si(111).[27,15] In the former case, the subsurface stacking fault, the surface Si-Si dimers, and the Si adatoms of the 7×7 structure are all rearranged to give a 1×1 symmetry after interaction with As at substrate temperatures above about 300 °C. The exact pathway from the Si(111) 7×7 to the Si(111):As 1×1 is not known, but the energy gain obtained by replacing the Si dangling bonds on the clean surface with As lone-pair orbitals is a very strong driving force. For Si(100)4°:As, the driving force for rearrangement is only the energy difference between the $As_{\parallel}$ and $As_{\perp}$ orientations. This energy difference can only be due to the steps because in a very large terrace, the $As_{\parallel}$ and $As_{\perp}$ orientations are equivalent. The analogous result for clean Si(100)4° is the preference for $Si_{\parallel}$ over $Si_{\perp}$ by an amount of 0.50 eV/a, where a is the surface lattice constant.[8] For the As-terminated case, Alerhand *et al.*[26] give a value of 0.18 eV/a along the step for the energy difference between $As_{\perp}$ and $As_{\parallel}$. The total energy difference per unit area thus decreases as the vicinal angle decreases.

The comparison with the As termination of Si(111) 7×7 shows that As-mediated rearrangement of a Si substrate is indeed possible at temperatures above ~350 °C and presumably takes place by nucleating and then sweeping out across the surface. It is more difficult to understand how the $As_{\parallel}$ orientation can form on Si(100)4° because we have shown that the $As_{\perp}$ orientation can be

locked in at low temperatures and is then stable up to ~700 °C. As a result, we might expect the first As_4 molecules arriving at the surface to form As-As dimers, with a statistically large number sticking in the center of the terrace and therefore taking up the $As_\perp$ orientation. The results for method (b) show that this does not seem to occur if the first As atoms arrive at the surface when the surface is held at temperatures between 400 °C and 600 °C. An alternative scenario is that As atoms arriving on a Si substrate at temperatures T_e above 350 °C have a high mobility and bind most strongly at the step edge, rather than locking in the $As_\perp$ orientation at the center of terraces. The competing processes are shown schematically in Fig. 7. For $T_e \lesssim 350$ °C, the movement of the Si atoms to enable the steps to move is not activated and the rate S at which As atoms can be incorporated at steps is zero. The rate T, the rate of buildup of As dimers at the center of the terrace, is nonzero. For temperatures in the range 400 °C–600 °C, $S > 0$, and the residence time in the center of the terrace is small, so that $T=0$. In the following, we suggest one possible mechanism for this to take place.

In a one-dimensional model such as that in Fig. 8, the first pair of As atoms can substitute for a Si dimer on the terrace edge [Figs. 8(a) and 8(b)] and the second pair of As atoms will then find a pair of exposed Si atoms to which it can bond [Fig. 8(c)]. The third pair of As atoms finds a less favorable situation [Fig. 8(d)] because it needs to displace Si atoms in a terrace site; however, once this has occurred, the fourth pair of As atoms will find exposed Si atoms [Fig. 8(f)]. This process of one Si atom pair being moved so that two As atom pairs can bond to the surface continues until the surface is covered by a monolayer of As. This is only one model that could explain the observed results. It is possible that As atoms (or dimers) could replace Si atoms (or dimers) in the center of terraces. It is difficult to see how this would have a lower energy than As atoms bonded on top of the Si atoms on the terraces, but our data cannot rule out such a mechanism.

We now turn to the case of As exposures made at the higher temperatures of $T_e > 650$ °C. The results show that surfaces prepared in this way have mixed $As_\parallel$ and $As_\perp$ orientations with a predominance of $As_\perp$. The question then arises of why the supposedly lower energy $As_\parallel$ orientation does not occur. The As and Si atoms must have even greater mobility on the surface than they had at 500 °C, so some other effect must be taking place. One possibility within the type of mechanism described above is that the As atoms do not reside long enough at the terrace edges. Referring to Fig. 7, if the rate C (the reemission rate of As atoms from the steps) exceeds the incorporation rate S or the arrival rate B, then the sequence of events that is necessary to move the position of the Si steps cannot take place. Kinetic limitations would then tend to lock in competing regions of $As_\perp$ orientation. Finally, at even higher temperatures, all As desorbs from the surface.

As a final point, we note that methods (a)–(d) are reversible. When any of the Si(100)4°:As samples made with these methods were annealed to 1000 °C, we obtained single-domain Si surfaces with the Si-Si dimers be-

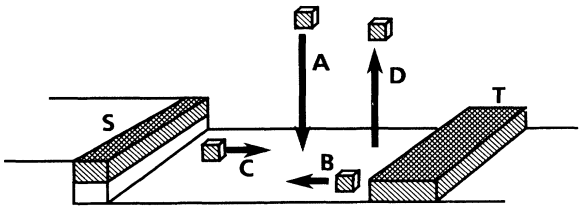

FIG. 7. Schematic illustration of the interaction of As with the Si(100) 4° surface. A and D are the adsorption and desorption rates of As atoms from the surface; T is the rate of As buildup on the terrace; S is the rate at which As atoms can be incorporated at steps with the movement of Si atoms; B is the diffusion velocity of adsorbed As_2; and C is the reemission rate of As_2 from the steps.

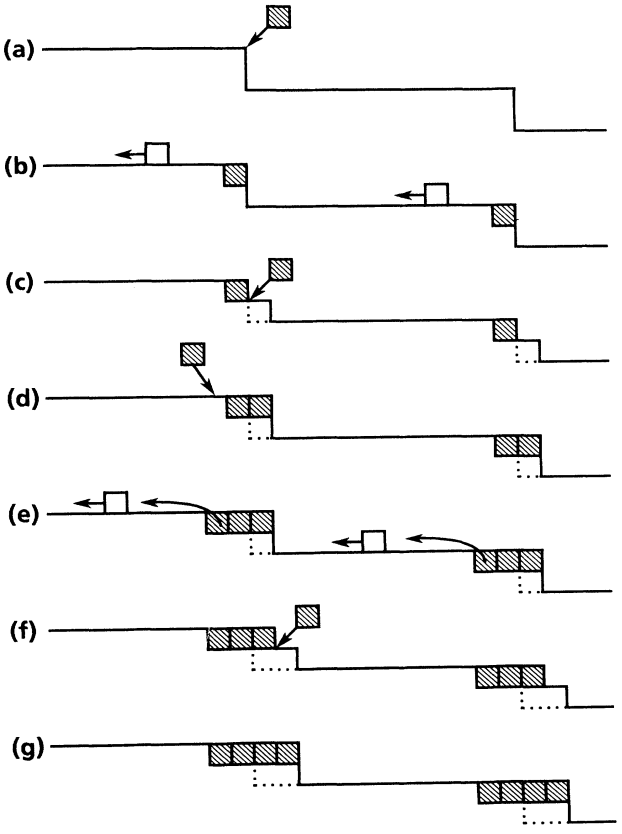

FIG. 8. Possible mechanism for the formation of $As_\parallel$ on single-domain surfaces such as that shown in Fig. 1(b). As and Si dimers are shown end-on as shaded squares and open squares, respectively. The sequence is shown from (a) to (g) and steps (d) to (g) will repeat until a single monolayer of As is formed.

ing parallel to the step edge ($Si_{\parallel}$ orientation). The transition from $As_{\parallel}$ to $Si_{\parallel}$ requires the movement of Si atoms in the substrate. We found that this occurred at the same temperatures (700 °C–800 °C) at which the As atoms leave the surface. This means it was not possible to prepare a metastable $Si_{\perp}$ surface by simply desorbing a monolayer of As atoms from the $As_{\parallel}$ surface.

CONCLUSIONS

The interaction of As with vicinal Si surfaces is complicated by the competition between kinetic and energetic effects. The lowest-energy structure is $As_{\parallel}$, but in many circumstances, the kinetically limited $As_{\perp}$ structure is found. In the paper we have described a study in which the conditions for achieving these two structures have been examined in detail. Tradeoffs between kinetically and energetically determined structures are important in understanding both surface structures and epitaxy. Our study of this particular system has allowed us to look at possible mechanisms for the rearrangement of substrates during growth.

The results we have obtained also have important implications for the epitaxy of GaAs on Si, which is usually carried out on vicinal Si(100) surfaces such as those studied here. We have shown that simply creating a single-domain bare Si surface at 1000 °C does not ensure a single-domain surface when As_4 begins to adsorb. We have further found that the use of $As_{\perp}$ or $As_{\parallel}$ templates for GaAs growth results in different GaAs crystal orientations. Our STM images also show qualitative differences in the step edge smoothness between the $As_{\perp}$ and $As_{\parallel}$ cases, suggesting that the crystal quality of GaAs grown on these templates may differ. Work towards this end is in progress. Preliminary measurements have shown that photoluminescence from the $As_{\perp}$ initiated GaAs has considerably greater intensity than that from $As_{\parallel}$ initiated material.

As a result of our study, we have obtained methods to reproducibly obtain either the $As_{\perp}$ or $As_{\parallel}$ structures. Previously, there had been a significant degree of apparent contradiction about the ranges of stability of the two structures, due to the uncertainty in the sequence of the surface exposure to As. The methods (a) and (b) which we have suggested to obtain the $As_{\perp}$ and $As_{\parallel}$ surfaces, respectively, have the important advantage that the temperature and pressure ranges are wide in each case and that the main determining factor is the time sequence of raising the As_4 pressure and raising the substrate temperature. This should allow the same results to be easily achieved in other growth systems. Our results have also shown that one of the most widely used surface preparation methods for MBE growth of GaAs on Si [labeled method (c)] is sensitive to the As dosage during the cooldown from the substrate cleaning step to the beginning of growth. This is generally an uncontrolled situation in most cases and most likely leads to a mixture of $As_{\perp}$ and $As_{\parallel}$ surfaces. Thus, even though a single-domain Si surface may be achieved by annealing to high temperatures, As-induced partial step rearrangement can subsequently drive the surface to a mixed-domain configuration, giving rise to anti-phase III-V growth in the early stages.

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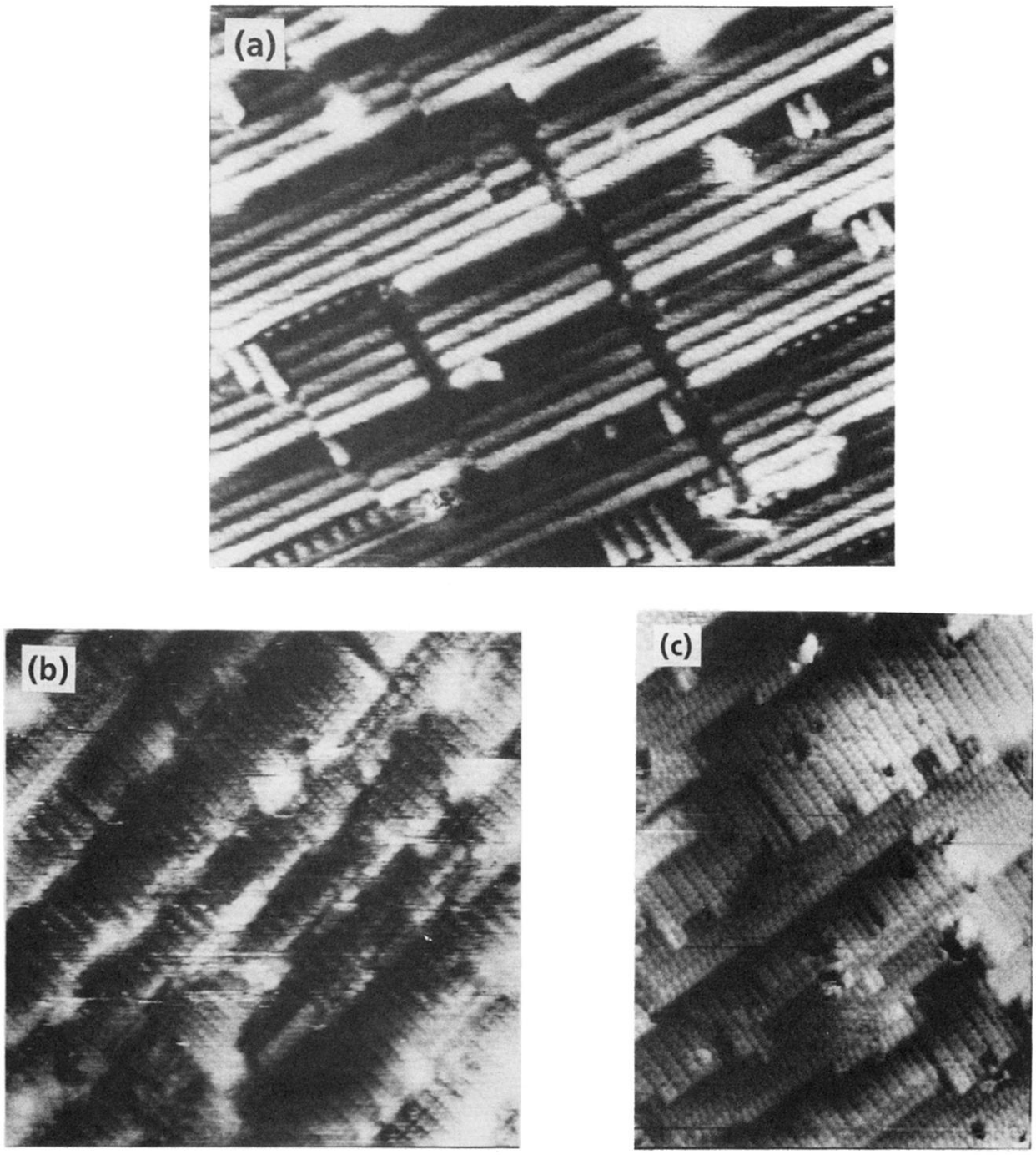

FIG. 5. STM constant-current images of Si(100)4°:As showing tunneling from filled states for (a), method (a) with $T_e = 650\,^{\circ}\mathrm{C}$; (b) method (b) with $T_e = 500\,^{\circ}\mathrm{C}$, and (c) method (c) with $T_e = 850\,^{\circ}\mathrm{C}$. The tunneling current was 100 pA in all cases and the sample bias was -1.5, -2, and -2 V for (a), (b), and (c), respectively. The dimer rows are 0.76 nm apart and the image widths are 25, 24, and 18 nm for (a), (b), and (c), respectively.