Resonant tunneling via microcrystalline-silicon quantum confinement

Qiu-yi Ye, Raphael Tsu, and Edward H. Nicollian
University of North Carolina at Charlotte, Charlotte, North Carolina 28223
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Resonant tunneling involving discrete quantum states in microcrystalline-Si (μc-Si) with a-SiO_2 barriers is observed experimentally. The low interface trap densities, and the high barrier height between Si and a-SiO_2, allow the observation of several aspects in the physics of quantum confinement. Even for extreme quantum confinement at low gate bias, applied to the Al/a-SiO_2/μc-Si/a-SiO_2/c-Si structure, the effects of quantized charge accumulation dominate over the wider separation of the energy levels of the quantum box. At high gate bias, we observe a transition from a three dimensionally to a one dimensionally confined system.

I. INTRODUCTION

Since the proposal,[1] and subsequent observation,[2] of resonant tunneling in quantum-well structures, the field has expanded to include tunneling in quantum wires[3] [two-dimensional quantum confinement (2D QC)] and in quantum boxes[4,5] [three-dimensional quantum confinement (3D QC)]. Experimentally, good lattice-matched systems of ternary and quarternary mixed alloys of III-V semiconductors, such as $GaAs/Ga_{1-x}Al_xAs$, form the majority of barrier-well heterojunctions required to realize these resonant tunneling structures. Recently, resonant tunneling in microcrystalline-silicon (μc-Si) with Si_xC_{1-x}:H barriers has been reported by Fortunato *et al.*[6] Takagi *et al.*[7] have reported quantum size effects on photoluminescence in Si particles in the size range of 45Å produced by microwave plasma decomposition of SiH_4. In the present work, μc-Si is produced by crystallization from the amorphous phase, and barriers are produced by thermal oxidation of silicon microcrystallites. The two heterojunctions with the lowest interface trap densities are $GaAs/Al_xGa_{1-x}$ As and Si/SiO_2. This work demonstrates quantum confinement in the Si/SiO_2 system opening the way to much wider applications of quantum-well structures.[8]

The structure fabricated is shown schematically in Fig. 1(a). It consists of a single layer of silicon microcrystallites embedded in a matrix of amorphous SiO_2 (a-SiO_2) sandwiched between an aluminum gate and a crystalline n-type silicon substrate. The approximately 3.2-eV barrier between the conduction bands of the μc-Si and a-SiO_2 serves to quantum mechanically confine electrons within the microcrystallites. In this work, the structure observed in the equivalent parallel conductance (dI/dV_G) measured at 1 MHz, and the dc current as the gate bias sweeps the Fermi level in the aluminum gate past the discrete energy levels in the silicon microcrystallites is explained by resonant tunneling of electrons via predominantly 3D QC in the silicon microcrystallites.

Figure 1(b) shows the spectrum of peaks observed in conductance versus gate bias at room temperature. To understand this spectrum in terms of 3D QC in the silicon microcrystallites, it is necessary to explain (1) why the peaks are so widely spaced along the gate bias axis, (2) the transition from a spectrum of sharp peaks at low gate bias to a steplike spectrum at high gate bias, (3) why the peaks at low gate bias are so narrow despite the fact that there is a distribution of microcrystallite size, and (4) that the observed spectrum is in agreement with the predicted density of states for 3D QC in silicon.[9]

To explain the large voltage separation between peaks in the spectrum, it is necessary to recognize the roll of charge accumulation in 3D QC of electrons in silicon microcrystallites bounded by a-SiO_2 on all sides. Whenever a quantum state in a silicon microcrystallite moves below the Fermi level of the aluminum gate, electrons occupy this state. This accumulation of negative charge in the microcrystallites produces a large separation between the discrete energy levels along the gate bias axis, far exceeding the separation in energy of the quantized energy states within the microcrystallites.

As gate bias is increased, the delocalization of the higher-energy states in the microcrystallites laterally couples the "atomiclike" states in neighboring microcrystallites. This coupling causes a transition from 3D QC to the usual resonant tunneling in 1D QC known as double barrier tunneling. Because delocalization requires a longer mean free path, this transition becomes more pronounced as temperature is reduced below room temperature. It is unlikely that the structures at high gate bias in Fig. 1(b) can be attributed to avalanche breakdown, because the current constrained to flow through microcrystallites the order of 100 Å in size results in a large spreading resistance, which suppresses the buildup of sufficient field.

The surprisingly narrow peaks in the observed spectrum at low gate bias will most likely occur because the distribution of microcrystallite size does not play a direct role in determining the shape of the peak. Rather, the narrow peaks probably result from the formation of uniformly charged clusters of microcrystallites. Such uniformly charged clusters could form by a selection process

of stronger coupling between crystallites with close energy level separation.

The major difference between this work[9] and the work reported by Reed *et al.*,[4] as well as the periodic oscillations of the conductance with the sequential addition of an electron to a segment of narrow channels interrrupted by two intentional barriers,[10] appears to be in the degree of quantum confinement. That is, the so-called Coulomb blockade due to charging effects[11] dominates the effects of the wider separation of the energy levels in the quantum box.

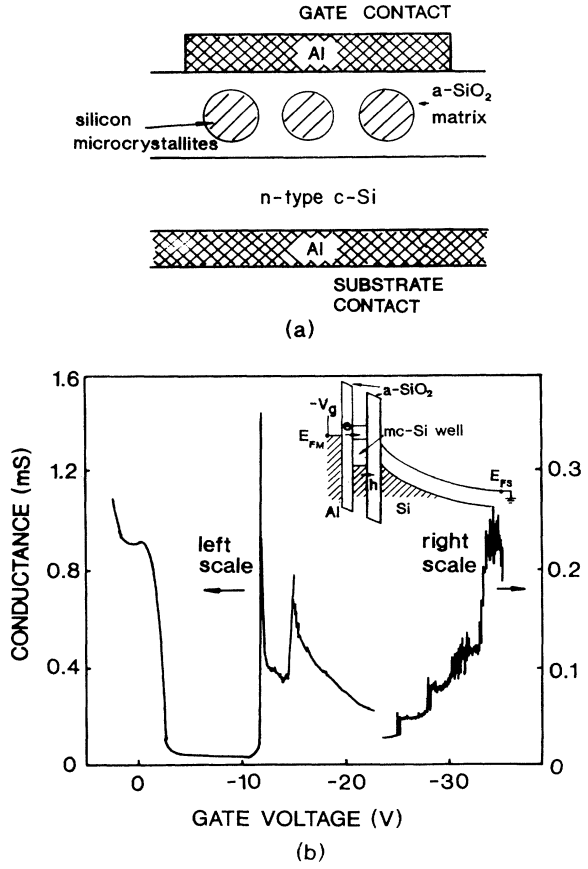

FIG. 1. (a) Cross-sectional schematic of the resonant tunneling structure. The layer labeled μc-Si consists of silicon microcrystallites embedded in a matrix of a-SiO_2. (b) Equivalent parallel conductance vs gate bias measured at 300 K, and a frequency of 1MHz. The conductance peak near zero volts is caused by electron capture and emission by interface traps at the a-SiO_2/c-Si interface. The discontinuity between the 3D QC and 1D QC regions results from the measurement of these regions on two adjacent devices on the same wafer which may have slightly different μc-Si/a-SiO_2 layer thicknesses. Examples of the measurement of both regions on the same device with no discontinuity are shown in Figs. 3 and 4. Inset: Band bending diagram in one dimension of the structure of (a) with the substrate in deep depletion. The arrows show electron and hole tunneling current components.

II. SAMPLE PREPARATION

A schematic cross section of the structure fabricated is shown in Fig. 1(a). The substrate is single-crystal silicon with a donor density of 3.5×10^{16} cm^{-3}. This structure is prepared by a planar process starting with a field oxide 1000 Å thick, thermally grown at 1050 °C in dry oxygen. The active device dimensions of 40×40 mm^2 are formed by etching a window in the field oxide photolithographically. A thin a-Si layer is deposited by e-beam evaporation, followed by simultaneous crystallization and oxidation at 800 °C for 20 min in a 3:1 dry N_2 and O_2 mixture at a total pressure of one atmosphere. Aluminum gate and substrate contacts are deposited by vacuum evaporation.

A. Microcrystallite size

Because our results depend on microcrystallite size and orientation, it is important to point out the various mechanisms that influence the properties of our structures. Microcrystallite grain size depends on deposition temperature.[12] Microcrystallites can be varied in size from 100 Å to several micrometers by controlling the substrate temperature T_s during deposition of amorphous silicon in a temperature range between 0 and 350 °C. It also was shown[13,14] that trace oxygen in the deposition chamber atmosphere results in a preferred orientation of thermally crystallized a-Si films. For example, subsequently crystallized μc-Si can have 80% of the microcrystallites oriented in the $\langle 111 \rangle$ direction for T_s in the temperature range between 30 and 200 °C, and up to 98% oriented in the $\langle 110 \rangle$ direction for $T_s \sim 600$ °C. The latter case already is crystalline as deposited, with microcrystallite linear dimension L_0, approximately equal to 2000 Å, which is too large for our purpose. Moreover, it was found that the microcrystallite linear dimension l_e obtained from Raman scattering is roughly equal to $L_0/2$ where L_0 is determined by transmission electron microscopy (TEM). The Raman peak position gives the microcrystallite size l_e when l_e is less than the electron phonon mean free path. Therefore Raman scattering is an accurate method of determining average microcrystallite size l_e for which quantum confinement will occur.[12,14] Comparing our microcrystallite film fabrication conditions with the literature,[12] we estimate l_e to be 100 Å for $T_s \sim 30$ °C, and annealing at 800 °C. The thickness of the deposited a-Si films prior to annealing and oxidation is between 120 and 180 Å. Therefore the structure consists of a single layer of silicon microcrystallites bounded on all sides by an a-SiO_2 barrier. The thickness of the a-SiO_2 is estimated from an oxide thickness versus time calibration curve at 800 °C to be about 25–30 Å.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. Measurements

The structure in Fig. 1(a) is electrically characterized by measuring dc current versus gate bias with a Keithley model 616 electrometer, and small signal capacitance and

equivalent parallel conductance ($G=dI/dV_G$) at 1 MHz as functions of gate bias V_G, with a lock-in amplifier equipped with a current preamplifier (Model 410 *C-V* plotter). Bias is applied to the device by means of a voltage ramp, at a ramp rate of 10 mV/s, and measurements are done in a light tight dry box. The inset in Fig. 1(b) is the energy-band diagram of the structure under negative bias. The arrow to the right indicates electron tunneling from the metal gate into the 3D QC levels. As electron mean free path is greater than l_e, the electron current to the right is controlled by the quantum states of the silicon microcrystallites. The arrow to the left indicates hole tunneling from the silicon substrate to the gate. The lower mobility and high trapping probability by defects for holes does not allow quantization of valence-band levels. Thus conventional hole tunneling simply contributes a background current component. The application of a voltage ramp drives the silicon surface into deep depletion because holes tunnel through the structure, preventing the formation of an inversion layer. Deep depletion is verified by the observation that the high-frequency capacitance, corresponding to a gate bias in strong inversion, does not return to its thermal equilibrium value upon momentary exposure to visible light.

B. Interpretation of the experimental results

In this section, a detailed explanation is given of the features seen in the experimental results shown in Fig. 1(b).

1. *The 3D QC spectrum—all levels empty*

For comparison with the observed spectrum, the energy spectrum for 3D QC in silicon microcrystallites is calculated with all levels empty. To show the insensitivity of the 3D QC spectrum to geometry, we have calculated the spectra for both cubic and spherical microcrystallites.[15] Because of the large voltage shifts produced by charge accumulation in the microcrystallites, the slight differences in the spectrum between cubic and spherical geometries become insignificant.

Consider first a cubic silicon microcrystallite having a volume l_e^3. The eigenvalues in such a silicon microcrystallite are given by

$$E_{mnp}=\left[\frac{m^2}{m_1}+\frac{n^2}{m_2}+\frac{p^2}{m_3}\right]\frac{\hbar^2\pi^2}{2l_e^2}\ . \tag{1}$$

In the $\langle 100\rangle$ crystallographic direction, $m_1=m_2=0.19m_e$, and $m_3=0.916m_e$. The result is more complicated in other crystallographic directions which are not considered here.[15,16] The eigenvalues for $E_{mnp}^{\langle 100\rangle}$, calculated from Fig. 2 Eq. (1), are shown at the top of Fig. 2(a).

Consider next a spherical silicon microcrystallite of radius a. A variational calculation is required to determine the eigenvalues for such a spherical microcrystallite. In this calculation, $m_t=0.19m_e$, and $m_l=0.916m_e$. Assuming that the wave functions vanish on the surface of a sphere of radius a, the resulting eigenvalues are shown at the bottom of Fig. 2(a).

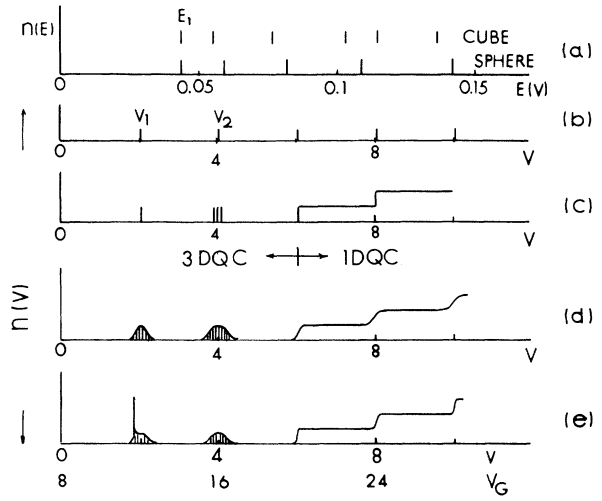

FIG. 2. (a) Calculated energy in eV for a cube of 100 Å, top (Ref. 16); and a sphere of radius 58 Å, bottom (Ref. 16). (b) Density of states vs voltage V in a microcrystallite due to charge accumulation. (c) Coupling between microcrystallites is included. (d) Spread in particle size is considered. (e) Clustering of microcrystallites is considered where the voltage drop in the depletion layer is included in V_G. Note that, at higher gate bias, delocalization of the wave functions results in a transition from 3D QC to 1D QC.

2. *The 3D QC spectrum—n levels occupied*

The two fundamental consequences of charge accumulation in the silicon microcrystallites are (1) the peaks in the observed spectrum appear at much higher voltages and are farther apart in voltage than the calculated spectra in Fig. 2(a), and (2) delocalization of electrons occupying n energy levels results in lateral charge transfer between adjacent microcrystallites. Consider first the effect of charge accumulation on the position and separation of the quantum states in the spectrum. As the Fermi level in the gate metal is swept by the applied bias past a quantum state, its energy level is shifted by a voltage $V=e/C$ where e is the electronic charge, and C is the capacitance of the two oxide barrier layers in series with the capacitance of the silicon microcrystallites. The condition for the alignment of the Fermi level in the gate metal with the nth quantum state is

$$V_n=E_n/e+(e/C)n \tag{2}$$

where E_n is the energy level of the nth quantum state when all levels are empty, V_n is the energy level in volts of the nth quantum state occupied by n electrons, and n denotes the quantum states in ascending energy. The energy separation in volts between quantum states n and $n+1$ is

$$V_{n+1}-V_n=(E_{n+1}-E_n)/e+e/C\ . \tag{3}$$

The value of e/C can be determined from the bias difference between the first two peaks in Fig. 1(b) because the number of clusters is so small that the average band

bending hardly changes when the charge in each cluster is increased by one electron. Preliminary results show consistency with experiment, but the details require further study presently underway. This separation is about 3 V across the symmetrical barriers so that $V_{n+1}-V_n=1.5$ V. A comparison of this value to $E_{n+1}-E_n$ for the first two peaks in Fig. 2(a) shows that $V_{n+1}-V_n \gg (E_{n+1}-E_n)/e$. Using this inequality in Eq. (3), $V_{n+1}-V_n \sim e/C$. To test the consistency between the observed and predicted voltage shift ΔV, we need to determine the capacitance C.[17] The value of C depends on the composite dielectric constant of the a-$SiO_2/\mu c$-Si/a-SiO_2 dielectric layers of the film, and the geometry of the film structure. A simple estimate of the composite dielectric constant, using $V=1.5$ V, $l_e=100$ Å a film thickness of 180 Å, and a planar geometry ignoring fringing fields, yields a value within a factor of 2 of the dominant dielectric constant of a-SiO_2. Because of the dominance of the charge accumulation term in Eq. (2) and (3), the detailed nature of the shape factors of these microcrystallites is not considered. In most of the experimental data, V_n is 1.5 to 2 V as shown in Fig. 2(b).

The relation between peak position predicted by Eq. (2) and gate bias V_G is $V_G=2V_n+\psi_s$ where ψ_s is the band bending in the silicon substrate. Because thermally generated holes tunnel through the a-SiO_2/mc-Si/a-Si_2 layer as shown in Fig. 1(c), no inversion layer forms, and the silicon substrate is driven into deep depletion to preserve charge neutrality. As a result, ψ_s can be quite large. From Fig. 1(b), the first peak ($n=1$) occurs at about 12 V. An analysis of the C-V curve measured at 1 MHz shows that about 25% of the gate bias appears across the a-$SiO_2/\mu c$-Si/a-SiO_2 layer, while the remainder appears across the substrate, and is equal to ψ_s.

3. *Explanation of the narrow peak widths*

Because the voltage observed across the a-$SiO_2/\mu c$-Si/a-SiO_2 layer in Fig. 1(b) for $n=1$ is comparable to the barrier height of about 3.2 eV between the conduction bands of the a-SiO_2 and μc-Si, the barrier height lowering for $n=1$ allows weak delocalization of the electrons, and stronger delocalization for $n=2$. For $n \geq 3$, delocalization is complete. Filling this level by aligning it with the metal Fermi level produces a current flow through the device and the lateral spreading of charge between adjacent microcrystallites. The lateral charge spreading is a transition that is observed from a 3D QC to a 1D QC spectrum as gate bias is increased. Figure 2(c) illustrates this transition in the spectrum. Because the gate is a metal which has a large Fermi surface, there is no region of negative resistance in the 1D QC I-V curve. Instead, after each quantum state is occupied, the current abruptly increases linearly with gate bias until the next quantum state is occupied. Thus the dI/dV_G versus gate bias curve resembles a staircase as shown.

Consider next the effect of the microcrystallite size distribution on the spectrum. A small microcrystallite will have quantum levels spaced more widely apart in energy than a large microcrystallite. Therefore several 3D QC peaks that are spread out in energy will be seen as several broadened peaks as shown in Fig. 2(d). The staircase in the 1D QC region also will be broadened as shown.

A 20% variation in microcrystallite size is found to be typical from Raman scattering experiments in μc-Si.[14] Figure 2(d) shows the effect on the spectrum of a 20% variation in microcrystallite size. A spectrum with such broadened peaks is commonly observed in our samples. However, some samples exhibit a peak width of approximately 1%. The observation of such a sharp peak may involve the formation of microcrystallite charge clusters. These specific clusters originate from a fraction of these crystallites having close physical proximity centering around the average size, which results in a significant overlap of wave functions. However, if this picture is correct, we are faced with the prospect that particles with size centering about the mean distribution are more likely to be next to each other. Alternatively, a Mott-like transition may be present. This aspect of our results is under investigation. Figure 2(e) shows the spectrum expected for 3D QC via individual microcrystallites with peaks broadened by the microcrystallite size distribution, superimposed on 3D QC via clusters which are independent of the microcrystallite size distribution, and are therefore sharp. Also shown is the 1D QC spectrum. When the 3D QC spectrum is determined by both clusters and individual microcrystallites, it is estimated, from a simple comparison of areas under the peaks, that about 20% of the contribution comes from clusters. Therefore the majority of microcrystallites do not form clusters.

4. *Discussion*

With the background just given, we show that both 3D QC and 1D QC have been observed in films consisting of silicon microcrystallites embedded in an a-SiO_2 matrix. Figure 3 shows that resonant tunneling is observed only in films containing μc-Si. Figure 3(a) shows conductance versus gate bias measured on an Al/a-SiO_2/c-Si structure having an a-SiO_2 thickness of 30 Å. Figure 3(b) is measured on an Al/a-SiO_2/a-Si/a-SiO_2/c-Si structure having an a-Si thickness of 120 Å where the a-SiO_2 was unintentionally grown to a thickness of about 20Å. Figure 3(c) is measured on an Al/a-$SiO_2/\mu c$-Si/a-SiO_2/c-Si structure where the a-Si in Fig. 3(b) has been crystallized and thermally oxidized. Only in Fig. 3(c) do features appear which can be attributed to 3D QC and 1D QC. These features are more clearly discernible in Fig. 4, which is measured at 77 K. Figure 4(a) shows conductance versus gate bias, and Fig. 4(b) shows the corresponding dc current versus gate bias, both measured at 77 K. An abrupt transition from 3D QC to 1D QC is seen at about 27 V in both curves. At gate biases below 27 V, the sharp peak indicates 3D QC via clusters, and the gradual decay of the peak with increasing gate bias indicates 3D QC via single microcrystallites. A comparison is made between conductance versus gate bias measured at 300 and 77 K in Fig. 5. In this sample, the a-Si layer was 180 Å thick before crystallization and thermal oxidation. The sharp peak originally observed at 300 K was degraded by re-

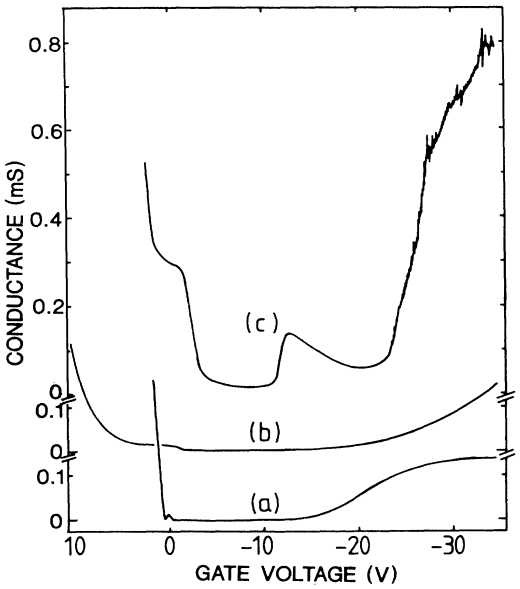

FIG. 3. Equivalent parallel conductance vs gate bias at 300 K measured at 1 MHz. (a) Al/a-SiO_2/c-Si structure. (b) Al/a-SiO_2/a-Si/a-SiO_2/c-Si structure. (c) Al/a-SiO_2/μc-Si/a-SiO_2/c-Si structure.

peated cycling between 77 and 300 K. However, this figure illustrates the temperature dependence of clustering. The decrease in mean free path with increasing temperature decouples the microcrystallites in the clusters so that no cluster formation occurs at 300 K, reflecting the effect of size distribution on the spectrum. Therefore the sharp peaks characteristic of 3D QC in clusters, and the staircase characteristic of 1D QC, are both eliminated. Figures 1(b), 3, 4, and 5 show a variety of spectra that have been observed. These spectra are reproducible from run to run and over several devices on a 3-in.-diameter wafer. The optimum a-Si thickness is found to be 180 Å. For this thickness, sharp peaks such as in Fig. 1(b) are most likely to be found. The broadened spectrum seen in Fig. 3(c) is more typical particularly when the thickness of the deposited a-Si is 120 Å. The thickness of the a-Si film was measured with a quartz crystal thickness monitor whose calibration was checked by TEM measurements.

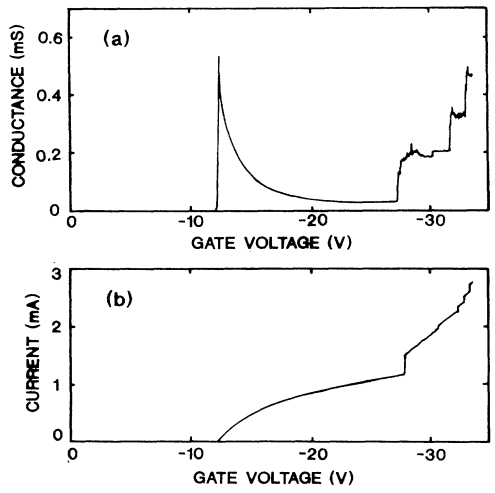

FIG. 4. (a) Equivalent parallel conductance vs gate bias at 77 K measured at 1 MHz. (b) dc current vs gate bias at 77 K measured on the same device as (a).

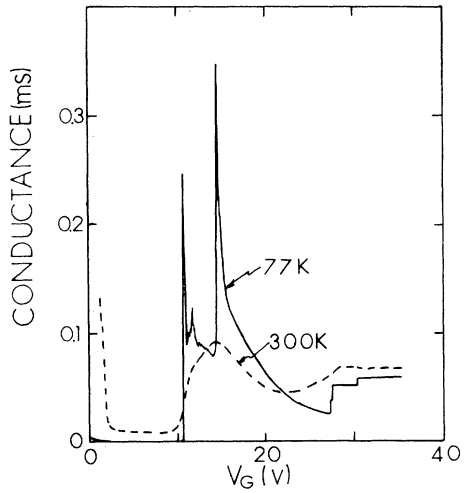

FIG. 5. Equivalent parallel conductance vs gate bias at 300 and 77 K measured at 1MHz.

IV. CONCLUSIONS

We have predicted and explained the features observed in conductance and dc current as functions of gate bias on Al/a-SiO_2/μc-Si/a-SiO_2/c-Si structures in terms of 3D QC and 1D QC. Charge accumulation is crucial for the understanding of the observations. Charge accumulation shifts the energy levels to higher values. The higher-energy quantum states are coupled, resulting in a sharp transition from 3D QC to 1D QC. Clustering is produced by lateral overlap of wave functions between adjacent microcrystallites. A consequence of such clustering is the appearance of extremely sharp peaks in the conductance versus gate bias. The sharpness of the peaks is not understood. It is possible that a Mott-like transition is present.

In this work, quantum confinement was observed in structures prepared by film growth rather than photolithography with the advantages of greater fabrication simplicity and lower costs. We have shown that quantum confinement is not limited to lattice-matched or nearly-lattice-matched material combinations. The observations reported in the Si-SiO_2 system open the way for much wider applications of quantum confinement phenomena.

ACKNOWLEDGMENTS

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[17]The effective capacitance depends on n because the induced image charge depends on the wave function. Taking C to be a constant in our discussions represents a simplistic assumption.