Periodic conductance fluctuations in quasi-one-dimensional metal-oxide-semiconductor field-effect transistors with shallow-trench isolations

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Results of conductance measurements in 0.2- μ m-wide and 0.15- μ m-long silicon metal-oxidesemiconductor field-effect transitions with shallow-trench isolations are presented. At T = 1.2 K, two kinds of periodic conductance fluctuations are observed; fine structure near threshold and plateaus in the higher conductance regime (~0.1 mS). The latter are accentuated by applying moderate magnetic fields of 1-2 T, remaining unchanged in their positions. We attribute these features to a quasi-one-dimensional transport mechanism caused by strain-induced narrow potential wells along the trench isolations.

The properties of electronic systems in very small silicon metal-oxide-semiconductor field-effect transistors (MOSFET's) are of great interest for both physicists and manufacturers. Unfortunately, one-dimensional quantization, as observed in a GaAs-Al_xGa_{1-x}As heterojunction structure,^{1,2} hardly occurs in silicon MOSFET's even with a narrow width of less than 0.1 μ m.^{3,4} This is probably because of the relatively heavy effective mass of the electrons, which requires an ultranarrow width to get a large subband spacing, and the shorter scattering length compared to that in GaAs. Thus, most studies on small silicon MOSFET's have focused on the large fluctuations in conductance at low temperatures. These fluctuations have been explained by $hopping^{5-8}$ or resonant tunnel ing^{9-11} between strongly localized states, or by changes in the phase of the eigenstates of electrons caused by weak localization effects¹² and the temperature dependence of elastic scattering.¹³ The universal conductance fluctuations are reproducible for a given sample, but differ between nominally identical samples, and they are not periodic.

In this paper we present results of conductance measurements in 0.2- μ m-wide and 0.15- μ m-long silicon MOSFET's with shallow trench isolations. The observed fluctuations are periodic and similar among identical devices. We attribute them to quasi-one-dimensional transport caused by strain-induced potential wells along the trench isolations.

Figure 1(a) shows a cross section of our samples across the channel. The *n*-channel MOSFET with a poly-Si gate over a 7-nm oxide was fabricated on a (100) substrate. The gate length is 0.15 μ m and the channel width is 0.2 μ m. The shallow trench isolation regions with the 0.5 μ m thickness are formed by wet oxidation of shallow trenches (0.1-0.2 μ m depth).¹⁴ Since the mask layers on the active channel regions mainly consist of thick and stiff silicon-nitride layers, they block the spreading of oxidation beneath the mask layers thus preventing the narrowing of the channel regions and producing strong compressive strains in the direction across the channel. The p^+ isolation regions beneath them are formed deeply, so that the current can flow even along the channel edge without suffering from an increase in threshold voltage at the edge. The deep formation also prevents the potential fluctuations caused by boron impurities, reducing an unintentional hopping current.⁵ Devices 5 μ m wide



FIG. 1. (a) Cross section of *n*-channel MOSFET with shallow-trench isolations across the channel. (b) Schematic of the conduction band across the channel. Compressive strains across the channel induced by shallow-trench isolations lower the band energy of the *y* valley, E_y , especially near the Si-SiO₂ interface regions, while they raise the band energy of the *z* valley, E_z .

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and 5 μ m long were simultaneously prepared on the same wafer. The mobility of these devices is $\sim 3000 \text{ cm}^2/\text{V}$ s at 4.2 K. This value leads to an elastic scattering length of ~ 30 nm for the gate voltage range discussed below $(V_g - V_{th} \sim 0.2 \text{ V}; \text{ an electron density } N_s \sim 6 \times 10^{11} \text{ cm}^{-2})$. The conductance was measured using conventional low-frequency ac lock-in techniques. The samples were studied at the end of a copper cold finger attached to the mixing chamber of a dilution refrigerator.

Figure 2 shows the conductance of two identical devices at 1.2 K. The source-drain voltage is 200 μ V. It is found that the two devices have three similar plateaus (A1, B1, C1 for sample 1 and A2, B2, C2 for sample 2)with gate voltage spacing, ΔV_g , of ~0.1 V between them, although the plateaus of sample 2 are less pronounced. These plateaus are hardly observable at 4.2 K. ΔV_g of 0.1 V corresponds to an electron density difference, ΔN_s , of 3×10^{11} cm⁻². This value is too large if we would assume that the plateaus stem from one-dimensional transport in a 0.2- μ m-width potential well; using the squarewell approximation with one-dimensional subbands, ΔN_s of 3×10^{11} cm⁻² leads to a well width of ~40 nm which value is an order of magnitude smaller than the width of the MOSFET.

Figure 3 shows the expanded version of the structure near threshold. In sample 1, the periodic fine structure with ΔV_g of ~0.03 V can be seen. In sample 2, at least two fine structures, a and b, can be seen with ΔV_g of ~ 0.035 V between them.

The fact that the plateaus of Fig. 2 and the fluctuations of Fig. 3 are periodic and similar between the identical devices strongly suggests that these fluctuations are not due to localized states which would not be distributed identically in different samples of identical devices. We attribute them to quasi-one-dimensional transport caused by strain-induced potential wells along the channel edges. Figure 1(b) shows a schematic of the conduction band across the channel without the gate voltage. The SiO₂ shallow-trench isolation will induce a strong compressive strain in the direction parallel to the surface and perpendicular to the current flow (y axis). The strain will reach over 10^3 N mm⁻² (Ref. 15) at the channel edge near the trenches, decreasing rapidly toward the channel center. The splitting of the conduction-band energy, ΔE , caused by the anisotropic strain P is given by 16, 17



A2

FIG. 2. The conductance of two identical devices as a function of gate voltage V_g at 1.2 K.

B2

A1

B1

C2

C1



FIG. 3. The conductance vs V_g at 1.2 K near threshold.

$$\Delta E(\text{meV}) = E_z - E_y = E_x - E_y = 8.4 \times 10^{-2} \text{ P(N mm^{-2})},$$

where E_x , E_y , and E_z are the conduction-band energies of x, y, and z valleys, respectively. Thus, ΔE could reach over 0.1 eV at the channel edge and decrease toward the channel center as shown in Fig. 1(b).

The plateaus of Fig. 2 and the fluctuations of Fig. 3 are considered to be caused by such strain-induced potential wells. For near-threshold gate voltages, the currents will flow only at the edge along the trenches. The periodic fluctuations of Fig. 3 could correspond to one-electron accumulation in the ultranarrow channel at the edge, i.e., Coulomb blockade. The channel width is roughly estimated to be ~10 nm for ΔV_g of 0.03 V, using the macroscopic calculation of $W \sim e/(CL_g \Delta V_g)$, where C is the capacitance per unit area. The small value of 10 nm implies that the strain is especially large in small regions near the Si-SiO₂ interface. It should be noted that electrons occupy the y valley whereas they occupy the z valley in ordinary MOSFET's with no strain present. Recently, periodic fine structure near threshold has also been reported in dual-gate silicon MOSFET's where a channel width of ~ 10 nm has been obtained by a novel split lower gate.18

The strain will also affect the conductance in the higher conductance regime shown in Fig. 2. As the gate voltage is increased, the current begins to flow over all the regions under the gate although the charge density is still higher at the edges. However, in the channel center regions where the separation between E_v and E_z is small, the electrons will occupy the z valley. This is because the heavier effective mass of the z valley perpendicular to the surface leads to a lower subband energy in the z direction.¹⁹ Since E_z is lowest in the center, as shown in Fig. 1(b), and the depth of the potential well could be enhanced by the repulsive force caused by electrons in the y valley at both edges, the effective channel width for the electrons in the z valley in the center will be much smaller than 0.2 μ m. This results in the observable plateaus of Fig. 2 caused by quasi-one-dimensional transport. The conductance should be a sum of the quantized value of $2e^{2}n/h$ for three one-dimensional channels; one in the center and one at each edge. The observed conductance is, however, much smaller than the expected value. This is because the transmission coefficient is less than unity due to scattering, especially for the channels at both edges, and because of the parasitic resistance in both

0.25

0.2

0.15

0.1

0.05

Conductance(mS

T=1.2K

Samp.2

contact and narrow diffusion regions. The plateaus are considered to mainly come from the channel in the center where scattering may be much less than at the edge, while the gradually rising backgrounds come from the channnels at both edges. We believe that the low conductance of sample 1 is not mainly due to the scattering, but can be attributed to the high contact resistance at low temperatures in this sample because the periodic structures are still clearly observed.

Figure 4 shows the conductance of sample 2 as a function of V_g for various magnetic fields applied perpendicular to the surface. The measurements were performed at the much lower temperature of 40 mK. The source-drain voltage is 40 μ V. The figure shows evidence that the plateaus are due to one-dimensional transport. A moderate magnetic field of 1-2 T is seen to accentuate the plateaus (A2, B2, C2), which are obscured in the random fluctuations appearing at 40 mK when no magnetic field is applied. A weak magnetic field reduces backscattering and phase coherence in the plateaus, making the plateaus sharper.²⁰ In addition, the structure is basically independent of the magnetic field, being the same as that of Fig. 2 at 1.2 K without magnetic fields. This indicates that the origin of the plateaus is not in changes in the phase of the eigenvalues caused by weak localization. Hopping or resonant tunneling would lead to lower observed conductance, so we rule out these processes as the origin of the plateaus. Thus, it is concluded that the plateaus A2, B2, and C2 come from quasi-one-dimensional transport probably caused by shallow trench isolation-induced strains.

Finally, we point out that the strain-induced potential wells at the Si-SiO₂ interface may also affect other types of devices operating at low temperatures. For example, anomalous recombination currents in bipolar transistors at low temperatures²¹ may partly be explained by the increased current injection at the Si-SiO₂ interface. The mobility measurements using lateral bipolar transistors²² would require careful consideration of the influence of the current path along the Si-SiO₂ interface, where the diffusion mechanisms and impurity concentrations are different from those in a bulk.

In summary, two kinds of periodic conductance fluc-



FIG. 4. The conductance of sample 2 as a function of gate voltage V_g at 40 mK for various magnetic fields perpendicular to the surface. The curves are offset vertically for clarity. The values of magnetic field are also indicated.

tuations have been observed in $0.2-\mu$ m-wide and $0.15-\mu$ m-long silicon MOSFET's with shallow-trench isolations. The periodic fluctuations near threshold could correspond to one-electron accumulation in a ~10-nmwidth potential well at the edge along the trenches, which would be caused by the strong compressive strain near the Si-SiO₂ interface in the direction perpendicular to the current flow. Periodic plateaus in the higher conductance regime (~0.1 mS) are also attributed to anisotropic strain induced by trench isolations, which leads to quasione-dimensional transport.

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