Observation of single-electron-tunneling oscillations

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(Received 1 June 1990)

The time correlation of tunneling events has been predicted to occur in ultrasmall tunnel junctions: a periodic tunneling with a frequency determined by the current $f=I/e$. To test the predictions, we have fabricated one-dimensional arrays of $Al/Al_xO_y/Al$ tunnel junctions with areas down to 0.006 μm^2 corresponding to capacitances of ~ 0.2 fF. Each array contained between 15 and 53 junctions. Current-voltage characteristics were measured at temperatures between 0.05 and 4.2 K. We observed phase locking of single-electron-tunneling oscillations to external microwaves in the frequency range 0.7–5 GHz. The phase locking manifested itself as peaks in the differential resistance at bias currents $I=nef$ ($n=\pm 1,\pm 2$), corresponding to multiples of the microwave frequency. Numerical simulations show good agreement with our spherical results.

I. INTRODUCTION

A correlation between tunneling events in both space and time may occur in ultrasmall tunnel junctions. This paper reports the observation of time-correlated tunneling of single electrons in arrays of junctions, as well as describing general properties of these arrays.

Anderson,[1] in 1964, was the first one to point out that if the capacitance of a tunnel junction was made very small, the charging energy term in the Hamiltonian for such junctions could be significant and lead to new effects in Josephson junctions. Later it was recognized[2,3] that the same is true for normal-metal junctions.

If the area, and consequently the capacitance C, of a junction is made very small, the elementary charging energy $E_c=e^2/2C$ associated with the tunneling of a single electron can become larger than both the thermal energy k_BT and the quantum fluctuation energy $\hbar/\tau$, where $\tau=RC$ and R is the resistance of the tunnel junction (i.e., $R \gg R_Q=h/4e^2\approx 6.5$ kΩ). Under these conditions, tunneling of a single electron results in a noticeable recharging of the junction capacitance, so that the probability of other tunneling events is drastically affected. The charge Q on a junction can be altered, not only by an addition or subtraction of charges multiple to e due to tunneling, but also by a continuous displacement of the charge distribution. Q can therefore assume any value and does not have to be an integer multiple of e. As long as the absolute value of Q of an isolated junction is less than $e/2$, tunneling of an electron in either direction will increase the charging energy, so that the tunneling is virtually blocked. This is called the Coulomb blockade of tunneling and it should manifest itself in the dc I-V characteristic in two ways: first, as a threshold voltage $V_t=e/2C$, below which no tunneling occurs ($I=0$), and second, as a voltage offset $V_{off}=\pm e/2C$ of the large-current asymptotes from the origin. As $|Q|$ exceeds $e/2$, tunneling becomes favorable and one electron can tunnel. After this tunnel event, $|Q|$ is again less than $e/2$. Further tunneling is then blocked until the current source has recharged the junction above $e/2$ again.

In the 1960's, the Coulomb blockade was observed experimentally in granular systems.[4,5] The rapid development of new technologies, such as e-beam lithography and scanning tunneling microscopy (STM), has made it possible to fabricate and study well-defined ultralow-capacitance junctions. Thus there has been a renewed interest in tunneling and other phenomena in mesoscopic systems.

The theory behind these charging effects has been developed by several groups.[6–10] New effects have been predicted; for reviews, see Refs. 11 and 12. Coulomb blockades and space correlation of the tunneling events in multijunction structures (i.e., a tunneling event in one junction affecting the tunneling probability in a neighboring junction) have been experimentally confirmed using thin-film junctions,[13–16] STM spectroscopy,[17,18] and granular systems.[19,20] The results give good support for the qualitative and quantitative correctness of the theory.

Maybe the most spectacular consequence of the Coulomb blockade is a time correlation between tunneling events.[7,11,12] In a current-biased junction, this correlation gives rise to voltage oscillations with a frequency f fundamentally related to the current I as $f=I/e$. It is possible to phaselock these oscillations to an external microwave frequency, or to its harmonics, so that equidistant *voltage* steps show up in the I-V characteristic at currents

$$I=nef_{ext} \ . \tag{1}$$

This is to a large extent analog to the *current* steps found in the I-V characteristic of an irradiated Josephson junction.[21]

In very small superconducting junctions, where the Josephson coupling energy $E_j=\hbar I_c/2e$ is comparable to E_c, very similar changing effects should occur as a result

of single Cooper-pair tunneling. The resulting oscillations are called Bloch oscillations[22] because of the similarity of the equations to those describing Bloch waves occurring in solids.[23]

Although several groups have been able to fabricate very small, well-controlled junctions,[13–16,24] the time correlation has not been conclusively observed up to now. In granular systems, some indication of phase locking has been reported,[25,26] but the interpretation is not straightforward. The main reason for the negative results in the search for time correlation is, we believe, the parasitic influence of the connecting measurement leads. The properties of the junction are very dependent on its high-frequency electrodynamic environment, i.e., the structure of the measurement leads connected to the junction.[27] The junction is affected by the environment in two ways: First, the parasitic capacitance of the leads, which is usually much larger than the junction capacitance C itself, is added to C, thereby decreasing the charging energy considerably. Second, the microwave impedance of the leads acts as a shunt resistance at high frequencies. This shunt resistance, which is of the order of the free-space impedance $\approx 377\ \Omega$ or less for any microstrip configuration, results in a voltage bias of the junction, which of course prevents any voltage oscillations.

The use of a one-dimensional array of N series-connected junctions may be a way to circumvent the problems with the environment of a single junction. Each junction inside the array is effectively decoupled from the parasitic capacitance and conductance of the leads by its high-resistance neighbors. The junction senses only the remaining parasitic capacitance C_0 of the electrodes between itself and its neighboring junctions. This parasitic capacitance C_0 can be made much smaller than C.

The properties of these arrays can be readily calculated.[28–30] When a voltage is applied to such an array, no current will flow as long as the voltage is kept below a certain threshold:

$$V_t \approx e/\sqrt{CC_0}, \quad \text{if } C \gg C_0 \ . \tag{2}$$

The voltage penetrates into the array and is voltage-divided capacitively by C and C_0, so that the voltage falls off exponentially as $V_i = Ve^{-(i/M)}$, where i is the number of the electrode counted from the edge, and

$$M \approx \sqrt{C/C_0}, \quad \text{if } C \gg C_0 \tag{3}$$

is the characteristic falloff length of the voltage. As the voltage exceeds V_t, a "charge soliton" will form and enter the array. Such a soliton has a core, an extra e charge on the kth electrode, and exponential wings of the length M, where the charge potential is exponentially falling as $\exp(-|i-k|/M)$.

As a charge soliton moves from one junction to the next, the whole charge distribution moves with it. This causes the charge on a junction in the vicinity to change. These discrete changes ΔQ are small if the soliton is distributed over a large number of junctions, i.e., if M is large. A junction inside the array is therefore fed by a current consisting of discrete changes ΔQ in the charge rather than by a continuous current. However, if M is large, the changes in charge are very small, $\Delta Q \ll e$. This means that we can simulate an almost continuous current, which promotes a well-defined single-electron-tunneling (SET) frequency. For this reason it is important to use a large M value. Furthermore, the solitons should be well contained in the array to avoid edge effects; i.e., a large number of junctions is required in the array ($N \gg M$).

If there are several solitons in the array, they repel each other because of Coulomb interaction, so that they line up in a one-dimensional Wigner lattice inside the array. Motion of the soliton lattice results in a nonvanishing dc current I.

At large voltages, the current asymptotically reaches $I = (V - V_{\text{off}})/R$, where

$$V_{\text{off}} = Ne/2C, \quad \text{if } M \ll N \ . \tag{4}$$

Numerical simulations[28,29] for arrays of junctions show that even when an array is voltage biased, coherent SET oscillations can take place there, provided that the conditions $N \gtrsim 2M \gg 1$, $T \ll e^2/k_B C$, and $I \lesssim e/RC$; the latter condition is caused by the decreasing amplitude of the SET oscillations with increasing current. As a result, the same kind of voltage steps predicted for a single current-biased junction can appear in the I-V characteristic of the array when it is irradiated with microwaves.

In this paper we will report on the fabrication of and measurements at very low temperatures on 14 different arrays of thin-film $Al/Al_xO_y/Al$ junctions. Especially, we will discuss our findings on the single-electron-tunneling oscillations observed in several of these arrays. A brief report on some of the results presented here has already been published.[31]

II. SAMPLE FABRICATION

Ultrasmall tunnel junctions have been fabricated using e-beam lithography. Surrounding circuit elements were defined using e-beam lithography and photolithography.

Two-inch silicon wafers are chosen as substrate material for two reasons. First, they are easily processed using standard photolithography equipment and, second, the doped Si has a nonvanishing conduction at room temperature, shunting the tunnel junctions and protecting them from electrical discharges, etc., during the fabrication process and the subsequent handling up to the point of measurement. At low temperature, the substrate is completely insulating and the junctions are shunted negligibly. A drawback of the silicon is its relatively high dielectric constant, $\varepsilon_r = 12$, which increases the parasitic capacitance of the electrodes between the junctions and gives a lower M value.

The contact pattern contains 12 separate $10 \times 10\text{-mm}^2$ chips, each with eight contact pads leading to a central area of $40 \times 40\ \mu\text{m}^2$. The photoresist AZ1470 is spun onto the wafer, exposed using the desired contact pattern, and developed in a Microposit developer. A double metal layer of 20 nm of chromium nickel and 80 nm of gold is evaporated (from slightly different angles for CrNi and Au), and the redundant metal is lifted off in acetone. The chromium-nickel film has several functions: It makes the

gold stick better to the surface, it gives better electrical contact to the substrate (good for junction protection), and, because of the slightly different evaporation angles, a step structure is formed which ensures a better contact between the CrNi/Au films and the very thin electrodes of the junctions to be evaporated on top.

An *e*-beam resist is spun onto the wafer which is then cut up into six pieces, each with two chips. A double-layer resist consists of an ~210-nm-thick bottom layer of PMMA/MAA (copolymer) and an ~60-nm-thick top layer of PMMA (950 k) is used. The double chip is mounted in a JEOL JBX 5DII *e*-beam lithography instruments, and the central 40×40-μm^2 area of each chip is exposed using the junction pattern. A current of 30 pA, a beam voltage of 50 kV, and an area dose of 160 $\mu C/cm^2$ are used. Each chip is then developed in two different selective developers: first, for ~15 s in the PMMA developer which consists of a 1:3 mixture of toluene and isopropanol; then, for ~35 s in the copolymer developer which consists of a 1:5 mixture of ethyl-cellosolve acetate (ECA) and ethanol.

The resist mask now contains an undercut pattern (Fig. 1) with suspended bridges[32] which will be used to form the junctions. By depositing bottom and top electrodes from different angles, the overlap can be controlled. The base and top electrodes are evaporated from electrically heated tungsten boats while the substrate holder is tilted at two different angles ($\sim\pm15°$) to give the desired overlap. Before the top electrode is deposited, a tunneling barrier is formed by introducing 0.05 mbar of oxygen to the chamber for 3–10 min. This results in individual junction resistances of 30 kΩ to 1 MΩ. The whole sequence is carried out at a substrate temperature of $\sim+2$ °C, which is achieved with Peltier elements built into the substrate holder. This process gives fine grains in the Al electrodes and a minimum linewidth of 50–60 nm. For this work, the linewidth is designated to be ~90 nm in order to increase the ratio C/C_0, and, consequently, the size of the solitons.

Several different layouts were used, usually with two arrays on each chip, except for chip No. 1 which contained five arrays. Figure 2 shows a typical layout for the 40×40-μm^2 center part of the chip; it contains five different objects which can be measured separately. Pad No. 0 is common for all objects. Arrays for this investigation, differing only in the number of junctions, are connected to pad Nos. 2 and 3, and a single junction is connected to pad No. 4. The remaining pads are used for measurements on single-electron three-terminal devices; these measurements will be presented separately.[33] Each metal island in an array is $\sim90\times170$ nm^2, and each junction is approximately 90×70 nm^2 in area, except for arrays 1.1 and 1.2, where they were $\sim90\times90$ nm^2. Both ends of the metal islands are used to form junctions; this is necessary to keep the parasitic capacitance C_0 low. A SEM picture of one of the arrays is shown in Fig. 3.

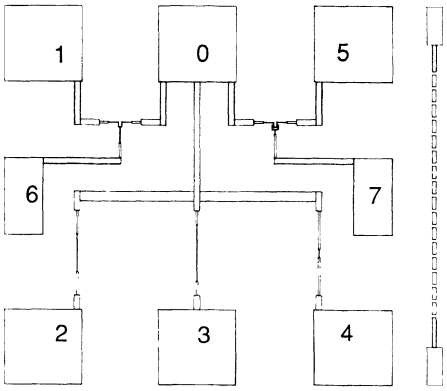


FIG. 2. Layout of the 40×40-μm center area. Two arrays of junctions are connected between the common electrode No. 0 and electrodes Nos. 2 and 3. A single junction is connected to No. 4. The rest of the pads are used for three-minimal devices that are not discussed in this paper but which give junction parameters in accord, with those reported here. The 33-junction array connection between the pad Nos. 0 and 2 is enlarged on the right.

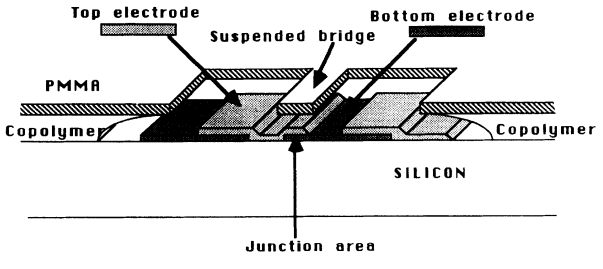


FIG. 1. The method of hanging resist bridges and evaporation from different angles is used to form overlap tunnel junctions as sketched above. The distances and angles are not to scale.

Using a specific capacitance for the Al_xO_y barrier of 45 ± 5 $fF/\mu m^2$ (see Ref. 34), we can estimate the junction capacitance to be about 0.25–0.30 fF. This gives a charging energy that corresponds to a temperature of 3–4 K.

The samples can usually be cycled between room and helium temperature several times without being destroyed. Stored at room temperature, in air, the junction resistance increases slowly with time. For instance, chip No. 4 was stored in air at room temperature for a week between two measurements. The resistance increased by 17% and 20% for the arrays 4.1 and 4.2, respectively. For the offset voltage, the increase was 9% and 11%, respectively. The data presented in Table I for this chip are taken from the second measurement.

III. MEASUREMENT TECHNIQUES

Each sample is tested between 1.2 and 4.2 K in a conventional ^{4}He cryostat and is then measured at temperatures down to 50 mK. To achieve these lower temperatures, a small dilution refrigerator with a short turnaround time is used. The temperature is measured with a calibrated carbon resistor.

The idea of the measurement system is to reduce the external noise pickup rather than filter it. The whole sys-

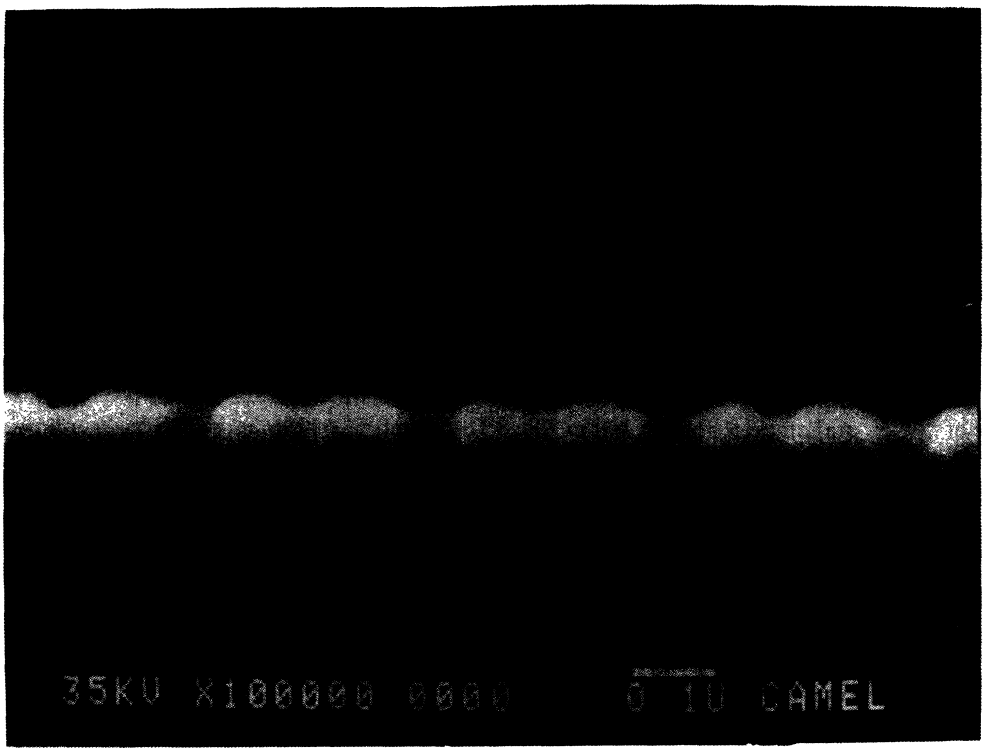


FIG. 3. A scanning-electron-microscope picture of a part of one of the arrays that was investigated.

tem is symmetric in order to minimize external pickup. A well-shielded box containing battery-operated low-noise amplifiers, voltage dividers, and RC filters is situated on top of the cryostat. Any signal coming out from or entering this box has a low source impedance and a high level (of the order of volts). The line-operated bias supply generates high-level signals that are voltage divided and filtered inside the box.

Thin silver and manganin wires, which are thermally grounded at several temperatures, connect the box with the sample holder. These wires are well shielded by the stainless steel of the cryostat and enter the sample-holder through feed-through capacitors. The sample holder forms a closed cavity.

The leakage resistance of the whole system, including the substrate, is of the order of a few hundred GΩ, measured at low temperature.

Microwaves from a sweep generator can be fed to the junctions via a coaxial cable and a three-turn coil wound close to the substrate. A 10-dB attenuator is situated in the helium bath in order to reduce the incoming noise. A 1-m-long, coiled, and very thin (0.6-mm outer diameter)

TABLE I. Data for 14 different arrays.

Sample No.	N	R (MΩ)	$2V_{\text{off}}$ (mV)	V_t (mV)	$2I_0$ (nA)	R/N (kΩ)	$2V_{\text{off}}/N$ (μV)
1.1	15	0.50	5.7	0.73	11.4	33.3	380
1.2	23	0.75	8.3	1.0	11.1	32.6	361
1.3	15	0.80	8.5	1.2	10.6	53.3	567
1.4	19	0.95	10.0	1.5	10.5	50.0	526
1.5	23	1.2	12.5	1.9	10.4	52.2	544
2.1	15	3.2	11.2	1.8	3.50	213	747
2.2	19	3.9	14.0	2.0	3.59	205	737
3.1	33	8.0	24.0	6.1	3.00	242	727
3.2	53	12.0	33.0	8.2	2.75	226	623
4.1	33	8.5	28.0	5.2	3.29	258	848
4.2	53	15.0	44.0	5.6	2.93	283	830
5.1	33	27.0	39.0	7.5	1.44	818	1180
6.1	33	38.0	42.0	7.9	1.11	1150	1270
6.2	53	43.0	59.0	11.0	1.37	811	1110

coaxial cable is used to minimize the heat transfer from the still to the mixing chamber. The power loss in this thin coaxial cable is about 5 dB at 1 GHz and increases rapidly with increasing frequency. The coupling between the three-turn coil and the sample is very poor, about -60 dB at the best. This makes it possible to affect the I-V characteristics of the arrays only at certain frequecies, without heating up the sample holder. At frequencies where the coupling is good, the microwave power needed (at the room-temperature end of the coaxial cable) to affect the I-V characteristic of an array is generally -5 to -20 Bm. Noise from frequencies outside the pass bands is effectively blocked from reaching the junctions. The typical microwave coupling as a function of frequency for array 2.2 is shown in Fig. 4.

The tunnel elements are connected between two large current-measurements resistors, typically 100 MΩ or 1 GΩ each. A symmetric bias voltage is applied to the resistors giving a current-biased junction (at low frequencies and beyond the threshold V_t). Both the voltage and the current are measured by instrumentation amplifiers with a very large input resistance ($R_{\text{in}} \approx 10^{13}$ Ω) and plotted on an x-y recorder.

A small ac signal can be added to the bias, so that both differential resistance dV/dI and conductance dI/dV can be measured using two lock-in amplifiers. The first one is used in a feed-back loop to keep either the ac voltage or the ac current constant. The second measures the ac response in the noncontrolled signal, which is then proportional to dI/dV or dV/dI, respectively. A modulation frequency of 17 Hz was typically used.

IV. EXPERIMENTAL RESULTS

We will now present data for 14 different arrays, with N ranging from 15 to 53. We start by treating the general dc I-V characteristics and the usual charging effects; then, we will show the microwave response of these arrays and the phase locking of the SET oscillations.

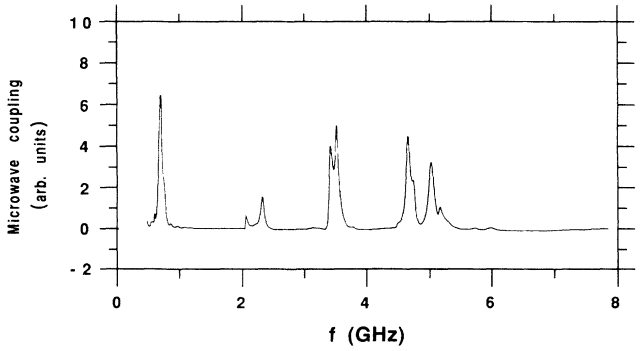
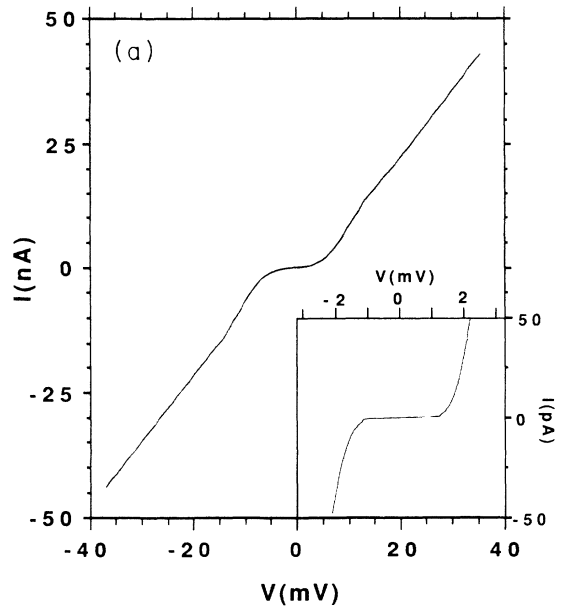


FIG. 4. The microwave response of array 2.2 as a function of frequency within the range 0.1–8 GHz. The coupling between the exciting coil and the array is good only within limited frequency regions. The coupling is measured as the voltage response of the junction biased at a constant current and kept at 50 mK.

A. I-V characteristics

Pertinent parameters have been extracted from the I-V curves and are presented in Table I. For each array the resistance R, the offset voltage, the threshold voltage, and the (roughly) area-independent quantity $2I_0 = 2V_{\text{off}}/R$ are given. Since R and V_{off} scale with the number of junctions, they are also given per junction. The sample number $x.y$ denotes the yth sample of the xth chip. The



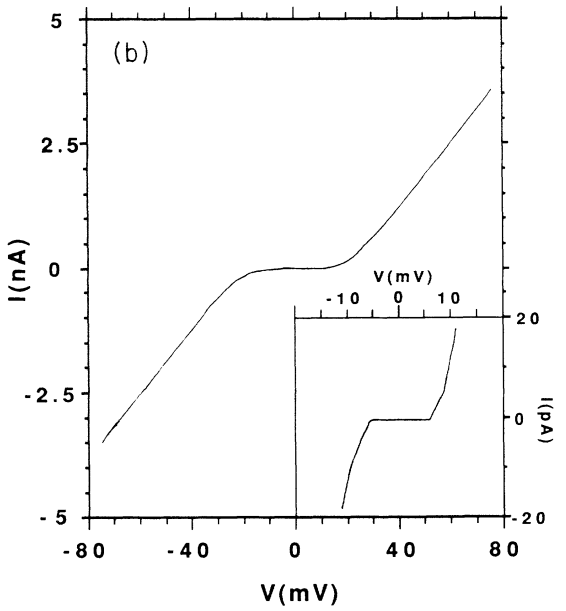


FIG. 5. (a) I-V of array 1.2 ($N=15$); $T=90$ mK. The inset (in the right-hand corner) shows the magnified picture of the same curve at low bias and at $T=60$ mK. Note that the current is practically zero until a threshold voltage of about 1.0 mV. (b) I-V for array 4.2 ($N=53$). The inset (in the right-hand corner) shows a magnified picture of the same curve at low bias. The threshold voltage is about 5.6 mV; $T=70$ mK.

data for array 2.2 is compared to numerical simulations.

I-V curves for the samples 1.2 and 4.2 are shown in Fig. 5. The typical voltage offset V_{off} at large voltage bias and the drastically reduced current at low voltage are clearly seen in all curves. At voltages $V < V_t$, the current is zero within the accuracy of our measurement (~ 50 fA). The slope of the *I-V* curve at $V < V_t$ corresponds to a resistance of more than 100 GΩ for all arrays. The insets in Fig. 5 show the low-voltage *I-V* curve for the samples 1.2 and 4.2, with an expanded current scale. The experimental *I-V* curve for sample 2.2 is compared with numerical simulations in Fig. 6 (for the parameters, see Sec. V).

The curves are only slightly affected by the superconductivity of the Al electrodes occurring at $T_c \approx 1.2$ K. Comparing different arrays, we observe a rapid smearing of the superconducting gap structure for increasing resistance. In the *I-V* curve of sample 1.2, which has a resistance per junction of 33 kΩ, it is possible to see a weak superconducting-gap structure; but in sample 4.2, which has $R/N = 820$ kΩ, there is no trace of the superconducting-gap structure, not even in the derivative measurement.

The superconducting-gap structures vanished as a magnetic field was applied. Otherwise, the *I-V* curve was not affected by the magnetic field. The Josephson supercurrent could not be observed in any of the arrays.

As the temperature is increased from 0.05 K, the large-scale *I-V* characteristic is unaffected up to ~ 0.5 K. Above 0.5 K the *I-V* curve is gradually smeared, as can be seen in Fig. 7 for sample 2.2. Note that an offset voltage can be seen at 4.2 K, i.e., well above the superconducting transition temperature of the Al electrodes.

B. Microwave response

The *I-V* curves were also smeared by applied microwaves as shown in Fig. 8. However, a fine structure also appeared with the microwaves. To amplify the structure, the differential resistance R_d versus current was measured as the arrays were irradiated with microwaves of different amplitudes A and frequencies f_{ext}. Peaks in R_d were observed in three of the measured arrays; data for sample 2.2 can be seen in Fig. 9(a). First- and second-order peaks were observed for both positive and negative currents at several frequencies. In a few plots, a weak third peak can even be seen. Figure 9(b) shows the R_d versus I results of a simulation of the microwave-irradiated array with the same parameters as for the *I-V* curve (see the discussion in Sec. V).

As the microwave amplitude was altered, the magnitudes of the peaks changed (they first increased and then decreased in a Bessel function manner), but their positions remained fixed. The arrays were irradiated with frequencies ranging between 0.7 and 5 GHz. The locations in current of the first- and second-order peaks are plotted in Fig. 10 as a function of the microwave frequency. The locations of the peaks were determined after subtracting the background slope of the zero-order peak. The errors are assumed to be $\sim \pm 15$ pA for the frequencies below 1 GHz. At larger frequencies, where the peaks were more shoulderlike, the error is larger: $\sim \pm 75$ pA.

The differential conductance G_d versus voltage was

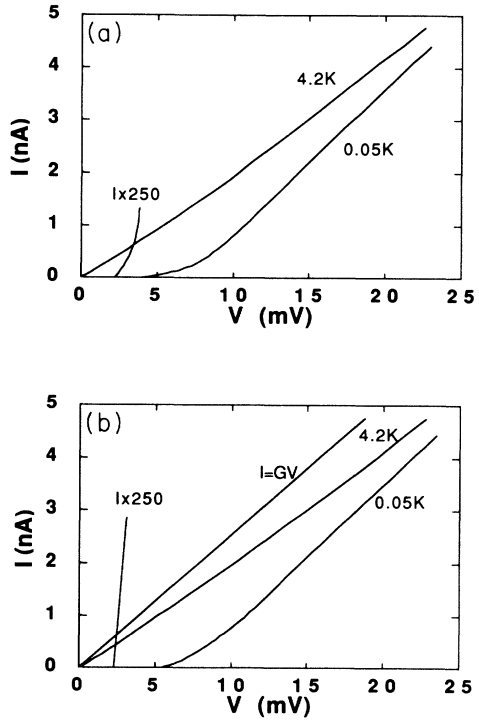


FIG. 6. *I-V* curves for array 2.2 ($N = 19$) at two temperatures. As clearly seen in the curve where the current is magnified 250 times, the current is essentially zero at low bias, $V < V_t \approx 2.0$ mV. At large bias, there is a voltage offset of about 14 mV between the extrapolations of the curves and positive and negative bias. (b) Corresponding theoretical curves. These were calcualted using the formalism and the parameters given in the text.

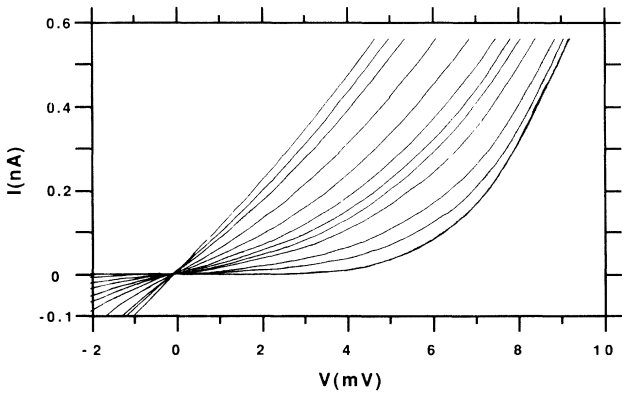


FIG. 7. *I-V* curves for array 2.2 at different temperatures (cf. Fig. 6). Counted from the right (in the upper part of the figure) $T = 0.06$, 0.12, 0.25, 0.50, 0.71, 0.82, 0.94, 1.02, 1.07, 1.13, 1.22, 1.30, 1.43, 1.52, and 1.83 K. The Coulomb blockade region is successively smeared as the temperature is increased. Note that the curves for temperatures ≤ 0.50 K coincide to the right-most curve, which is a little bit broader than the other curves.

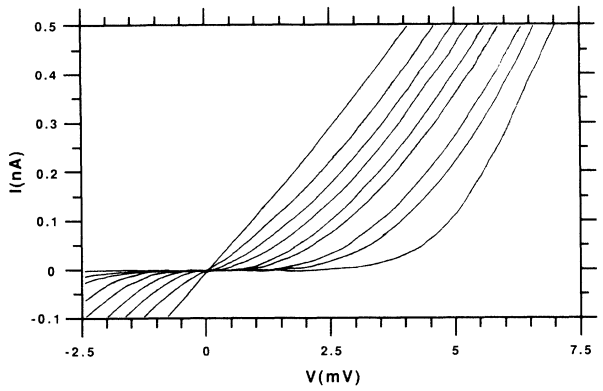


FIG. 8. Smearing of the I-V curve of array 2.2 (cf. Fig. 6) with increasing microwave power with reference to the room-temperature end of the coaxial cable. Traces are given with no microwave power and with decreasing damping of the microwave power: -20, -17, -15, -14, -13, -12, -11, and -10 dBm; $T=50$ mK; $f=687$ MHz.

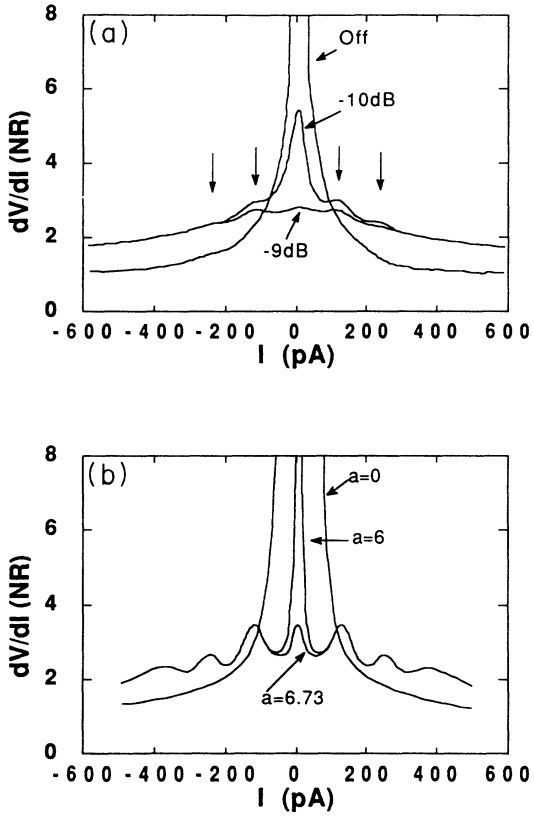


FIG. 9. Differential resistance ($R_d=dV/dI$, normalized to the array resistance) of array 2.2 as a function of bias current and at different microwave radiation powers. (a) Experimental curves for no radiation power and for relative dampings of -10 and -9 dB; $T=50$ mK; $f=0.75$ GHz. The ac modulation of the derivative measruements was about 5 pA rms. (b) Corresponding theoretical curves with relative microwave amplitudes of $a=0$, 6, and 6.73, where a is the normalized voltage amplitude $[a=A/(e/C)]$ of the microwaves. The parameters used were the same ones as for the calculations for Fig. 6(b).

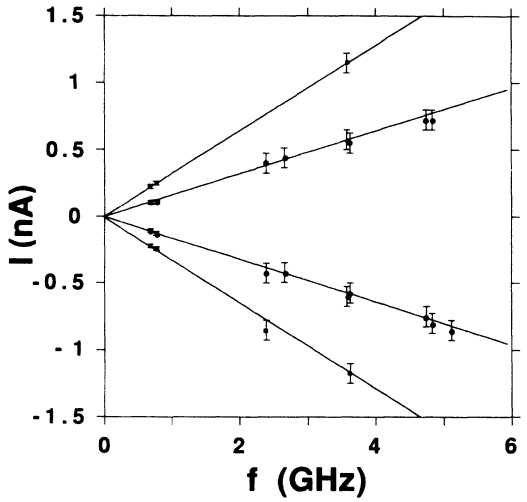


FIG. 10. The locations of the differential resistance peaks (and shoulders) at applied radiation as a function of microwave frequency. Data are given for arrays 1.5 ($N=23$), 2.1 ($N=15$), and 2.2 ($N=19$). The lines are given by $I=nef$ with $n=\pm1,\pm2$.

also measured during the microwave irradiation. Figure 11(a) clearly shows that the dip structure moves in voltage in a G_d-V plot as the microwave power is changed. For comparison, an R_d-I plot for the same array under the same conditions is shown in Fig. 11(b), where it can be seen that the peaks do not move in current when the microwave power is changed.

Even without microwaves, we observe a small structure in R_d around 120 and 240 pA in several plots; one of them is shown in Fig. 12(a).

The temperature dependence of a resistance peak is shown in Fig. 13. Between 0.1 and 0.05 K, the peak does not sharpen considerably. Above 0.1 K, the peak is gradually smeared by temperature. Up to ~0.9 K, there is still some trace of the peak, but at still higher temperatures the peak vanishes completely. The stability of the phase locking to the SET oscillations is remarkable; 0.9 K corresponds to at least a fourth of E_c.

V. DISCUSSION

A. I-V characteristics

All arrays show the characteristic charging effects: the voltage offset of the large-current asymptotes, and the sharp threshold voltage, below which tunneling is blocked by the Coulomb interaction.

A computer program employing a Monte Carlo technique was used to perform numerical simulations[27,28] for a case corresponding to sample 2.2. We used parameters $R/N=210$ kΩ, $C=2.4\times10^{-16}$ F, and $2\Delta(0)/e=0.38$ mV, and $R/NR_{sg}=0.15$ for each junction, $C_0=1.2\times10^{-17}$ F for each electrode between two junctions, and $N=19$. The R/N value is taken from the large-voltage asymptote of the I-V curve divided by N,

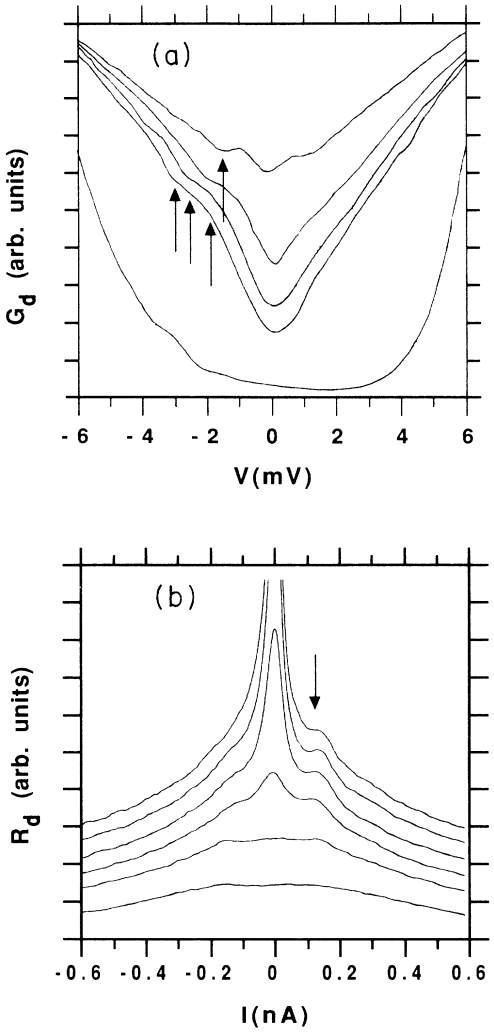


FIG. 11. (a) Differential conductance vs V for different microwave powers ($-\infty$, -19, -18, -17, and -15 dB). The voltage location of the microwave-induced (dip) structure depends on the microwave power. (b) Differential resistance vs I for different microwave powers (-15, -12, -10, -8, and -7 dB). The microwave-induced peaks do not shift in current as the microwave power is increased. Data are given for array 2.2; $T=50$ mK; $f=0.76$ GHz.

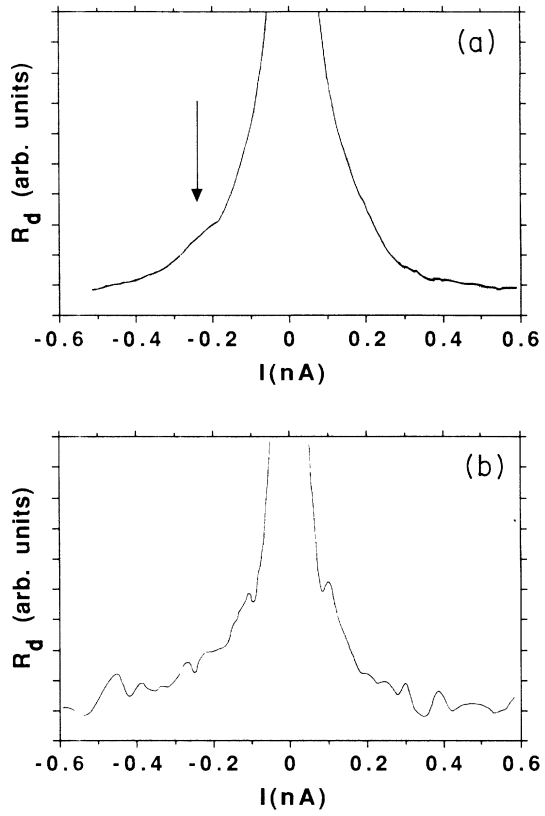


FIG. 12. (a) The dynamic resistance R_d as a function of dc current I for array 2.2 with no microwaves applied. Note that there is a weak structure in the curve, even without any microwave radiation. This may be due to resonances in the circuit as discussed in the text. (b) R_d vs I for array 3.2 ($N=53$) with no microwave radiation. The array is probably not uniform, witnessed, e.g., by the large V_t, cf. Table I, and the relatively strong structure in dV/dI may be due to a Coulomb staircase. Note that this structure is not due to noise since it is reproducible. $T=50$ mK.

the values of C and C_0 agree with calculated values, while the values for $2\Delta(0)$ and R/NR_{sg} agree with literature values. R_{sg} is the assumed subgap resistance for a large or voltage-biased single junction, i.e., a junction where the charging effects are negligible but where superconductivity is taken into account. These simulations can reproduce the large-scale data of the array at both 4.2 and 0.05 K. The only deviations are that the calculated threshold value of 2.4 mV differs slightly from the experimental value of 2.0 mV, and that the shapes of the calculated and the experimental curve above the threshold are slightly different. These small discrepancies between experiment and simulations are probably due to the crude assumptions of a voltage independent R_{sg} and of vanishing background charge Q_0 of the electrodes.

According to theory, the threshold voltage should be $V_t \approx e/\sqrt{(CC_0)}$ if $M \ll N$. Since C and C_0 are approximately constant for all arrays investigated, the soliton-size parameter M is approximately the same for all the arrays. From design parameters, it can be estimated to $M \approx 5$, for sample 1.1 and 1.2, whereas $M \approx 4.5$ for the others. This means that the arrays 1.1–2.2 cannot be exactly regarded as long arrays. This fact should decrease V_t; however, the correction to V_t should be fairly small since the voltage that penetrates the array falls off exponentially. Therefore V_t should be independent of the number of junctions and less than approximately 2–3 mV for all the arrays.

We can compare the different threshold voltages listed in Table I with this numerical value. The arrays 1.1–2.2 show a good agreement, whereas the arrays 3.1–6.2 show considerably higher values. These higher values of V_t might be explained in two different ways. One hypothesis is that these higher values are due to inhomogeneities in

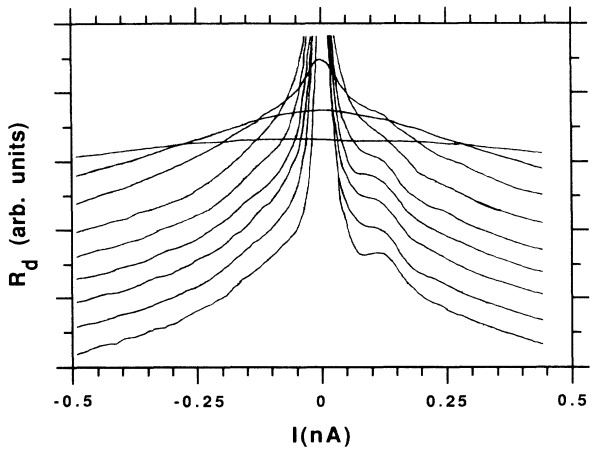


FIG. 13. Temperature dependence of dV/dI vs I for array 2.2 irradiated by microwaves with $f=0.76$ GHz. Curves are given for $T=50$, 100, 175, 300, 500, 750, 920, 1080, and 1300 mK. Note that the resistance peaks are smeared by increasing temperature but can easily be distinguished up to about 1 K, close to T_c of Al. The peak structure is asymmetric for this microwave amplitude. By changing the amplitude slightly, the structure could be made either symmetric or made to have the opposite asymmetry.

the arrays, i.e., a spread in capacitance and resistance values for the junctions in the arrays. If one of the junctions has a considerably lower area, it will dominate and give a higher V_t value if it is located near one of the edges. Note that an inhomogeneity, well inside the array, should not change V_t since the voltage only penetrates $\sim M$ junctions into it. Another possible explanation would be that internal charging effects in the barrier produce a larger V_t. Tunneling via a two-step process in a high-resistance junction will give rise to a Coulomb staircase and a larger V_t. It has been observed that internal charging effects very often occur in high-ohmic tunnel junctions ($R \gtrsim 1$ MΩ); see, for instance, Ref. 35.

Taking a close look at the derivative curves of the "bad" arrays, 3.1–6.2, we observe a Coulomb staircase behavior [Fig. 12(b)]. In fact, we do not observe this behavior [Fig. 12(a)] for the "good" arrays having "reasonable" values of V_t, namely, the arrays 1.1–2.2. This Coulomb staircase behavior can be explained by either hypothesis.

We can also see in Table I that the spread in R and $V_{\rm off}$ for arrays fabricated on the same chip is considerably lower for the "good" arrays than for the "bad" ones, even though the "good" ones consist of fewer junctions. It should be remarked that the "good" arrays 1.1–2.2 were fabricated when the filament of the e-beam lithography instrument was fresh, while the other arrays were exposed using an old filament.

In Table I we have listed the characteristic current for the array, I_0, which is $V_{\rm off}/R$. Since the expression for I_0 contains the product of C and R, it should be independent of the junction area to first order. By comparing I_0 for different arrays on the same chip, we can get information about the tunnel barrier. We can see that I_0 differs by less than a few percent for the good chips. This indicates that the oxidation procedure is reliable and gives only a small spread in the junction parameters.

The smearing of the superconducting-gap structure is not quite understood. However, we observe a clear effect of the gap sharpness as a function of resistance per junction. For arrays with junction resistances below ~ 100 kΩ, we can observe a smeared gap directly in the I-V curve. For arrays with R/N up to ~ 500 kΩ, the gap structure can be seen in the derivative curves; whereas, above ~ 500 kΩ, it cannot be observed at all. We observe this behavior in double junctions also.

The fact that we cannot observe any Josephson supercurrent in these arrays is not surprising. According to the Ambegaokar-Baratoff relation,[36] these arrays should have supercurrents of the order of 10 nA (sample 1.1) or less. For high-resistance junctions (as ours), the supercurrent is expected to be completely suppressed by the temperature and quantum fluctuations.[16]

B. Microwave response

The dynamic resistance peaks were found in three different samples, namely, in 1.5, 2.1, and 2.2. We are confident that these peaks are due to phase locking of the SET oscillations to the external microwaves. The current positions of the peaks remain constant as the microwave amplitude is altered; whereas, the voltage positions of the peaks clearly change with the microwave amplitude. The position in current of the peaks corresponded well to the irradiated frequency according to Eq. (1). This is shown in Fig. 10, where the lines give the current resulting from $n=\pm 1, \pm 2$.

Furthermore, the numerical simulations of the peaks show a good qualitative agreement with the experimental data, although the peaks are somewhat more smeared in the experimental curves. This is at least partially caused by the ac modulation applied to measure the differential resistance ~ 5 pA rms. Additional broadening might also be due to quantum fluctuations ($\hbar/RC$) which are of the order 0.15 K. Possibly, the array is also affected by some pickup of external noise. It should be noted that the resistance peaks were considerably more pronounced at nighttime, when the research activity in the rest of the building was lower, than during daytime.

In spite of the good agreement with the numerical simulations, we should consider whether our results could be attributed to some other cause. We only know of one other effect that could produce the same kind of stable current peaks, namely, Bloch oscillations.[22] However, the fundamental phase locking to Bloch oscillations should give rise to peaks at twice the current. One might argue that the first-order peaks that we observe are due to phase locking to the second harmonic of the Bloch oscillations. This explanation can be contradicted by several arguments. First, the I/e peak is always the largest one; in fact, at higher frequencies this peak alone is visible. Second, if we calculate the Josephson coupling energy, again using the Ambegaokar-Baratoff relation,[36] we obtain $E_J=4.7\times 10^{-25}$ J, which, compared with the charg-

ing energy $E_c = 5.3 \times 10^{-23}$ J, is very small ($E_J/E_c = 0.009$). In this case, and for our nonvanishing value of $\alpha = R_Q/R \gtrsim 0.1$, any Bloch oscillations should be completely suppressed by Zener tunneling.[12]

Since the peaks are constant in current and not in voltage, they cannot be due to the Josephson effect or to photon-assisted tunneling, which both give rise to photon-induced structures separated by voltages determined by the frequency. Furthermore, the voltage separation between the observed peaks is much larger than those corresponding to the Josephson effect, $\Delta V_J = hf/2e$, or to photon-assisted tunneling $\Delta V_{\rm ph} = hf/e$.

The structure at 120 (and 240) pA that was often seen even with no microwave radiation corresponds to a frequency of 0.75 GHz (or its harmonic), where the microwave coupling is good (Fig. 4). This good coupling indicates that there may be a resonance in the system at this frequency. When the array is biased at this current, or at a multiple of it, this resonance might cause self-pumping of the array and give rise to structure in the I-V curve. However, it cannot be ruled out that these small structure in the derivative of the I-V curve could also be traces of a Coulomb staircase.

We also believe that we can explain why phase locking to SET oscillations have not been observed in all arrays. As we have seen in the discussion of the dc-charging effects, the arrays 3.1–6.2 are either nonuniform or internal charging effects are present. Nonuniformity is, of course, harmful for the SET oscillations if it is too large. The charge solitons will be pinned by junctions with a smaller capacitance. According to our simulations, a random scattering of the junction parameters R and C of more than 30% smears the peaks considerably. The internal charging will also alter the form of the solitons and might be harmful for the SET oscillations. Moreover, even if the peaks would be present in the "bad" arrays, it would be very hard to distinguish them from the Coulomb-staircase peaks. These arrays all have a lower characteristic current. This also lowers the current range at which the phase locking should be observable. At the same time, the larger resistance of these arrays increases the noise level.

The arrays 1.1–1.4 are fairly low resistive, and therefore the quantum fluctuations cannot be disregarded. Since the SET oscillation effect is fairly weak, these quantum fluctuations might be enough to wash out the effect. The array 1.5, in which we do see a small effect of phase locking, is also low resistive, but on the other hand it is slightly "longer" (i.e., N/M is slightly larger) than the other arrays on the same chip. This favors time correlation.

Recently, Geerligs *et al.*[37] have reported flat voltage steps in the I-V characteristics of an rf-driven four-junction device. The rf oscillation was coupled to the middle electrode of the device via a gate capacitor. It controlled the flow of electrons through the array. In spite of the low currents ($\sim$pA) of the steps, their results look very encouraging for future applications. It should be noted that their experiment is different from our experiment, since their device cannot perform SET oscillations when driven by a dc field, which is in sharp contrast to our longer arrays.

VI. CONCLUSIONS

We have observed phase locking of SET oscillations to external microwaves in the frequency range 0.7–5 GHz in three different arrays of ultrasmall tunnel junctions. This phase locking showed up as peaks in the differential resistance of the arrays. The locations in current of these peaks, which were independent of microwave power, agreed well with $I = nef_{\rm ext}$ predicted by theory. Furthermore, we have made computer simulations of one of these arrays, obtaining good agreement with experimental data. The peaks that we observe are somewhat weaker than those obtained by the computer simulations.

The main reason for the success of our work is, we believe, the use of arrays of junctions in which the individual junctions are decoupled from the parasitic capacitance of the measurement leads. The parasitic capacitance of the interconnecting electrodes, C_0, was kept as low as possible, in order to obtain a large size of the "charge solitons" which form in these arrays. Our simulations show that, if C_0 is reduced further and the arrays are made longer, the peaks in R_d will become more pronounced. One way of doing this is to use a substrate material with a lower ϵ_r. If we, for instance, were to use quartz instead of silicon, C_0 would be reduced by a factor of 2.5.

If the SET oscillations could be made more pronounced, the phase locking of them to external microwaves would result in horizontal steps in the I-V curve. Then, it may be possible to realize a current standard, which would involve the same type of fundamental relations as the Josephson voltage standard and the quantum Hall resistance standard. The Delft experiment[37] is a good step in this direction.

ACKNOWLEDGMENTS

The generous help of B. Nilsson in fabricating the samples, of P. Davidson in the measurements, and of G. S. Kazacha and O. A. Vasilieva in numerical calculations is gratefully acknowledged. We utilized the Swedish Nanometer Facility and were supported by the Swedish Natural Science Research Council, the Swedish Board of Technical Development, and the Soviet Scientific Council on the High-T_c Superconductivity Problem.

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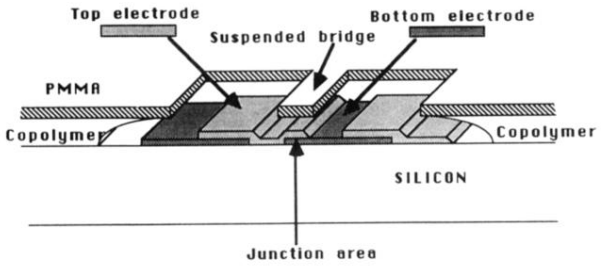

FIG. 1. The method of hanging resist bridges and evaporation from different angles is used to form overlap tunnel junctions as sketched above. The distances and angles are not to scale.

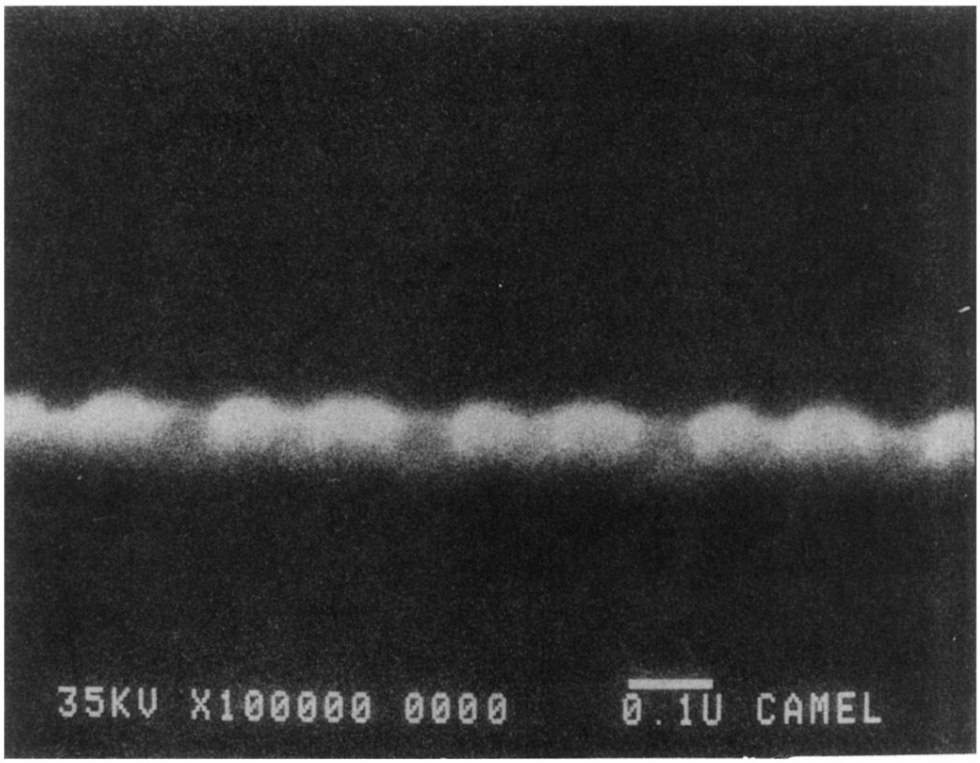

FIG. 3. A scanning-electron-microscope picture of a part of one of the arrays that was investigated.