Schottky-barrier behavior of copper and copper silicide on *n*-type and *p*-type silicon

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The Schottky-barrier heights of Cu and its silicide Cu_3Si on both *n*-type and *p*-type Si(100) have been measured in the temperature range 95–295 K with the use of a current-voltage technique. X-ray photoemission spectroscopy, Rutherford backscattering, and glancing-angle x-ray diffraction were used to monitor the reaction between Cu and Si. Impurity-related energy levels in Si were determined using deep-level transient spectroscopy. Only one level was observed at ~ 0.55 eV below the conduction-band edge upon copper deposition. Silicide formation was found to cause the disappearance of this level and also to have very little effect on the barrier height and its temperature dependence. For both the metal and the reacted silicide phase, the change in the *n*-type barrier height with temperature follows closely the change in the indirect energy gap in Si. The *p*-type barrier height does not exhibit a temperature dependence. These results suggest that the Fermi level at the interface is pinned relative to the valence-band edge. These results deviate from the predictions of models of Schottky-barrier formation based on Fermi-level pinning in the center of the semiconductor indirect band gap. Along with those Schottky barriers reported for metal-Si systems with a wide range in metal electronegativity, the present results show that the barrier height and its temperature dependence are affected by the metal.

I. INTRODUCTION

Almost all theoretical models of Schottky-barrier formation at metal-semiconductor interfaces have been based on the original suggestion of Bardeen,[1] that the Fermi level is pinned at the interface by states in the semiconductor band gap. The nature of these states is clearly one of the key issues in establishing a microscopic understanding of the barrier height. Recently, new models[2] have been proposed based on Fermi-level pinning in midgap by states intrinsic to the interface. In these models the effect of the metal has been neglected and the barrier height has been related to the semiconductor band-structure properties (i.e., indirect band gaps and spin-orbit splittings). We show here that these models, while successful in explaining variations in barrier height with semiconductor properties, do not correctly predict the dependence of the barrier height on temperature for metal (silicide) -silicon systems with a wide range in metal electronegativity. Other models[3] of barrier formation have been proposed based on pinning by states associated with defects in the semiconductor. However, these defect models, which are commonly used to describe pinning of Fermi level on surfaces with submonolayer metal coverages, still provoke much controversy.[4] In an attempt to shed light on the nature of the states responsible for Fermi-level pinning, we have measured the dependence of the barrier height on temperature for copper on silicon in the temperature range 95–295 K using a current-voltage technique.

Copper is known to have a high diffusivity in silicon.[5] The fast diffusion has been shown[6] to be due to singly ionized interestitial Cu. On the other hand, substitutional Cu diffuses very slowly and, consequently, the effective diffusion rate of Cu in Si is determined by the relative abundance of the two species. Early measurements of the solubility of Cu in *p*-type and *n*-type Si have indicated that interstitial Cu gives rise to a single donor level, and that substitutional Cu is a triple acceptor.[7] However, in a recent electron-paramagnetic-resonance study,[5] no donor level of interstitial Cu has been identified. This was attributed to the instability of this defect even at room temperature. The three acceptor levels associated with substitutional Cu (Ref. 8) are generally considered to be at $E_v+0.24$ eV, $E_v+0.37$ eV, and $E_v+0.52$ eV, where E_v is the valence-band edge. The choice of the Cu-Si system then makes it also possible to determine whether deep impurity levels play any role in pinning the Fermi level at the interface.

II. EXPERIMENTAL PROCEDURE

The samples used in this study were prepared by depositing 1000–2000-Å Cu films simultaneously on 0.005-Ω-cm n^+- and p^+-type (100)-oriented Si wafers with 3-μm-thick, 10-Ω-cm n-type (phosphorus-doped) and p-type (boron-doped) epitaxial layers, respectively. The Cu was deposited using dc magnetron sputtering. The deposition chamber was evacuated to 5×10^{-8} Torr prior to the introduction of high-purity (99.999%) argon to a pressure of 10 mTorr. The Cu target was sputter cleaned at a potential of 440–460 V for 30 min prior to sputter deposition. The Cu films were deposited at a target potential of 440–460 V, resulting in a deposition rate of 12–18 Å/sec. The substrates were grounded during film deposition. The resistivity of the Cu films was 2.0–2.5 $\mu\Omega$ cm. Before Cu deposition, the Si surfaces were chemically prepared using a standard chemical cleaning procedure which included a final dip in diluted hydrofluoric acid.[9] The Si wafers were inserted into the deposition chamber immediately after chemical cleaning. Auger spectra from the Si surfaces showed that such a cleaning procedure leaves less than a monolayer of oxygen and carbon on the surfaces.[10] During the same deposition, the following set of samples were made: bare Si samples for x-ray photoemission spectroscopy (XPS), Rutherford backscattering (RBS), and x-ray-diffraction analysis, 5000-Å thermal SiO_2-covered samples with openings for current-voltage (I-V) measurements, and bare Si samples held under a metal mask with openings of 1 and 2 mm in diameter for deep-level transient spectroscopy (DLTS) measurements. For the I-V measurements the deposition was made through a metal mask having 2-mm-diam holes, but the active area of the diodes was defined by oxide openings with diameters of 25, 100, 225, and 400 μm. The samples were processed together and annealed in the temperature range 473–673 K for interfacial reaction in a pressure of 10^{-7} Torr.

XPS was used to monitor the reaction between Cu and Si upon annealing. The measurements were carried out using the monochromatic Al $K\alpha$ line (1486.6 eV) with a resolution of ~1 eV. For these measurements samples were also annealed *in situ* in the analysis chamber at temperatures in the range 473–673 K in a pressure of 10^{-9} Torr. RBS and glancing-angle x-ray diffraction were used to examine the stoichiometry, and to determine the crystal structure of the reacted silicide phase. DLTS measurements were performed at temperatures between 77 and 350 K. Eight different rate windows in the range $(20\text{ ms})^{-1}$–$(2560\text{ ms})^{-1}$ were used to determine the energy positions of the observed levels.[11]

Schottky-barrier-height (SBH) values for n and p-type Si(100) were determined by extrapolating the forward I-V characteristics to zero applied voltage. The extrapolation was made by a linear fit over 2 orders of magnitude or greater of current on the semilogarithmic I-V characteristics. The slope of the linear portion yielded the value of the ideality factor $n=(q/kT)(\partial V/\partial \ln J)$, which represents deviation from ideal diode behavior. The I-V measurements were made on all diode areas with the samples held at temperatures in the range 95–295 K. SBH values were also determined from the activation-energy analysis[12] of $\ln(J_0/T^2)$ versus $1/T$, where J_0 is the saturation current density at zero applied voltage measured in the temperature range 95–295 K.

III. RESULTS

A. Cu-Si(100) interfacial reaction

RBS spectra of samples with 1000 Å of Cu after an annealing at 473 K for 30 min showed the formation of a metal-rich Cu-Si compound with a composition near Cu_3Si. The metal-rich compound has been identified by x-ray diffraction to be the η'- and η''-Cu_3Si phases.[13] We note that Cu precipitates formed by rapid quenching of Cu-doped Si from high temperatures have also been identified by electron diffraction and microscopy to be the η''-Cu_3Si phase, which is the equilibrium phase at room temperature.[14]

For samples with 1000 Å of Cu an annealing at 473 K for 30 min was sufficient to cause the Cu film to fully react with Si to form Cu_3Si. Upon extending the annealing to longer time or higher temperatures, Si was found to segregate at the surface.[15] Upon Ar^+-ion sputtering using 1-keV ions the Si-rich surface layer disappeared and an homogeneous layer (50–80 Å) was found by an XPS probe. From measurements of the integrated intensities of the Cu($2p$) and Si($2p$) core-level signals, and by taking into account the ionization cross sections, its

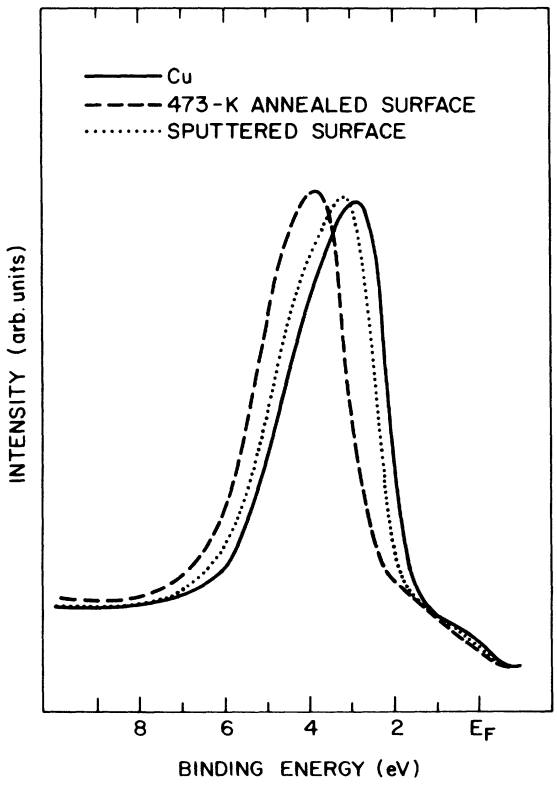

FIG. 1. Valence-band spectra from the 473-K annealed and sputtered surfaces. The stoichiometry of the sputtered surface is estimated to be close to Cu_3Si.

stoichiometry was estimated to be close to Cu_3Si, in agreement with the bulk characterization of the reacted layer using RBS measurements. This sputtered surface will be considered as characteristic of the reacted samples. In contrast, the one which will be referred to as "the annealed surface" is Si rich.

The valence-band spectra from the annealed and sputtered surfaces are shown in Fig. 1. The spectra are dominated by the Cu($3d$) emission. The Cu($3d$) peak shifts progressively toward higher binding energy as compared with pure Cu with increasing Si concentration, and a slight narrowing of the d band is noticed. Similarly, in the annealed surface and in the Cu_3Si, the Cu($2p$) core levels are shifted by 1 and 0.5 eV, respectively, toward higher binding energy. These shifts are common to other near-noble metal-rich silicides.[16] The chemical bonds responsible for silicide formation originate from hybridization of metal(d) and Si(p) states, which results in the formation of bonding and antibonding states below and above the main metal(d) states.[16] The presence of hybridization between Cu(d) and Si(p) states should induce strong modifications in the Si($3p$) density of states. These modifications cannot be seen unambiguously in the valence-band spectra of Fig. 1 since the cross section of Si($3p$) electrons for x-ray photon analysis is very low. However, these modifications can clearly be seen in the Si(LVV) Auger transition (Fig. 2), which is sensitive to the Si($3p$) states[17] and reflects the local environment of the Si atoms when they are in a Cu matrix. Figure 2 shows that the initial Si(LVV) line at 92 eV is split for Cu_3Si into two peaks at 90 and 94 eV. This behavior is similar to that observed in the case of Pd_2Si,[18] where the Auger spectra are interpreted to reflect the redistribution of Si($3p$) states into two components, one comprising the Si(p)—Pd(d) bonding states, ~5.5 eV below the Fermi level E_F, and the other, the antibonding states at E_F. The Auger spectra of Fig. 2 suggest that a similar hybridization of Si($3p$) states occurs in Cu_3Si.

It has been reported[19] that upon the deposition of 5 monolayers of Cu on a clean Si surface at room temperature, the Cu($2p$) core levels and the Cu($3d$) peak shift by 0.4 and 0.5 eV, respectively, towards higher binding energy. These shifts cannot be attributed to a band-bending effect, but they agree with the shifts observed on Cu_3Si surfaces within the experimental uncertainty. Moreover, a similar splitting of the Si(LVV) line was also observed.[19] Recently, Dallporta and Cros[20] have found that splitting of the Si(LVV) line appears even for less than 5-monolayer coverages of Cu. The results of these previous and the present studies suggest that a metal-rich silicide-like phase forms in the initial stage of interfacial reaction during deposition.

B. Schottky-barrier heights

1. *n-type Si(100)*

The forward I-V characteristics plotted in Fig. 3 as a function temperature show examples of the results obtained for as-deposited Cu on n-type Si(100). Above 195 K the samples display a good ideality factor which is independent of temperature. Below 195 K, however, the ideality factor increases with decreasing temperature, reaching a value of 1.25 at 95 K. This temperature dependence of the ideality factor is found to have the form $n = 1 + T_0/T$, where T_0 is a constant, independent of temperature. The value of T_0 for these samples is found to be 18 K. Moreover, the dependence of $\ln(J_0/T^2)$ on $1/T$ is found to be nonlinear in the temperature range measured; however, if $\ln(J_0/T^2)$ is plotted against $1/nT = 1/(T + T_0)$, a straight line is obtained

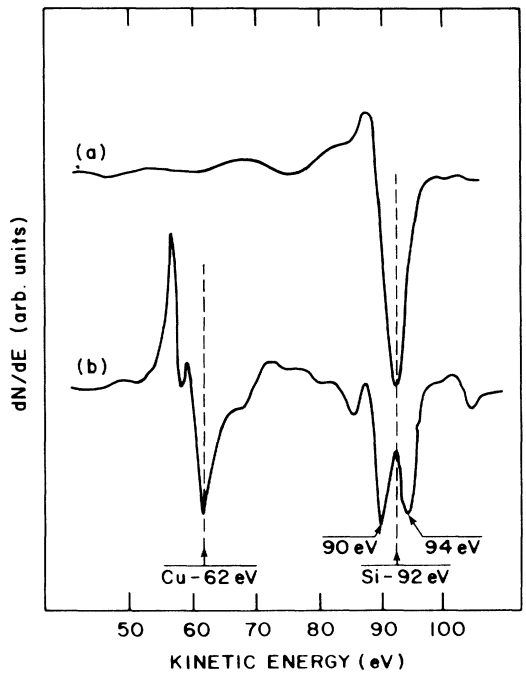

FIG. 2. Si(LVV) and Cu(MVV) Auger lines for (a) the clean Si surface and (b) the reacted Cu-Si surface after annealing at 473 K.

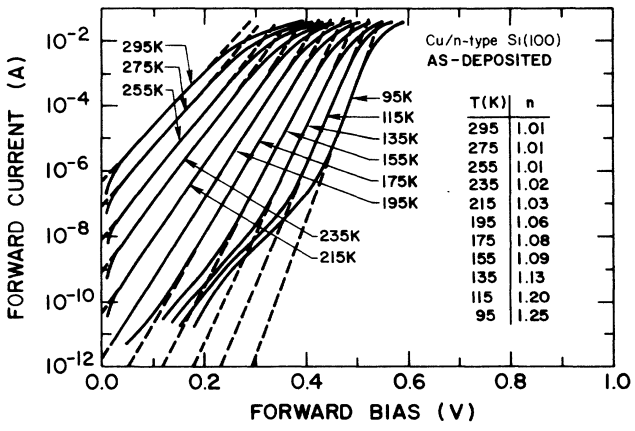

FIG. 3. Forward current-voltage characteristics of Cu on n-type Si(100) as a function of temperature for samples in the as-deposited state. Diode area is 3.974×10^{-4} cm^2.

with a slope giving a barrier-height value at 0 K of 0.68 eV, as shown in Fig. 4, in very good agreement with the 0-K value reported by Arizumi and Hirose[21] for Cu on n-type Si(111). This shows that the saturation current density J_0 can be described by

$$J_0 = A^* T^2 \exp[-q\Phi_{Bn}(T)/k(T+T_0)] , \quad (1)$$

where A^* is the Richardson constant and Φ_{Bn} is the n-type barrier height. Assuming that the temperature dependence of the barrier height is of the form $\Phi_{Bn}(T)=\Phi_{Bn}(0)-\alpha(T+T_0)$, where α is the temperature coefficient of the barrier height, the intercept of the straight line with the ordinate in Fig. 4 then gives the Richardson constant corrected by the temperature coefficient of the barrier height, $A^*\exp(q\alpha/k)$. Using the theoretical value (112 A/K^2cm^2) of the Richardson constant for n-type Si,[22] the temperature coefficient of the barrier height is found to be 3.3×10^{-4} eV/K, in good agreement with the temperature coefficient of the indirect energy gap in Si.[23] This means that the change in the n-type barrier height with temperature closely follows the change in the Si energy gap. This is in agreement with the results of Arizumi and Hirose[21] and of Crowell *et al.*[24] reported for Cu and Au on n-type Si(111). The values of α and $\Phi_{Bn}(0)$ give a value for the barrier height at 295 K in very good agreement with that reported by Thanailakis[25] for Cu on clean, n-type Si(111) using photoelectric measurements, indicating that the Richardson constant is nearly equal to the theoretical value. It is also clear from the open circles shown in Fig. 5 that the barrier height calculated using Eq. (1) decreases with increasing temperature.

Two models have been proposed to explain the inclusion of the excess temperature T_0 in Eq. (1): the interface-state model[26,27] and a doped-interface model.[27] The former describes the interface in terms of a localized energy distribution of interface states, and the latter is a more macroscopic description in which the conversion of the n-type semiconductor near the interface to p-type results in a distribution of dopants which creates a voltage-dependent potential-energy maximum inside the semiconductor. Our results rule out the doped-interface model, since n-type Si is found to be only partially compensated after copper deposition.[28] It is likely that the T_0 anomaly observed here is related to a particular energy distribution of interface states resulting in a charge that causes an increase in the barrier height with forward voltage and a decrease with reverse voltage.[27] It can also be seen from Fig. 3 that an excess-current region of the forward characteristics becomes more pronounced at low voltages as the temperature is lowered below 175 K. This excess current exhibits a small temperature dependence, suggesting that it is likely caused by high-electric-field effects

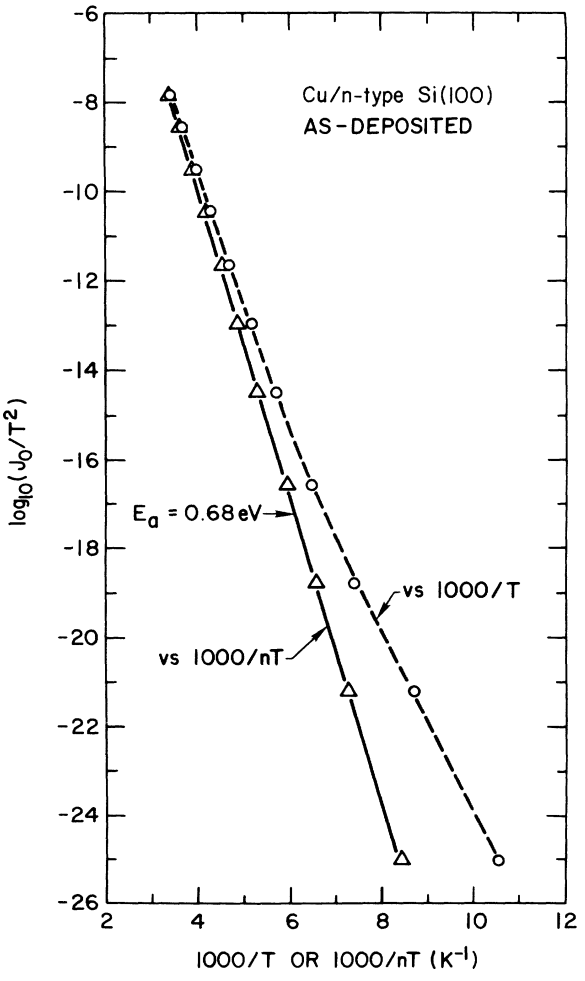

FIG. 4. Temperature dependence of forward current measured at zero applied voltage for n-type samples in the as-deposited state.

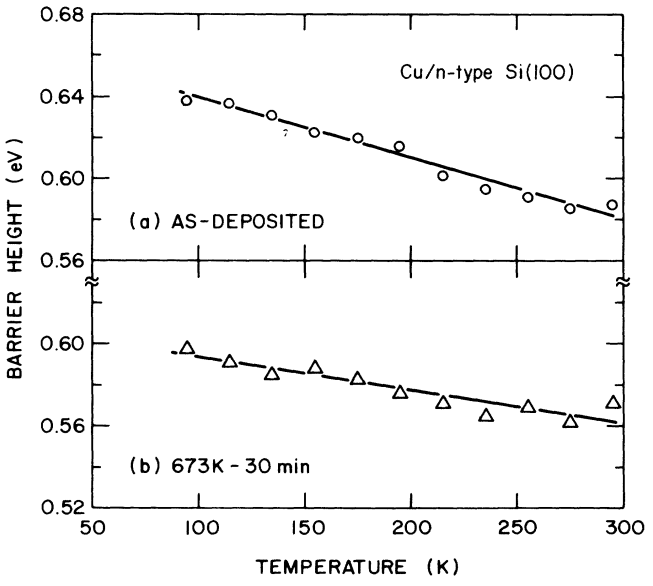

FIG. 5. Change of the barrier height of Cu on n-type Si(100) as a function of temperature for (a) as-deposited samples and (b) samples annealed at 673 K for 30 min. Solid lines: least-squares fits to the experimental data assuming a linear dependence of barrier height on temperature in the temperature range 95–295 K.

near the edges of the contacts.[29] However, this excess current appears to have a very little effect on the temperature dependence of the ideality factor at higher forward voltages where thermionic emission dominates, since if the effect is large, then one would expect T_0 to be temperature dependent, i.e., to increase at low temperatures.[29] This is clearly not the case here. Also, we show below that while this excess current is almost completely removed after annealing the samples at temperatures in the range 473–673 K, the T_0 anomaly is still observed.

The forward I-V characteristics obtained after annealing the samples at 673 K for 30 min are shown in Fig. 6. Results of the annealing at 473 K for 30 min are very similar. The samples display a good ideality factor which, however, increases slowly with decreasing temperature, reaching a value of 1.19 at 95 K. Again, this temperature dependence of the ideality factor is found to have the form $n = 1 + T_0/T$, T_0 having a value of 18 K. In addition, the dependence of $\ln(J_0/T^2)$ on $1/T$ is again not linear, whereas the dependence of $\ln(J_0/T^2)$ on $1/nT$ is linear in the temperature range 95–295 K with a slope giving the barrier-height value at 0 K, as shown in Fig. 7. From the intercept of this straight line with the ordinate, and using the theoretical value for the Richardson constant, the temperature coefficient of the barrier height is found to be 2×10^{-4} eV/K, again in good agreement with the temperatures coefficient of the indirect energy gap in Si. Thus, for the reacted silicide phase, the change in the n-type barrier height with temperature also closely follows the change in the Si energy gap. The temperature variation of the barrier height calculated using Eq. (1) is shown in Fig. 5 by the open triangles. It can be seen from Fig. 6 that a region of the forward characteristics with a high ideality-factor value becomes evident at low voltages as the temperature is lowered below 155 K. The dependence of $\ln(J_0/T^2)$ obtained by extrapolating this low-voltage linear region of the forward characteristics to zero applied voltage on $1/T$ (not shown here) is found to be linear in the temperature range 95–135 K with a slope giving an activation energy of 0.26 eV. This low activation-energy value is evidently associated with recombination current, which causes small departures from thermionic-emission behavior at low voltages and low temperatures.[12]

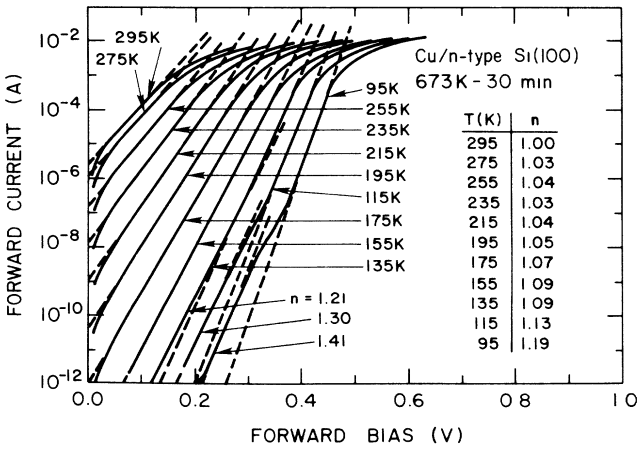

FIG. 6. Forward current-voltage characteristics of Cu on n-type Si(100) as a function of temperature for samples annealed at 673 K for 30 min. Diode area is 12.56×10^{-4} cm^2.

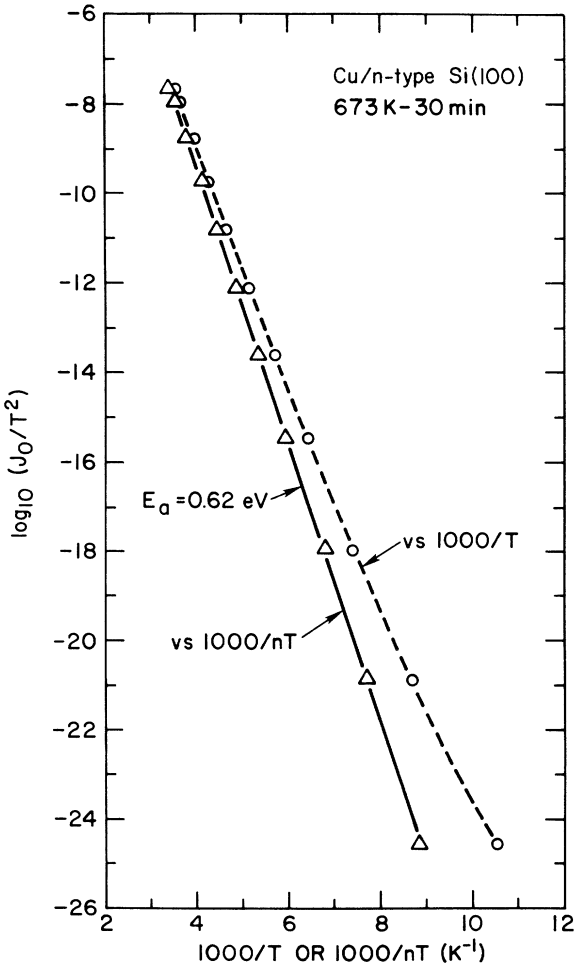

FIG. 7. Temperature dependence of forward current measured at zero applied voltage for n-type samples annealed at 673 K for 30 min.

DLTS spectra of Cu/[n-type Si(100)] samples in the as-deposited state and after annealing at 473 K for 30 min are shown in Fig. 8. Only one level is observed at

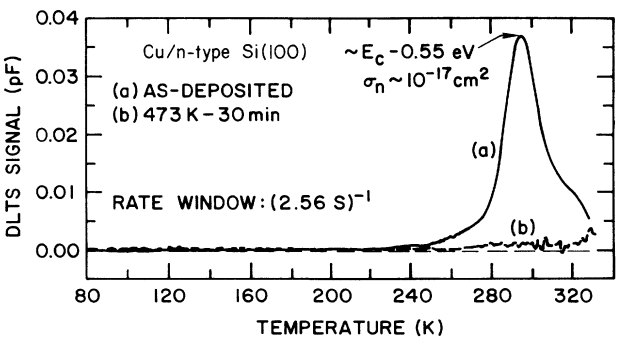

FIG. 8. DLTS spectra from Cu[n-type Si(100)] samples (a) in the as-deposited state and (b) after annealing at 473 K for 30 min.

~0.55 eV below the conduction-band edge with a small shoulder on the high-temperature side at 320 K [spectrum (a) of Fig. 8] upon copper deposition. In the temperature range 280–310 K its electron-capture cross section σ_n is found to be temperature dependent, and has a value of the order of 10^{-17} cm^2. The concentration of this level as determined from the DLTS measurements is about 10^{12} cm^{-3}. Annealing at 473 K for 30 min, however, causes the disappearance of this level, as shown by spectrum (b) of Fig. 8.

2. *p-type Si(100)*

The forward I-V characteristics plotted in Fig. 9 as a function of temperature show examples of the results obtained for the as-deposited Cu on p-type Si(100). The samples display a high ideality factor which, however, remains essentially unchanged in the temperature range 98–290 K. Moreover, in contrast to the n-type samples, the dependence of $\ln(J_0/T^2)$ on $1/T$ is linear in this temperature range, with a slope giving an activation energy of 0.43 eV, as shown in Fig. 10. This value of activation energy is less than the barrier height for Cu on p-type Si(100) at 0 K (0.49 eV). These results indicate that the current is due to thermionic emission in combination with recombination in the depletion region. In fact, if the relation for thermionic emission[12] is used to calculate a barrier height, then the barrier height is found to increase with increasing temperature, as shown in Fig. 11 by the open circles, since departures from thermionic-emission behavior become more pronounced as the temperature is lowered.[12] It is to be noted that the p-type barrier height is not expected to exhibit a temperature dependence, since almost all the change in the Si energy gap is reflected in the change of the n-type barrier height with temperature. It can also be seen from Fig. 9 that an excess-current region of the forward characteristics becomes clearly evident at low voltages as the temperature is lowered below 195 K. A plot of $\ln(J_F/T^2)$ at 0.2 V versus $1/T$ (not shown here) is found to be linear in the temperature range 98–155 K, with a slope giving an ac-

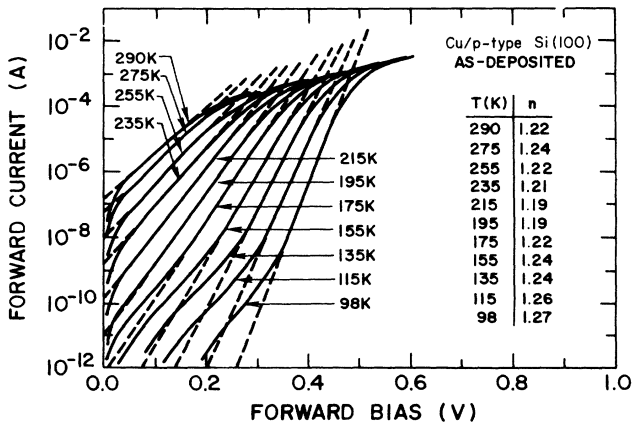

FIG. 9. Forward current-voltage characteristics of Cu on p-type Si(100) as a function of temperature for samples in the as-deposited state. Diode area is 1.31×10^{-4} cm^2.

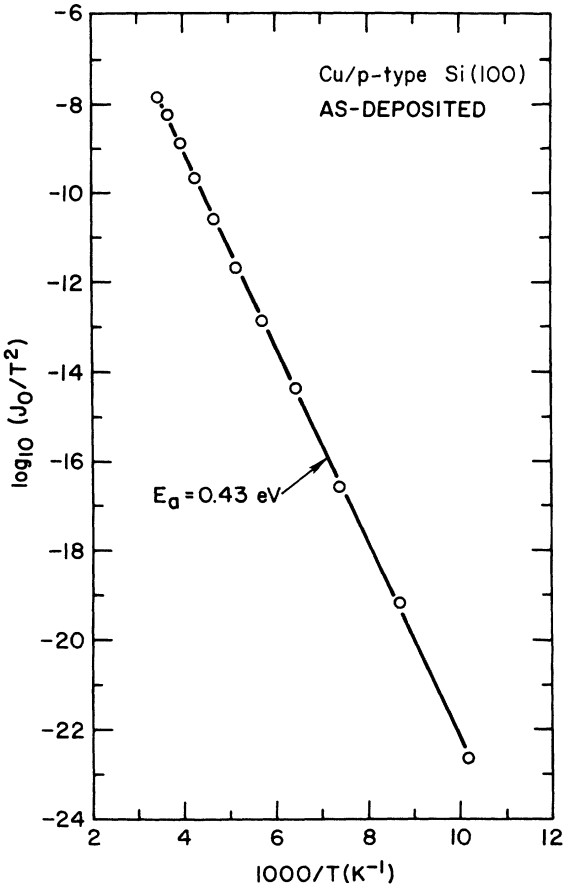

FIG. 10. Temperature dependence of forward current measured at zero applied voltage for p-type samples in the as-deposited state.

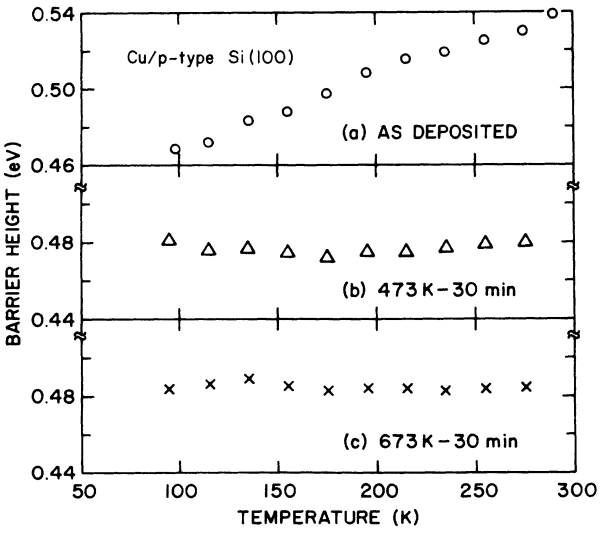

FIG. 11. Change of the barrier height of Cu on p-type Si(100) as a function of temperature for (a) as-deposited samples and samples annealed at (b) 473 K for 30 min and (c) 673 K for 30 min.

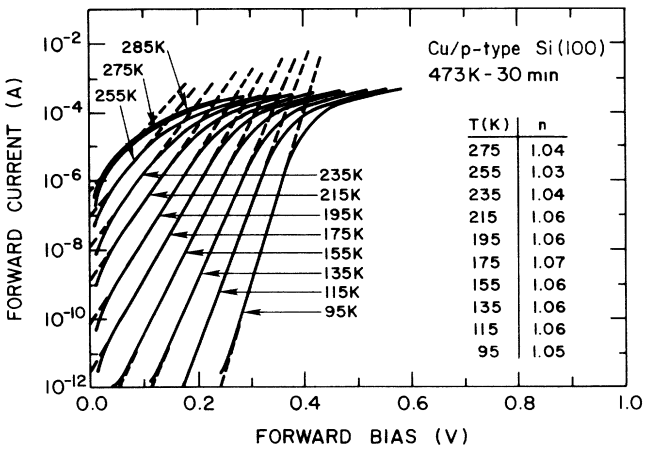

FIG. 12. Forward current-voltage characteristics of Cu on p-type Si(100) as a function of temperature for samples annealed at 473 K for 30 min. Diode area is 1.31×10^{-4} cm^2.

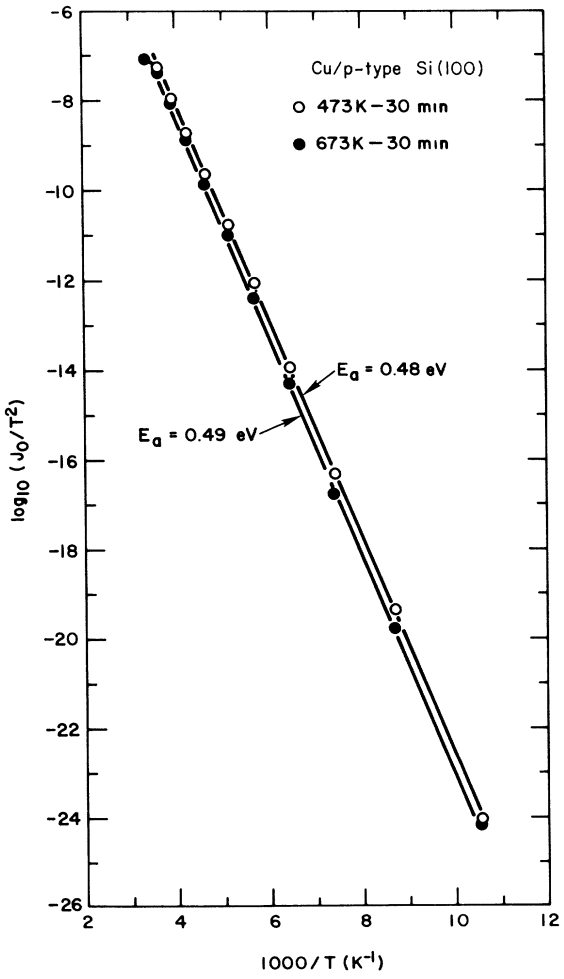

FIG. 13. Temperature dependence of forward current measured at zero applied voltage for p-type samples annealed at 473 K for 30 min (open circles) and at 673 K for 30 min (solid circles).

TABLE I. Values of SBH's at 295 K for Cu on Si(100).

Annealing conditions	Barrier height (eV) Φ_{Bn}	Φ_{Bp}[a]
none	0.60 (0.62)[b]	
at 473 K for 30 min	0.59	0.48
at 673 K for 30 min	0.59	0.49

[a]Values determined from I-V measurements at 275 K. In the as-deposited p-type samples the current is due to thermionic emission in combination with recombination in the depletion region, resulting in unreliable barrier-height values.
[b]Values determined from photoelectric measurements (Ref. 25).

tivation energy of 0.14 eV. This low activation-energy value is again associated with recombination, which causes even more departures from thermionic-emission behavior at low voltages and low temperatures. We show below that this excess thermally activated current is completely removed after annealing the samples at temperatures in the range 473–673 K.

The forward I-V characteristics obtained after annealing the samples at 473 K for 30 min are shown in Fig. 12. Results of the annealing at 673 K for 30 min are very similar. Above 275 K the forward characteristics are nonlinear. Below 275 K the samples display a good ideality factor which is independent of temperature. Moreover, for the 473- and 673-K annealed samples, the dependence of $\ln(J_0/T^2)$ on $1/T$ is linear in the temperature range 95–275 K, with slopes giving the barrier-height values at 0 K, as shown in Fig. 13. The intercepts of these straight lines with the ordinate now yield values for the Richardson constant in excellent agreement with the theoretical value (32 A/K^2 cm^2) for p-type Si.[22] It is also evident from the open triangle in Fig. 11 that in the 473-K annealed samples the barrier height calculated using the relation for thermionic emission does not show a temperature dependence. The temperature variation of the barrier height for the 673-K annealed samples is very similar, as shown in Fig. 11 by the crosses.

DLTS spectra of Cu/[p-type Si(100)] samples in the as-deposited state and after annealing at 473 K for 30 min are found to be similar to those of n-type samples shown in Fig. 8. Values of the n- and p-type SBH's (Φ_{Bn},Φ_{Bp}) at 295 K for the as-deposited and annealed samples are summarized in Table I. Also listed are the barrier-height values reported hy Thanailakis[25] for Cu on clean, n-type Si(100).

IV. DISCUSSION

The SBH data in Table I show that for the as-deposited metal the n-type barrier-height values are similar to those reported for Cu on clean, n-type Si(111). This indicates that a small amount (less than 1 monolayer) of oxygen on the initial Si(100) surface is not sufficient to change the barrier height on clean Si surfaces. On the other hand, we have found[28] that only a few (2–3) monolayers of silicon oxide on the initial Si(100) surface are sufficient to cause a decrease in n-type barrier height of more than 0.1 eV, consistent with the recently reported results for Ti

(Ref. 10) on Si(100).

As can be seen in Fig. 8, an impurity or defect level at $\sim E_c - 0.55$ eV is introduced in the Si band gap upon copper deposition. Deep levels associated with defects in the semiconductor may play a role in determining the barrier height if they are formed at or near the interface[30] and have the high density[31] required for Fermi-level pinning. However, the present results show that the barrier height remains essentially unchanged, while the $\sim E_c - 0.55$ eV level disappears upon silicide formation (see Table I). Furthermore, the defect density is not sufficiently high for Fermi-level pinning. The present results thus clearly indicate that the barrier height is not determined by this level.

Recently, a relationship between barrier heights and semiconductor band-structure properties has been proposed based on the suggestion of Fermi-level pinning in the center of the semiconductor indirect band gap.[2] The p-type barrier height was given by

$$\Phi_{Bp} = \tfrac{1}{2}(E_g^i - \tfrac{1}{3}\Delta) + \delta_m \ , \qquad (2)$$

where E_g^i is the semiconductor indirect band gap, Δ is the spin-orbit splitting (0.04 eV for Si at room temperature), and δ_m is an adjustable parameter, which allows for some shift in Fermi level from the gap center, depending on the metal. A comparison of Eq. (2) with the present SBH data as well as with those reported[32] previously for Cu on elemental and III-V compound semiconductors at 295 K is shown in Fig. 14. The value of δ_m which best fits the data for Cu is $\delta_{Cu} = -0.13$ eV, indicating that Fermi-level pinning occurs below the gap center. Also shown in Fig. 14 are the SBH data for Au on elemental and III-V compound semiconductors. Comparing with the δ_{Au} value of -0.2 eV for Au (Ref. 2) (i.e., Fermi-level pinning occurs well below the gap center), this δ_{Cu} value for Cu is reasonable in view of the fact that Cu is less electronegative than Au. It is therefore evident that the Si barrier height is sensitive to the metal.

Equation (2) predicts that both the n- and p-type barrier heights decrease with increasing temperature and with the same coefficient. This coefficient is equal to one-half the temperature coefficient of the indirect energy gap in Si, $\partial E_g^i/\partial T$. This suggests that the Fermi level at the interface falls in the middle of the indirect band gap, independent of temperature. The present results, on the other hand, show that for the as-deposited metal and the reacted silicide phase, where the Fermi level falls below the gap center, the n-type barrier height decreases with increasing temperature with a coefficient close to $\partial E_g^i/\partial T$, and that the p-type barrier height does not exhibit a temperature dependence (Fig. 11). This suggests that the Fermi level at the interface is pinned relative to the valence-band edge. It is therefore clear that the present results deviate from the predictions of Eq. (2) regarding the temperature dependence of the barrier height, $\partial\Phi_{Bp}/\partial T$. The present results, however, are consistent with those previously reported[21,24,33] for Cu, Au, and $CoSi_2$ on Si(111). Recently, Duboz *et al.*[33] have also shown that for $ErSi_2$ on Si(111), where the Fermi level falls well above the gap center, the change in p-type barrier height with temperature is almost equal to the change in the Si indirect energy gap, and that the n-type barrier height ($\Phi_{Bn} = 0.28$ eV at 77 K) does not exhibit a temperature dependence. This suggests that the Fermi level at the interface is now pinned relative to the conduction-band edge. These results thus show that while Eq. (2) correctly describes the trends in barrier heights with semiconductor band-structure properties, it fails to correctly predict the dependence of barrier height on temperature.

However, we have recently shown[10,34] that for Ti on Si(100), where the Fermi level falls near the gap center, both the n- and p-type barrier heights decrease with increasing temperature and with a coefficient approximately equal to $\frac{1}{2}\partial E_g^i/\partial T$. This is consistent with the predictions of Eq. (2) about the temperature dependence of the barrier height, $\partial\Phi_{Bp}/\partial T$. It is therefore clear that there is a continuous change in the temperature dependence of the p-type barrier height, $\partial\Phi_{Bp}/\partial T$ (from ~ 0 to $\frac{1}{2}\partial E_g^i/\partial T$, and finally to $\partial E_g^i/\partial T$), as the Fermi level at the interface shifts from below to the gap center, and then to above the gap center with changing the metal electronegativity in the sequence Au→Cu→Ti→Er. This then raises an interesting question concerning the effect of the metal on the temperature dependence of the barrier height for other elemental (e.g., Ge) and III-V compound semiconductors. This is a subject worthy of further study.

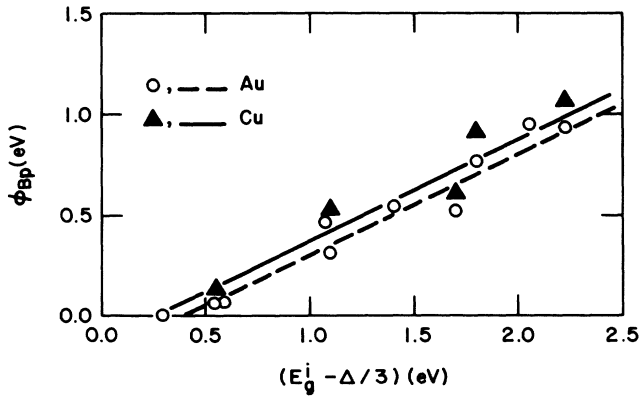

FIG. 14. Comparison of predicted and experimental barrier heights. Solid and dashed lines are Eq. (2), $\Phi_{Bp} = \frac{1}{2}(E_g^i - \frac{1}{3}\Delta) + \delta_m$, with δ_{Au} for Au (open circles) $= -0.2$ eV (Ref. 2) and δ_{Cu} (solid triangles) $= -0.13$ eV.

V. CONCLUSION

The Schottky-barrier height of Cu and its silicide Cu_3Si on both n- and p-type Si(100) has been measured in the temperature range 95–295 K. Only one impurity or defect level is observed at ~ 0.55 eV below the Si conduction-band edge upon copper deposition. Silicide formation is found to cause the disappearance of this level and also to have very little effect on the barrier height

and its temperature dependence. For both the metal and the reacted silicide phase, the change in the n-type barrier height with temperature closely follows the change in the indirect energy gap in Si. The p-type barrier height does not exhibit a temperature dependence. These results suggest that the Fermi level at the interface is pinned relative to the valence-band edge. These results deviate from the predictions of models of Schottky-barrier formation based on Fermi-level pinning in the center of the semiconductor indirect band gap. Along with those Schottky barriers reported for metal-Si systems with a wide range in metal electronegativity, the present results show that the barrier height and its temperature dependence are affected by the metal.

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