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Optical and electrical studies of interface traps in the Si/SiO_2 system by modified junction space-charge techniques

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Interface traps in the Si/SiO_2 system have been examined by adapted-junction space-charge methods. Principal photoionization thresholds, observed at 86 K, are $E_v + 0.38$ eV for excitation of holes from traps, and $E_c - 0.35$ eV and $E_c - 0.8$ eV for electrons. These are assigned to the two levels of the P_b center. The photoionization thresholds differ by 0.05–0.1 eV from P_b levels at $E_v + 0.3$ eV and $E_c - 0.3$ eV, as previously observed by capacitance-voltage (C-V) analysis, deep-level transient spectroscopy, and gated electron-spin resonance (ESR). This suggests a configuration change with electron occupancy, in accord with molecular-orbital calculations. Single-shot measurements of thermal emission rates for holes and electrons in the range 150–185 K show activation energies from 0.29 to 0.36 eV, which are corroborated by deep-level transient spectroscopy. Pulse-train measurements show that capture rates do not exhibit a pronounced temperature dependence. Exponential capacitance transients from emission and capture measurements are discussed with respect to previous C-V and ESR studies which suggested wider P_b levels.

I. INTRODUCTION

The understanding of interface defects in Si/SiO_2 structures has improved significantly during the past few years, primarily due to electron-spin resonance (ESR). Realistic structural models for several important defects have been determined, with special emphasis on trivalent silicon defects at the interface, termed P_b centers.[1,2] Quantitative correlation of physical, chemical, and electrical properties indicates that P_b centers are the defect source of about half of the interface states.[3] However, the study of detailed electrical and optical properties of P_b centers is far from complete, and there are still numerous uncertainties regarding the electronic properties of all interface states throughout the band gap.

Over the same time span, there have also been important advances in the electrical and optical characterization of bulk traps in Si, especially by use of junction space-charge techniques.[4,5] These have contributed to considerable improvement in the understanding of the electronic properties of bulk defects. In the present work, we have applied some of these techniques, slightly modified for the metal-oxide-silicon (MOS) test structure, to learn more about the electronic properties of interface traps. The application of modified junction space-charge techniques to MOS systems has several advantages, but is not entirely unprecedented. A brief comparison of the junction and MOS methods for trap study has been given by Nicollian and Brews.[6] In corollary, bulk traps have been studied with the MOS technique by careful ion implantation.[7] An important advantage of MOS test samples is the lack of current flow, which on the one hand somewhat simplifies the application of junction techniques to the MOS case, but on the other, implies some complication which will be briefly discussed later.

The apparent spectrum of interface trap levels within the forbidden energy gap is a rather featureless U-shaped continuum when the total density of traps is low. However, with higher densities, richer structure has been observed by several investigators, including peaks at various energies.[8] Most recently, with trap densities $\geq 10^{12}$ cm^{-2} on (111) Si, two peaks are found at 0.3 and 0.85 eV above the valence band, superimposed on a U-shaped background. These peaks were first clearly observed with deep-level transient spectroscopy (DLTS) (Ref. 9) and later quantitatively correlated with similar peaks from electric-field-controlled ESR.[10] Other groups have also examined the nature and band-gap distribution of interface traps by ESR and capacitance-voltage (C-V) analysis.[11–13]

Optical properties of uncharacterized interface traps in the Si/SiO_2 structure have been examined several times previously.[14–16] The general approach has been the use of sub-band-gap monochromatic light to induce electronic transitions between the localized states of interface defects and the extended states of silicon. These transitions were detected by monitoring either photocurrent or photocapacitance transients in MOS devices. Data

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analysis yielded interface-state distributions and photoionization cross sections. However, the above optical studies were conducted without knowledge of P_b centers, and usually on fully processed MOS devices which did not have identifiable P_b concentrations.

A number of optical studies of limited scope have been specifically directed to P_b centers. In a recent study, optical absorption by P_b centers was measured by electroabsorption spectroscopy with sub-band-gap monochromatic light on MOS capacitors.[17] The results yielded an interface-state distribution with a band of states centered near $E_v+0.3$ eV. The study also concluded that optical absorption by singly occupied P_b centers is dominated by hole emission, in contrast to the dangling-bond defect in amorphous silicon where electron photoemission dominates.[18] With photothermal deflection spectroscopy, it has also been determined that the optical cross section for electron emission from the singly occupied P_b center is small (i.e., $\ll 10^{-17}$ cm^2).[19] P_b centers have also been detected by optically induced spin-dependent recombination[20] and by optically detected magnetic resonance,[21] although these studies did not establish the distribution or optical properties of the deep levels. Finally, limited results are available from photocurrent transient spectroscopy, which reveal substantial photoionization of P_b centers with 0.37-eV photons.[22]

The present study extends these earlier measurements with more comprehensive data on the optical and electrical properties of P_b centers as measured by modified junction space-charge techniques. Photoionization spectra and thresholds for holes and electrons in interface traps have been determined, as well as absolute values for optical cross sections by use of photocapacitance, which is much more sensitive than the usual ESR approaches. Single-shot electrical methods, including pulse-train techniques and DLTS measurements have been used to examine carrier capture and thermal emission processes. The analysis of the investigations was greatly simplified since most of the optical and thermal capacitance transients were exponential. It was therefore possible to measure the enthalpies of interface traps in both n- and p-type samples.

II. EXPERIMENTAL TECHNIQUES

All measurements here were performed on MOS capacitors fabricated on (111)-oriented Czochralski-grown silicon of, p- and n-type, $\geq 30\ \Omega$ cm. The samples were selected from those remaining from previous studies,[2,9] in order to improve correlation of results. The samples had been oxidized in such a way as to achieve a high density D_{IT} of interface traps in general and P_b centers in particular. A typical sample is shown in Fig. 1; the small Al dots are for electrical or optical measurements; the large Al capacitor is for gated ESR.

The optical experiments were performed in a liquid-N_2 cryostat with optical windows. A Kratos single-grating monochromator with a 1000-watt tungsten lamp, in conjunction with suitable filters, was used as a light source. Spectral distributions were measured with a vacuum double-grating monochromator. Most of the spectral distributions were studied employing the initial slope technique[23] in measuring the change in the capacitance due to the illumination with monochromatic light. The intensities were chosen such that the response times were of the order of seconds.

All electrical measurements were performed in a commercial DLTS equipment from Polaron; this equipment served for single-shot measurements, for pulse-train capture studies, and of course, for DLTS. Supporting ESR measurements were made on Varian Associates E-line Century x-band spectrometers. Additional details on samples and experimental techniques are given in the references cited or in the appropriate sections to follow.

III. EXPERIMENTAL RESULTS

A. Preliminary characterization

The samples used for this study were given a preliminary examination by conductance-voltage (G-V) and capacitance-voltage (C-V) analysis at 300 K, to establish the broad features of the traps present. High-frequency (1 MHz) and low-frequency (10 Hz) C-V and G-V curves for a p-type sample are shown in Fig. 2; other p-type samples and n-type samples were very similar. The G-V curves show a large peak in the depletion region, overshadowing losses elsewhere, and demonstrate the dominance of interface traps, as opposed to bulk traps. The band-gap energy-level spectrum of interface traps is shown in Fig. 3; the results from previous C-V, DLTS, and ESR measurements are plotted together on the same scale. The two P_b peaks account for about half the total integrated trap density ($Q_{IT} \approx 8\times10^{12}$ cm^{-2}) between

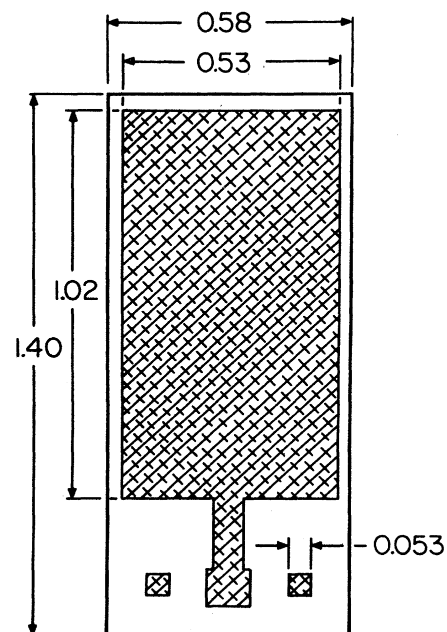

FIG. 1. Typical silicon MOS test chip used for electrical, optical, and ESR measurements. Dimensions are in cm.

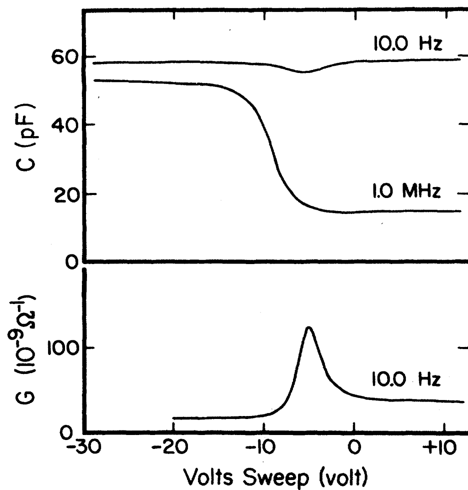

FIG. 2. Wide-range C-V and G-V curves for p-type (111) Si chip. C-V trace was taken at 10 Hz, lower C-V trace at 1 MHz; G-V trace at 10 Hz; room temperature.

$E_v+0.2$ eV and $E_v+0.9$ eV. The n-type samples had a slightly lower integrated concentration, about 5×10^{12} cm^{-2}. It is worth mentioning that the energy resolution of interface-state distributions obtained by C-V and DLTS is about $3.5kT$ and $2.5kT$, respectively, i.e., no better than about 0.1 eV for C-V measurements at room temperature.[24] Furthermore, the entropy properties of interface traps can have a considerable influence on measured energy distributions.[25]

Because of the very high interface trap concentration, there is a great stretchout of the C-V curves. Even though it is not difficult to produce accumulation or depletion conditions, as reflected by carrier capacitance at 1 MHz, it is extremely difficult to fill or empty most of the interface traps over a wide range of energy within a reasonable time interval, evidenced by the very shallow dip in the low-frequency C-V curve. Integration of the curve shows that to fill and empty traps between $E_v+0.15$ eV and $E_v+1.0$ eV in p-type samples requires a gate voltage range of -60 to $+40$ V. Repeated application of such voltages would have quickly destroyed the samples, of which only a very limited number were available. In the experiments to be described here, it was therefore generally not feasible to achieve extreme trap occupancies, nor was it feasible to derive wide-range bias versus band-bending functions at the required low temperatures. Care was taken to achieve sufficiently accumulated or depleted conditions to fulfill the needs of a meaningful measurement. Possible effects of these experimental conditions on data analysis and interpretation are presented in pertinent sections to follow.

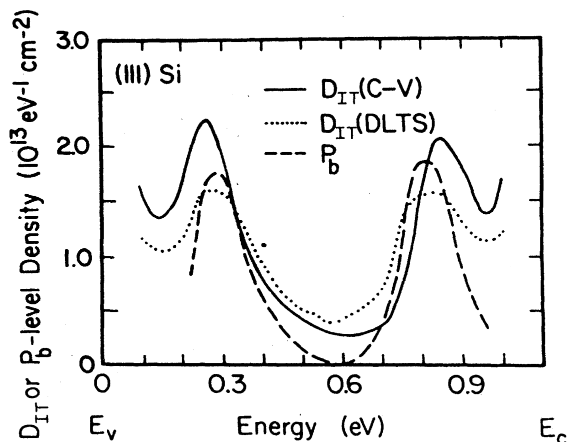

FIG. 3. Band-gap density of interface trap levels in p-type Si, determined by electrical (D_{IT}) and ESR (P_b) methods.

B. Low-temperature C-V analysis

Typical high-frequency (1-MHz) C-V curves of n-type samples are shown in Fig. 4 for different temperatures. The curves were obtained by sweeping the gate voltage from $+5$ to -15 V and back to $+5$ V with a rate of 100 mV/s. Several features are of interest. (1) The depletion regime is shifted toward higher positive bias with decreasing temperature; (2) the depletion regime is stretched out over a wider range of bias with decreasing temperature; and (3) below 260 K, a ledge appears in the deep depletion regime. The shift toward positive bias is due to the rise in the Fermi level with reduced temperature in this n-type sample. Thus, more net negative charge is stored in the interface traps; and a more positive bias is required to produce a specific band-bending condition. If D_{IT} were constant across the band gap, this would be the main effect of lowered temperature on the overall appearance of the curves. However, D_{IT} is not uniform, as seen in Fig. 3. Thus, a rise in the Fermi level brings increasingly more interface traps into play through the range 0.6–0.85 eV above the valence band. This accelerating density of occupied traps causes increasing stretchout of the C-V curve.[6]

The situation described verbally above has been developed in a comprehensive theoretical treatment.[26] It is found that the observed capacitance C is given by

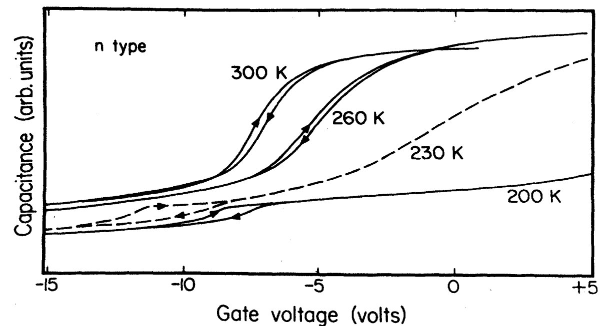

FIG. 4. High-frequency (1.0 MHz) C-V curves for n-type chip at various low temperatures.

$$\frac{C}{C_{\mathrm{ox}}}=\left\{1-\frac{C_{\mathrm{ox}}}{qD_{\mathrm{IT}}+C_{\mathrm{ox}}}+\left[\left[\frac{C_{\mathrm{ox}}}{qD_{\mathrm{IT}}C_{\mathrm{ox}}}\right]^2+\frac{2C_{\mathrm{ox}}^3(V_{\mathrm{FB}}-V)}{qN_d\varepsilon_s(qD_{\mathrm{IT}}+C_{\mathrm{ox}})}\right]^{1/2}\right\}^{-1},$$

where C_{ox} is oxide capacitance, q is electron charge, D_{IT} is band-gap density of interface traps, N_d is donor density, ε_s is oxide permittivity, V_{FB} is flatband voltage, and V is bias. The same researchers have also observed low-temperature *C-V* behavior in a metal-insulator-semiconductor (MIS) capacitor, and have thereby verified the theory over a wide range of parameters.[27] The curves of our Fig. 4 are very similar to a narrow-range portion of their curves. It is possible to utilize the shift and stretchout *per se* to study interface traps;[12] however, that approach is less direct and less sensitive for the transient phenomena reported here.

The ledge in the deep depletion regime below 260 K emerges because the electron emission rate is too slow for the sweep rate of 100 mV/s.[6] The size (with respect to the capacitance) and the position (with respect to the gate voltage) of the ledge do not depend on the accumulation voltage in the range between 0 and +30 V. This implied that at a constant temperature, the *C-V* curve did not change markedly above a certain accumulation voltage due to the recharge of the defect which caused the ledge, whether or not the measurements were performed in thermal equilibrium or after illumination. At 160 K this was valid for any voltage above 0 V. Thus, the *n*-type samples were usually run with accumulation voltage around +5 V.

Since the hysteresis is caused by electron emission, the position and size of the ledge depend on the sweep rate of the gate voltage.[6] The size and position of the ledge are rather independent of the sweep direction, i.e., whether the voltage sweep starts at +5 V going to −12.5 V and back or whether it starts at −12.5 V and goes to +5 V and back. For convenience the *C-V* curves were always taken by sweeping the gate voltage from negative values to positive values and back.

If the *n*-type MOS device is kept in depletion (i.e., −12.5 V) at sufficient high temperature after the initial accumulation, the capacitance will relax in darkness towards equilibrium because the defects are thermally emitting their charges and therefore a change in capacitance is observed. Since the capacitance of the *C-V* ledge increases with time and the sample in this example is *n* type, this means that either electrons are emitted or holes are captured. The capacitance increase depends on the temperature and can be accelerated at low temperatures by momentary illumination with sub-half-band-gap light. This implies that *electrons* are emitted and *not* holes, i.e., that the sample is not in inversion at −12.5 V. This is shown in Fig. 5, where two *C-V* curves are presented. Both were taken at 160 K in darkness, one after about 3 min in darkness and the other after illumination with white light. The shape of the ledge after illumination did not depend on the photon energy, i.e., whether above-band-gap, sub-band gap or sub-half-band-gap light was used, as long as the photon energy was larger than about 0.4 eV and steady state was achieved. Since steady state was readily obtained even with sub-half-band-gap light it has to be assumed that the upper capacitance curve of the ledge in Fig. 5 corresponds to the case where most of the upper P_b levels are empty.

When the device was inversion biased to −30 V at 160 K, the depletion part of the *C-V* curve shifted to more negative voltages. The original *C-V* curve could be restored by heating the sample to 230 K for about 3 min. These effects did not change the size or position of the ledge. At 100 K the *C-V* curves showed features similar to those presented by Chang *et al.*[12] In darkness (i.e., without illumination prior to measurement) the *C-V* curve showed no ledge at this temperature, and no change was observed with time. Similar considerations apply for *p*-type samples. Apart from the polarity no qualitative differences were observed.

C. Optical measurements

The spectral distribution of the photoionization cross section was measured for holes in *p*-type samples and for electrons in *n*-type samples at about 80 K using the initial slope technique.[23] It was found that absorption in air considerably influenced the photoionization thresholds and that all spectral distributions therefore had to be measured with a vacuum spectrometer. The bias of the sample was always chosen such that the measurements were executed in deep depletion, well within the ledge. Care was taken that for every measuring point, the level to be studied was equally occupied by majority carriers, since the observed threshold energy can be affected by inadequate filling of the level. In most measurements this was achieved by switching the sample from accumulation. It was found that the capacitance due to the large signal amplitude increased almost linearly with time at the very beginning of the transient when illuminated with

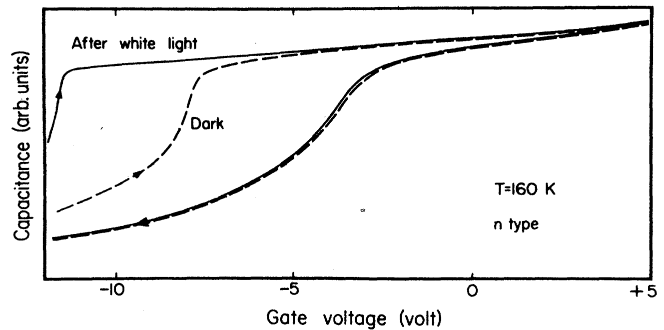

FIG. 5. Light-enhanced relaxation of capacitance (——) toward equilibrium value by the emptying of interface trap levels in *n*-type samples previously subjected to accumulation bias; temperature 160 K. *C-V* curve in darkness without previous illumination (— — —).

monochromatic light of variable wavelength and that the change in capacitance was persistent when the light source was switched off. It has been shown previously[23] that the slope of the capacitance change due to an almost completely occupied level is proportional to the photoionization cross section of the excited charge carrier. If the center is only partially occupied, a different proportionality factor is needed. As long as the initial occupancy of the center is constant, the photoionization spectrum is readily measured by the initial slope technique.

The spectral distribution measured in p-type samples is shown in Fig. 6. The threshold is at 0.38 eV. At about 38 meV above threshold a subsidiary increase of the cross section is observed, suggesting that an additional excitation process is contributing to the spectral distribution. Since the spin-orbit split-off band lies about 42 meV below the valence band gap, it seems rather probable that the extra contribution is due to the split-off band. Above about 0.6 eV, the spectral distribution is completely smooth, indicating that a possible excitation involving the second trap peak level of the p-type Si is much weaker than the excitation of the first trap peak level. The spectral distribution of e_p^0 with a rather well-defined threshold energy suggests that a possible complication of the initial slope technique due to an energy distribution of the interface states is obviously not as disturbing as one might have expected.[28]

All samples showed some photosensitivity for photon energies smaller than 0.38 eV. Our equipment did not allow us to measure spectral distributions accurately in this energy range because of the small signal and the low intensity of our light sources. We can therefore not decide whether the signal for these photon energies is due to stray light of higher energy or caused by carrier excitation in the sample at these particular energies. Previous studies by photocurrent transient spectroscopy on n-type and p-type MOS capacitors have shown nearly complete depopulation of P_b centers after about one hour by 0.37-eV photons of a He-Ne laser at low temperatures (i.e., ≤ 56 K).[22] Similar phenomena in the case of bulk traps have been ascribed to excited states. Such bound-to-bound transitions cause a capacitance change if the excited charge carriers are then thermally excited into the valence or conduction band, as the case may be.[29] In the MOS system, such excitations might also involve the continuum states.

The spectral distribution of the photoionization cross section for electrons e_n^0 is shown in Fig. 7. The curve shows two main threshold energies. One is at about 0.35 eV and the second one at about 0.8 eV. As in the case of the hole spectra, there is some optical excitation below the first main threshold, presumably with analogous origins.

The second threshold at about 0.8 eV was carefully substantiated, and represents excitation of electrons into the conduction band, as seen from the increase of the capacitance due to illumination. This threshold can be explained by two different excitation processes if it is assumed that some of the P_b centers remain singly occupied during application of the accumulation bias: (1) photoexcitation of electrons from the lower trap level into the conduction band and (2) photoemission of holes from singly occupied centers and subsequent photoexcitation of the electrons from the doubly occupied center.[15] The symmetrical position of P_b levels in the gap precludes distinction between the two possibilities on an energy basis. Whichever explanation is correct, however, it is of interest that a similar higher-energy transition is not ob-

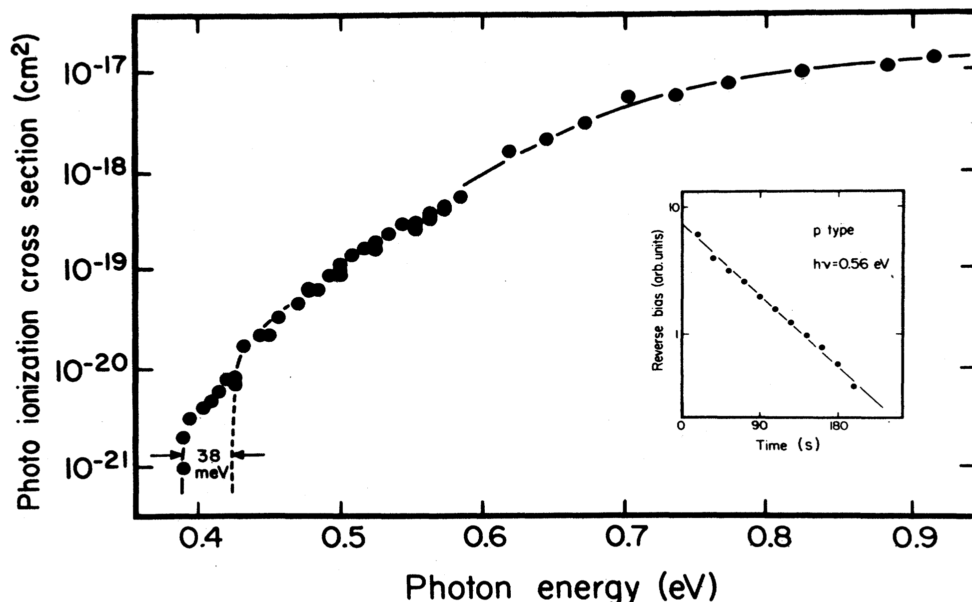

FIG. 6. Spectrum of photoionization cross sections of interface traps in p-type Si; temperature 86 K. The inset shows the optically initiated transient depletion-bias increase at constant photocapacitance.

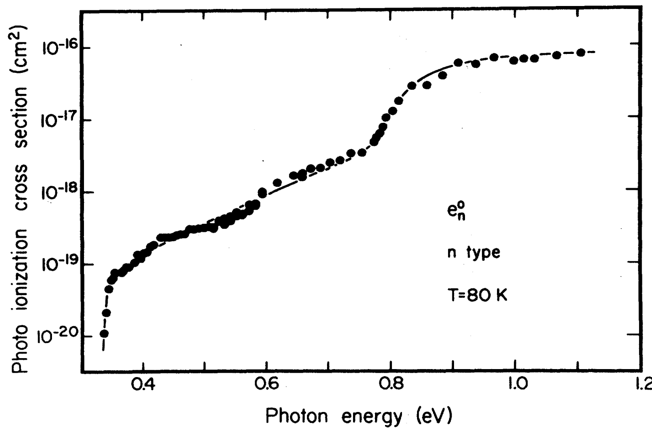

FIG. 7. Photoionization cross-section spectrum of interface traps in n-type Si; temperature 86 K.

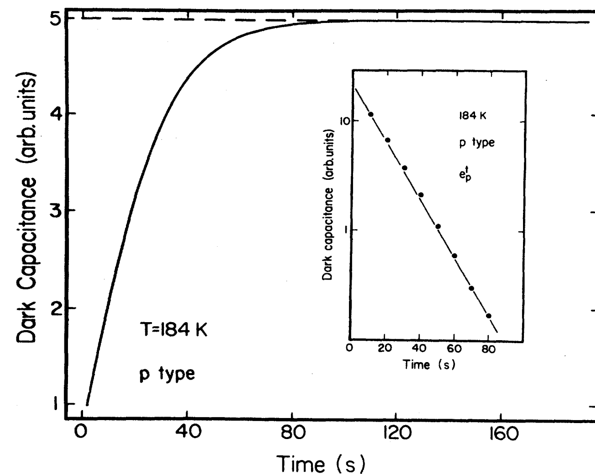

FIG. 8. Single-shot transient capacitance increase; p-type Si. First accumulated at -5 V, 230 K, then cooled to 184 K, then zero biased.

served in p-type Si, since the ionization curve is otherwise very similar to n-type. A comparison of the absolute cross-section values presented in Figs. 6 and 7, however, suggests that the second threshold probably is caused by photoexcitation of electrons from the lower trap level.

Exponential optical decays were obtained at low temperature when instead of the depletion bias the photo capacitance was kept constant. The inset of Fig. 6 shows an example of a p-type sample which was obtained for 0.565-eV light causing an increase of the depletion bias with an exponential transient over more than 1 order of magnitude. Since the number of photons striking the sample in this example was about 3.8×10^{16} $cm^{-2}\,s^{-1}$, a value of 3.6×10^{-19} cm^2 is obtained for the photoionization cross section of holes at 0.565 eV.

D. Electrical measurements

Thermal emission and capture were measured in both n- and p-type samples by single-shot techniques.[5] Thermal emission of holes from the lower band-gap level in p-type samples was investigated by first heating the device to 230 K with -5-V accumulation bias and then cooling the sample to the temperature at which the thermal emission rate was measured. When the capacitance had stabilized, showing that the sample had reached the desired temperature, the device was zero biased, resulting in a fast decrease of the capacitance followed by a much slower exponential increase. A typical transient obtained for 184 K is shown in Fig. 8. In the inset the increasing capacitance signal is plotted semilogarithmically, showing that the transient is a single exponential over at least 2 orders of magnitude. From the slope of the semilogarithmic plot the absolute value of the hole emission rate is readily calculated for this particular temperature, giving $e_p^t(184.3\text{ K})=6\times10^{-2}\text{ s}^{-1}$. The positive capacitance transient proves that the signal is due to hole emission, not electron emission. As mentioned earlier at these temperatures and voltages we have good reasons to believe that no inversion layers are formed and that an increase in capacitance due to thermal generation of minority carriers can therefore be excluded. An Arrhenius plot of hole emission rates e_p^t obtained at different temperatures is presented in Fig. 9, giving an activation energy of 0.35 eV. This energy is unspecified; but, since e_p^t/T^2 is plotted versus $10^3/T$, it is equal to the enthalpy if the hole capture is temperature independent. To complete the analysis, it is necessary to know the temperature dependence of the capture process.

It should be noted that the accumulation bias (-5 V) is probably not sufficient to empty all centers completely, as explained earlier. However, the bias was chosen to empty the lower level adequately; and further, great care was taken to assure the same initial occupancy throughout the experimental run. As seen from Figs. 4 and 5 this was easily achieved since the size and position of the ledge was not dependent on the accumulation bias.

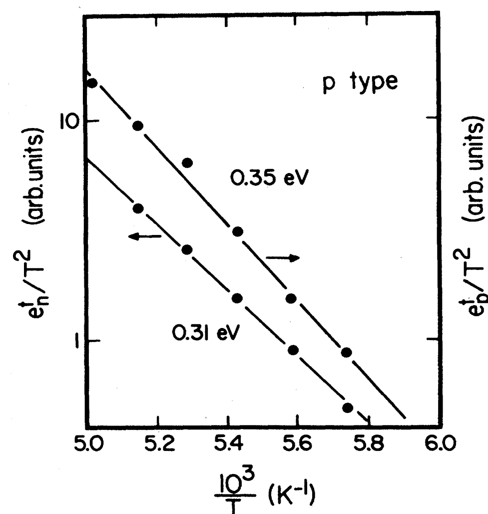

FIG. 9. Arrhenius plot of thermal emission rates of holes (●) and electrons (●) from interface traps in p-type Si, derived from several tests like those in Figs. 8 and 10, over a range of temperature.

Some further aspects of this procedure are discussed later.

Thermal emission of electrons from the doubly occupied level in the upper half of the band gap in p-type samples was likewise done by a single-shot measurement. The sample was put into deep depletion (+ 5 V) at about 230 K and then cooled to 189 K. The sample was then zero biased, resulting in a fast capacitance increase due to the voltage change, followed by a slower capacitance decrease, Fig. 10. The decrease suggests that the signal is due to thermal emission of electrons and not holes, since in the latter case a capacitance increase would be expected. Plotting the decrease of capacitance semilogarithmically (as shown in the inset of Fig. 10) gave a single exponential over 2 orders of magnitude. From the slope of this plot, the thermal emission rate of electrons e_n^t for the upper level was calculated. Performing these measurements at different temperatures and plotting the electron emission rate e_n^t/T^2 versus $1/T$ resulted in a straight line with an activation energy of 0.31 eV, Fig. 9.

Measurements of thermal electron emission from the upper level were also executed with n-type samples. Instead of heating to 230 K as in the case of p-type samples, the n-type samples were first warmed to 180 K under accumulation bias (+ 10 V), and then cooled to the temperature at which the study was performed. When the temperature had stabilized the diode was zero biased, and the time dependence of the capacitance increase recorded. All transients appeared singly exponential over more than an order of magnitude. Performing these measurements at different temperatures and plotting the electron emission rates e_n^t/T^2 in an Arrhenius plot (Fig. 11) resulted in a straight line with an activation energy of 0.29 eV, in good agreement with similar results on p-type samples.

Investigation of the hole emission from the lower level in n-type material was performed in a manner similar to the electron emission in p-type material by cooling the samples from 180 K under depletion bias (− 30 V). After zero biasing the sample, a fast capacitance increase was observed, followed by a much slower capacitance decrease. The transients due to the capacitance decrease were singly exponential over more than an order of magnitude at all temperatures studied (120 – 150 K). From an Arrhenius plot of e_p^t/T^2 an activation energy of about 0.29 eV was derived from the hole emission in n-type material in fair agreement with the p-type result and DLTS measurements.

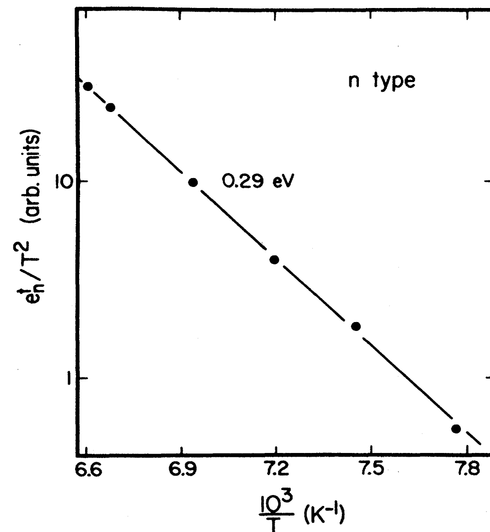

FIG. 11. Arrehenius plot of emission rates of electrons from interface traps in n-type Si.

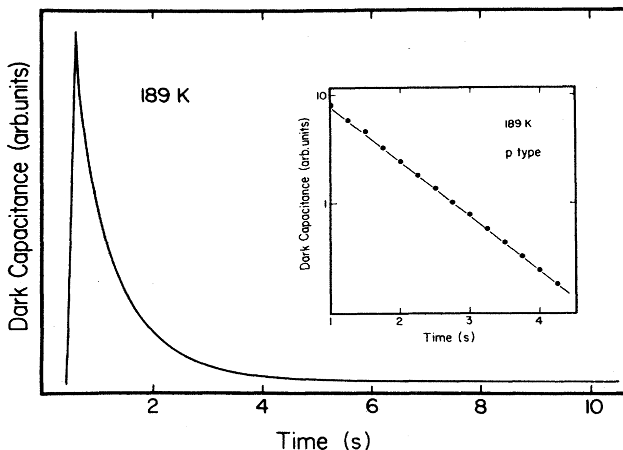

FIG. 10. Single-shot transient capacitance decrease, p-type Si. First depleted at + 5 V, 230 K, then cooled to 189 K, then zero biased.

The thermal emission of holes for the lower level and of electrons for the upper level was also studied in p-type samples by using conventional DLTS. In both cases well-resolved DLTS peaks were observed, as in Fig. 12(a) for hole emission. An Arrhenius plot of the hole emission rates e_p^t/T^2 reveals an activation energy of 0.31 eV [Fig. 12(b)], somewhat smaller than the one obtained from single-shot measurements in p-type samples but in good agreement with the single-shot measurements in n-type samples. For a continuous distribution of interface states one would expect a rather featureless DLTS spectrum with a smoothly varying signal over the entire temperature range.[30] The fact that we obtained very similar activation energies from DLTS and single-shot measurements in both n- and p-type material with very different initial conditions suggests that we probably rather deal with a peak in level distribution than with a distribution in occupancy. Similar studies of the electron emission in p-type samples showed two emission peaks with activation energies of 0.31 and 0.37 eV. The peaks seen for e_p^t were positive, whereas in the case of e_n^t only negative peaks were observed. Since conventional DLTS measurements on MOS capacitors can detect only majority-carrier emission and surface generation through interface states for depletion-bias conditions,[30] it has to be assumed that the negative peaks arise from minority-carrier recombination. These measurements were performed on two different samples, both giving essentially the same results.

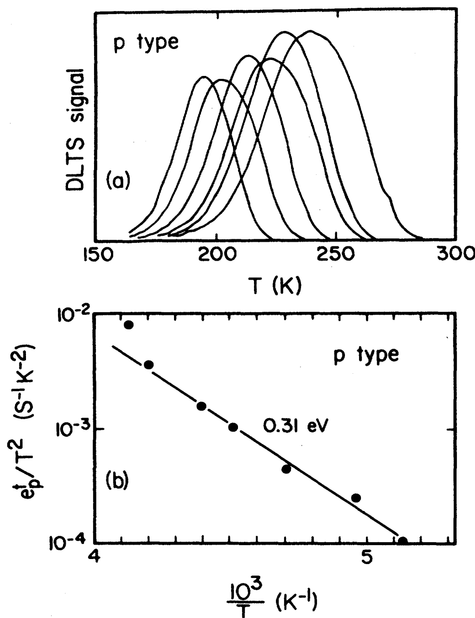

FIG. 12. (a) DLTS observation of thermal hole emission from interface traps in p-Si. (b) Arrhenius plot of e_p^t/T^2.

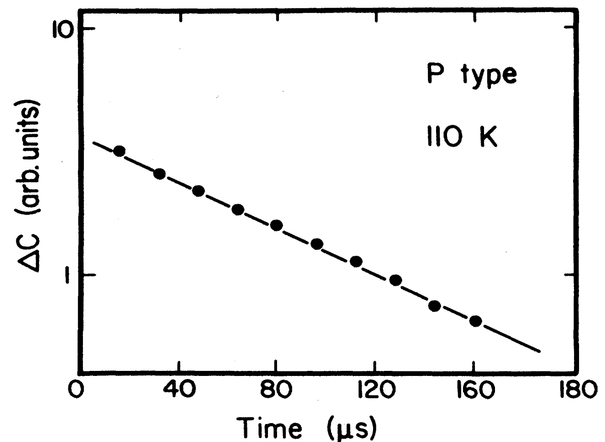

FIG. 13. Hole capture by interface traps in p-type Si at 110 K. Sample was initially depletion biased and illuminated with white light to fill all traps with electrons, then returned to the dark, and repeatedly subjected to 18-μs accumulation-bias pulses. The plot shows a steady exponential decrease in capacitance.

The thermal emission of electrons was similarly studied in n-type samples by DLTS. Well-resolved peaks were observed for all windows used. An Arrhenius plot of the thermal emission rates e_n^t/T^2 obtained in this way gave an activation energy of 0.35 eV, in reasonable agreement with the single-shot measurements.

Hole capture in p-type samples was studied using the pulse-train method.[5] The sample was put into depletion and illuminated with sub-band-gap light prior to the measurement, to make sure that lower levels were filled with electrons. After removing the light source the sample was accumulation biased by an 18 μs pulse, resulting in a small, persistent decrease of the capacitance. The decrease of the capacitance proves that holes and not electrons are captured. Plotting the capacitance semilogarithmically as a function of the number of pulses applied, a single exponential straight line was obtained. Typical data obtained at 110 K are shown in Fig. 13. From these measurements the absolute value of the hole capture cross section is easily calculated[5] if the number of free holes, present during the capture process, is known. The measurement of free carriers at the interface of a MOS structure is not straightforward; in fact, the surface concentration of free carriers decreases with time as interface states are filled during the accumulation pulse.[30] No attempt was made to perform a rigorous determination. Assuming a value of $10^{15}-10^{16}$ cm^{-3} for the free-carrier concentration gives a value of about $10^{-18}-10^{-19}$ cm^2 for the hole capture cross section. These measurements were performed at different temperatures in the range between 87 and 125 K. The measured values varied by about $\pm 25\%$ without showing any temperature trend (Fig. 14). These results are in good agreement with previous measurements, using the energy-resolved DLTS technique on similarly processed MOS capacitors which likewise established that the capture cross section for the characteristic interface states is essentially constant.[31,32] In our further discussion it is therefore assumed that the hole capture cross section is not significantly dependent on temperature and that the activation energy obtained from the different Arrhenius plots of e_p^t/T^2 is an enthalpy ΔH_p. Investigations performed with two different p-type samples resulted in the same enthalpies, but gave slightly different values for the hole emission rate.

Since the cryostat which was available for our measurements only allowed for temperatures down to about 85 K and the thermal emission of electrons is observed at lower temperatures than in the case of holes, the electron capture into the upper level could only be studied qualitatively. These measurements suggested that the electron capture obviously is not very dependent on temperature. It is therefore assumed that, as in the case of holes, the capture cross section of electrons is temperature independent and that the activation energy in the electron emission measurements is close to the enthalpy.

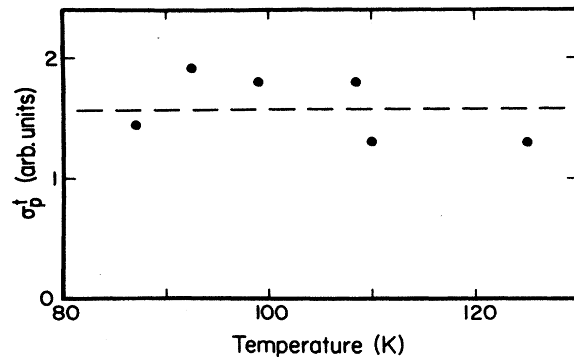

FIG. 14. Temperature dependence of hole capture in p-type Si, derived from several tests as in Fig. 13.

E. Hydrogen annealing

The *G-V* analysis reflects the dominance of interface traps over bulk traps in the samples studied. However, the very high sensitivity of the electrical and optical techniques used makes it desirable to further delimit the possible contributing trap species. In spite of several attempts it was not possible to produce sufficient optical modulation of the ESR signal to correlate directly with the photocapacitance and electrical analysis. This may be due to the low optical cross section of P_b centers. Indirect means were therefore necessary. Hydrogen is known to anneal both interface traps and P_b centers; in fact, the two show quantitatively identical annealing kinetics, with $T_a \approx 220\,^\circ\mathrm{C}$.[33] After many of the measurements were completed, one of the samples was annealed for 20 min in forming gas at 400 °C. The ESR signal (Fig. 15), the stretchout in the *C-V* curve, and the trap ledge in the *C-V* curves were all eliminated. In particular, the sample became almost completely insensitive to light even at 180 K. After about ten days, the electrical manifestation recovered somewhat; but electrical signals remained an order of magnitude weaker than the unannealed values. Interestingly, physical parameters derived from electrical or optical measurements did not change, despite the far fewer traps present.

IV. ANALYSIS AND DISCUSSION

The photon energies and general character of the principal optical photoionization responses at about 0.4 eV are very well correlated with the two peaks in the interface trap spectrum from *C-V* or ESR. The ~0.1 eV difference between the optical hole threshold at about 0.4 eV (Fig. 6) and the lower trap level at 0.3 eV (as observed by *C-V* or ESR) may be interpreted as a configurational change in the trapping center with electron occupancy. This has been calculated for P_b by a molecular-orbital approach to be about 0.1 eV;[34] the experiment and the theory are consistent. A similar but smaller difference for the electrical and ESR energy (0.3 eV) and optical energy (0.35 eV) for the upper level (Fig. 7) presumably indicates the same effect, though theoretical calculation is more complicated for this case and has not been attempted. The occurrence of a second major threshold at about 0.8 eV in the case of electron excitation in *n*-type samples (Fig. 7) is assigned to ionization of the single electron remaining in the amphoteric[12] trap after the first ionization. The position of the lower level via this ionization route is about 0.4 eV above the valence band. For small lattice relaxations the level positions, and associated optical cross sections, are in reasonable accord with theory.[35] Because of the generally good correlation of photoionization features with established properties of the P_b center, and because of the dominance of P_b over other traps in the samples, it seems very reasonable to assign the photocapacitance results to P_b centers.

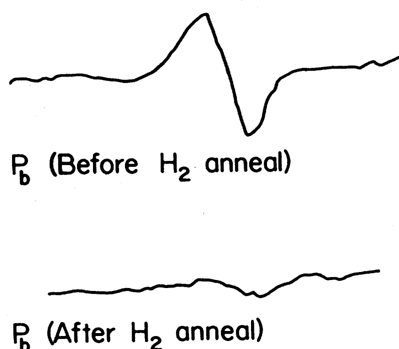

FIG. 15. ESR signal from P_b centers in *p*-type Si before and after anneal in forming gas (10 vol % H_2+90 vol % N_2) for 20 min at 400 °C.

The activation energies for thermal carrier emission correlate closely with the P_b energy-level positions observed by equilibrium techniques at room temperature, viz., *C-V* and gated ESR. For the transition between valence band and the lower level of the interface trap distribution, the single-shot thermal energies in this study average 0.32 eV; previous *C-V* measurements yielded 0.26 eV and ESR, 0.30 eV. For the transition between the upper trap level and the conduction band, our single-shot thermal energies average 0.33 eV while previous *C-V* measurements gave 0.28 eV and ESR, 0.32 eV. Considering that the ESR studies were performed at room temperature whereas the electrical measurements described in this paper were executed at low temperatures, good agreement is obtained between our thermal data and previous ESR results.

Nonetheless, there is a puzzling aspect to the emission results. Two interesting features of the observations are the steep onset of photoionization and the single-exponential character of the capacitance transients observed in various electrical and optical experiments. Single-exponential capacitance transients were only observed for measurements performed within the ledge of the *C-V* curve shown in Fig. 5. These phenomena both suggest trap levels narrower than those seen as peaks in gated ESR and ESR hyperfine linewidth, which indicate P_b center level distribution width for ~100 meV. This discrepancy may indicate that the trap levels are narrower than previously assumed or that the discrepancy is only seeming and can be at least partially explained by experimental factors. Since thermal measurements inherently are caused by collective excitation processes they give little direct information on the energy distribution of energy states. The circumstances are somewhat better for optical excitation processes.

In addition to the experimental factors, the physical nature of the trap system may play a part. The role and behavior of the continuum traps were not separately studied; they may act in series or parallel with P_b centers with uncertain effects on the observed behavior. Another possible factor is the usual randomly distributed oxide fixed charge, providing local electric fields which would broaden D_{IT} peaks observed in gated electrical or EPR methods, but would not necessarily affect photoionization. For all these reasons, the electrically observed parameters, studied previously or in this paper, are not exclusively assigned to P_b centers, although the P_b centers

appear to play a major role.

The hydrogen annealing has another meaning beyond the excellent correlation of signal strengths from ESR and electrical measurements. Silicon dangling orbital centers are the only well-defined defects in Si which anneal in H_2 at 400 °C and below; all the other common bulk traps require 700 °C or higher temperatures.[7,36] This further reduces the likelihood of interference in our observations from the familiar bulk trapping impurities. In addition, the presence of bulk Si-dangling orbital defects (as opposed to interface P_b centers) is ruled out by absence of the characteristic bulk D-center ESR signal, easily differentiated from the P_b signal. Thus on several counts, it is likely that P_b centers dominate many of the effects presented here. Nonetheless, possible contributions from undefined weak-bond states in the U-shaped continuum (which are also H_2-annealable at low temperature) cannot be ruled out.

V. CONCLUDING REMARKS

An important conclusion for this entire investigation is the overall great similarity of behavior of MOS interface traps to the numerous bulk Si traps which have been studied by junction space-charge methods.[4,5] The general character of photocapacitance, single-shot, pulse-train, and DLTS results is much like that observed for many other deep levels in silicon and other semiconductors.

Photocapacitance experiments on interface traps show sharp ionization thresholds at energies 0.05–0.1 eV different from those determined for the two levels of the P_b center by dark capacitance, C-V, and gated ESR. Since in the latter cases the system is in its relaxed state throughout the observations, the displacement of the optical threshold seems very likely to be the Franck-Condon shift associated with a configurational change in the center with different electron occupancy. Thus on the basis of the overall consistency of the picture, the photoionization results are ascribed to the P_b center, which is clearly the dominant trap present. Furthermore, absolute values for the photoionization cross section of electrons and holes of the P_b center are presented for the first time.

Electrical measurements presented here also show aspects which are consistent with assignment to P_b centers, such as the clear emergence of discrete levels and the energies of activation for thermal hole and electron emission. It should be noted that the sign of the dark capacitance transients was consistently in agreement with what one would expect from the various initial conditions and that the enthalpies for the upper and lower level are very similar irrespective of whether they were measured in n-type or p-type samples. However, there is a discrepancy in the observed exponential electrical transients compared with previous findings. Exponential transients would otherwise imply a narrow width for the pertinent trap energy level. It is not clear whether they arise from experimental conditions used or from undemonstrated features of MOS interface traps, such as the participation of band-tail states. Thus we do not make definite assignments of the single-shot emission energies and rates to P_b centers at this time.

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