Influence of thin interfacial silicon oxide layers on the Schottky-barrier behavior of Ti on Si(100)

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(Received 20 May 1988)

The Schottky-barrier height of Ti on both *n*-type and *p*-type Si(100) with thin surface oxide present has been measured in the temperature range 85–355 K with the use of a current-voltage technique. Auger-electron spectroscopy and x-ray photoemission spectroscopy were used to characterize the Si(100) surfaces prior to metal deposition, and to monitor the reaction between Ti and Si upon annealing. The results showed that only a few monolayers of silicon oxide on the initial Si(100) surfaces have a large effect on the barrier height and its temperature dependence, compared with that of silicide formation. The temperature dependence of the barrier height was found to deviate from the predictions of models of the Schottky-barrier formation based on the suggestion of Fermi-level pinning in the center of the semiconductor indirect band gap. However, annealing to sufficiently high temperatures to reduce the interfacial oxide by the Ti resulted in values of barrier heights on both *n*-type and *p*-type Si(100) similar to those on clean Si(100) and in temperature dependence of barrier heights consistent with the predictions of these models. A higher temperature was required to initiate the silicide formation reaction for Ti on Si(100) with few monolayers of surface oxide present. For the reacted silicide phase the temperature dependence of the *n*-type and *p*-type barrier heights was also found to be consistent with the predictions of these models of barrier formation.

I. INTRODUCTION

Understanding Schottky-barrier formation at metal-semiconductor interfaces on a fundamental basis still remains a challenging problem. Both structure and composition of silicide-silicon interfaces can now be varied systematically for understanding phenomena occurring at these interfaces. Experimental results reported for epitaxial $NiSi_2$-Si(111) interfaces have recently pointed to the importance of interfacial structure in the Schottky-barrier formation.[1] However, it has been shown that the electrical characteristics depend critically on the quality of epitaxy of the interface which is strongly affected by the presence of oxygen or silicon oxide on the initial Si(111) surface.[2] This then leads to the basic question concerning the impurity effect on Schottky barrier.

In general, the impurity effect on the barrier height is still unclear. Such an effect could be large since it takes only a small number of band-gap states [$(10^{13}-10^{14})e/\text{eV cm}^2$] to pin the Fermi level at a Si surface, and thus a small amount of impurity (~ 0.1 monolayer) would be sufficient to dominate the barrier height. In an attempt to clarify the role of impurity, the Ti-Si system was chosen for barrier-height measurements on both *n*-type and *p*-type Si(100) using a current-voltage technique at temperatures ranging from 85 to 355 K.

Surface spectroscopy studies of Ti (Refs. 3 and 4) on Si(100) surfaces with several monolayers of silicon oxide present have shown that Ti reacts strongly with the oxygen in the silicon oxide when deposited at room temperature. Furthermore, annealing to 673–773 K has been shown to cause Ti to reach through the thin oxide, producing a silicide similar to that formed with a clean Si(100) surface. The choice of the Ti-Si system then makes it possible to determine the effect of thin interfacial silicon oxide layers on the barrier height and its temperature dependence and also to monitor changes in the barrier height upon annealing to sufficiently high temperatures to reduce the interfacial oxide by the Ti and to initiate silicide formation reaction.

II. EXPERIMENTAL DETAILS

The samples were prepared by depositing (100–1000)-Å Ti films simultaneously on 0.005-Ω cm n^+ and p^+ (100)-oriented Si wafers with 2-μm-thick, 10-Ω cm *n*- and *p*-type epitaxial layers, respectively. The Ti was deposited using dc magnetron sputtering. The details of the sputter-deposition process have been presented previously,[5] and therefore they are omitted here. The Si surfaces were chemically prepared using the RCA clean with and without the final dip in diluted HF, as described by Taubenblatt *et al.*[6] The Si wafers were inserted into the deposition chamber immediately after chemical cleaning, and the deposition chamber was evacuated to $\sim 8\times 10^{-8}$ Torr prior to sputter deposition. During the same deposition, two types of samples were made: bare Si samples for x-ray photoemission spectroscopy (XPS), and thermal SiO_2-covered Si samples with openings for current-voltage (*I-V*) characteristics. For the *I-V* measurements the deposition was made through a metal mask having 2-mm-diam holes but the active area of the diodes was defined by oxide openings with diameters of 25, 100, 225, and 400 μm. The samples were processed together and annealed in the temperature range 673–873 K for interfacial reaction in a continuous flow of helium purified both

over Ti at 1123 K and then over Zr at 923 K.

Auger-electron spectroscopy (AES) was used to determine the effect of Si surface preparation on surface contaminant levels. XPS coupled with Ar^+-ion sputtering at an estimated rate of 1 Å/min was used to monitor the reaction between Ti and Si upon annealing.

Schottky-barrier height (SBH) values for n- and p-type Si(100) were determined by extrapolating the forward I-V characteristics to zero applied voltage. The extrapolation was made by a linear fit over 2 orders of magnitude or greater of current on the semilog I-V characteristics. The slope of the linear portion yielded the value of the ideality factor $n = (q/KT)(dV/d\ \ln I)$, which represents deviation from ideal diode behavior. The I-V measurements were made on all diode areas with the samples held at temperatures in the range 85–355 K. SBH values were also determined from the activation energy analysis[7] of $\ln(J_0/T^2)$ versus $1/T$, where J_0 is the saturation current density at zero applied voltage measured in the temperature range 85–355 K.

III. RESULTS

A. Characterization of Si(100) surfaces

Auger spectra from the Si(100) surfaces are shown in Fig. 1, for the RCA clean with and without the final HF dip. The RCA clean leaves less than a monolayer of oxygen and carbon on the Si surface. If, on the other hand, the HF dip is omitted, a surface with 2–3 monolayers of SiO_2 and less than half a monolayer of carbon is produced. The presence of the thin SiO_2 on the surface prepared by the RCA clean without the HF dip is evidenced by the shift of the Si LVV transition line (from 89 eV for Si to 75.5 eV for SiO_2), and its splitting into two main satellites (at 75.5 and 62 eV), as shown in Fig. 1. Note also the presence of a large substrate component in the LVV spectra, consistent with 2–3 monolayers of SiO_2 on the surface.[6]

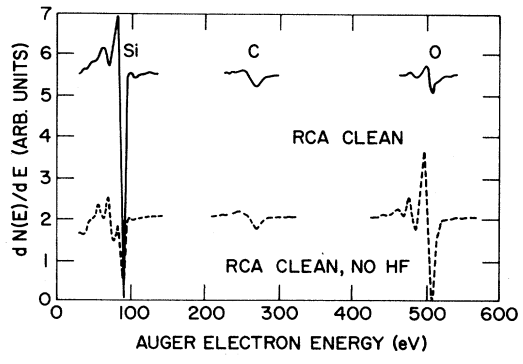

FIG. 1. Auger spectra showing comparison of chemical cleaning procedures. The RCA clean with HF dip leaves less than a monolayer of oxygen and carbon on the Si(100) surface. Omitting the final HF dip from the procedures leaves 2–3 monolayers of silicon oxide and less than half a monolayer of carbon.

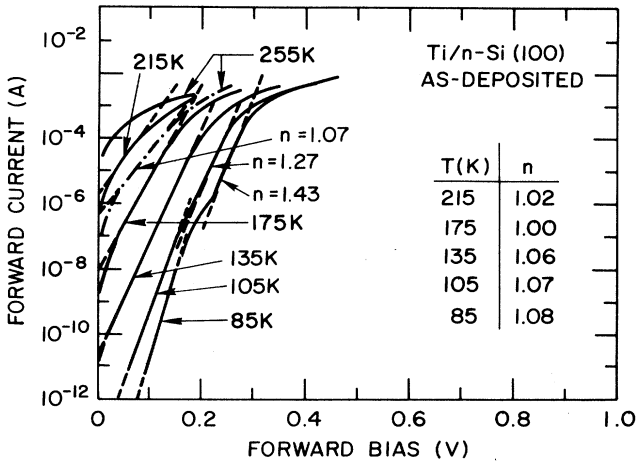

FIG. 2. Forward current-voltage characteristics of Ti on n-type Si(100) as a function of temperature for as-deposited samples prepared using the RCA clean (dashed lines) with and (solid lines) without HF dip. Diode area is 3.974×10^{-4} cm^2.

B. Schottky-barrier heights

1. *n-type Si(100)*

The forward I-V characteristics plotted in Fig. 2 as a function of temperature show examples of the results obtained for as-deposited Ti on n-type Si(100) prepared by the RCA clean without HF dip. Results obtained for n-type samples prepared using the RCA clean with HF dip have been presented in a previous paper[8] and only an example of these results is shown in Fig. 2 for the purpose of comparison. The results clearly show that the current for a given voltage is increased when the samples are prepared using the RCA clean without HF dip, where a thin interfacial oxide is present. Above 215 K, the forward characteristics are highly nonlinear. Below 215 K the samples display a good ideality factor which, however, increases very slowly as the temperature is lowered, reaching a value of 1.08 at 85 K. Moreover, the dependence of $\ln(J_0/T^2)$ on $1/T$ is found to be nonlinear in the range of temperature measured, however, if $\ln(J_0/T^2)$ is plotted against $1/nT$, a straight line is obtained, as shown in Fig. 3, thus showing that J_0 can be described by

$$J_0 = A^* T^2 (-q\phi_{Bn}/nKT) , \quad (1)$$

where A^* is the effective Richardson constant and ϕ_{Bn} is the n-type barrier height. Similar results have also been found by several authors for other Si,[9] GaAs,[10] and InP (Ref. 11) Schottky barriers. It is evident from Fig. 3 that the temperature dependence of the current can be described by two activation energies in the temperature range 85–215 K. Above 115 K, the current is dominated by thermionic emission with an activation energy of 0.37 eV, and below 115 K the current behavior is governed by an activation energy of 0.24 eV. The activation energy of 0.24 eV is evidently associated with recombination current which causes small departures from thermionic emission behavior at low voltages and low temperatures.[7] Attempts have been made to explain the inclusion of the

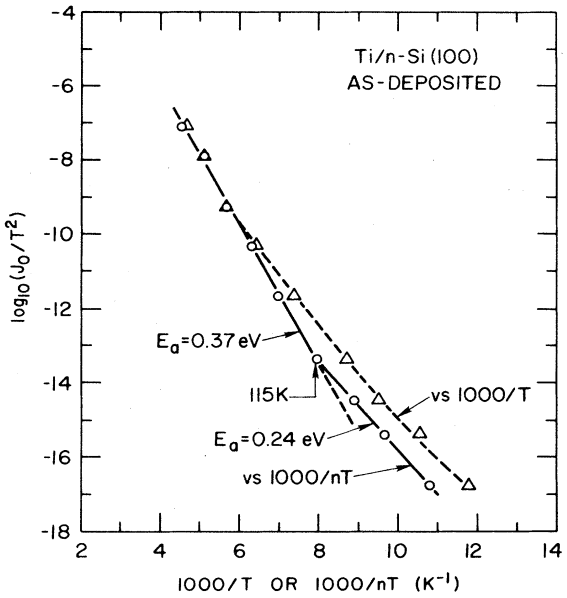

FIG. 3. Temperature dependence of forward current measured at zero applied voltage for n-type samples in the as-deposited state.

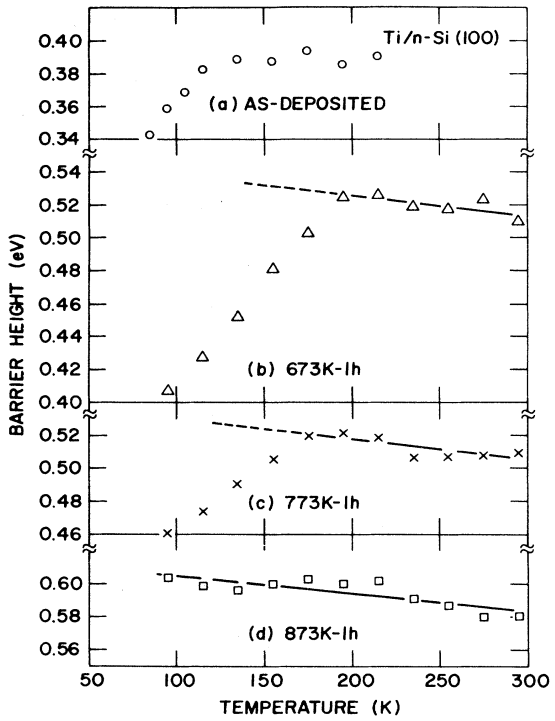

FIG. 4. Change of the barrier height of Ti on n-type Si(100) as a function of temperature for (a) as-deposited samples and samples annealed at (b) 673 K for 1 h, (c) 773 K for 1 h, and (d) 873 K for 1 h. Solid lines: least-squares fit to the experimental data assuming a linear variation for ϕ_{Bn} from 85 to 295 K.

ideality factor in Eq. (1) in terms of a particular distribution of interface states.[12,13] It is to be noted that above 115 K the barrier-height values calculated using Eq. (1) are in good agreement with those reported by Taubenblatt *et al.*[6] for Ti on n-type Si(100) prepared by the RCA clean without HF dip using internal photoemission measurements. It can also be seen from the open circles shown in Fig. 4 that below 115 K the barrier height calculated using Eq. (1) increases with increasing temperature, while above 115 K it remains essentially unchanged with increasing temperature, even though the dominant current mechanism is thermionic emission. Moreover, the forward characteristics displayed in Fig. 2 show that at temperatures lower than 115 K, the ideality factor increases when the voltage exceeds 0.15 V whatever the magnitude of the current and the temperature may be.

The forward I-V characteristics obtained after annealing the samples at 773 K for 1 h are shown in Fig. 5. Results of the annealing at 673 K for 1 h are similar. Above 175 K the samples display a good ideality factor which is independent of temperature. Before 175 K, however, the ideality factor increases with decreasing temperature, reaching a value of 1.24 at 95 K. In addition, a plot of $\ln(J_0/T^2)$ versus $1/T$ is not a straight line, whereas a plot of $\ln(J_0/T^2)$ versus $1/nT$ is a straight line, as shown in Fig. 6. There is, however, a break in the curve at 175 K, showing that above 175 K the current is dominated by thermionic emission with an activation energy of 0.55 eV, and below 175 K the temperature dependence of the current is described by an activation energy of 0.36 eV. This low value of activation is again associated with recombination current which causes deviations from thermionic emission behavior at low temperatures. Thermionic field emission, on the other hand, is highly unlikely, since it would be expected to be significant only at very low temperatures in the lightly doped material used in the present work.[7] In addition, nT is found to be a linear function of temperature.[9,14] It can also be seen from the crosses shown in Fig. 4 that below 175 K the barrier height calculated using Eq. (1) increases with in-

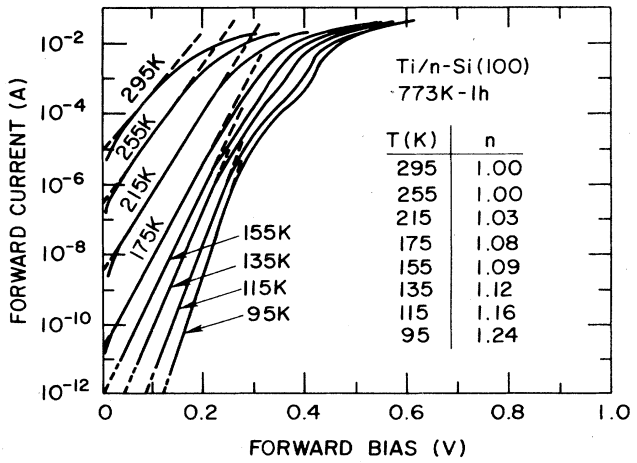

FIG. 5. Forward current-voltage characteristics of Ti on n-type Si(100) as a function of temperature for samples annealed at 773 K for 1 h. Diode area is 3.974×10^{-4} cm^2.

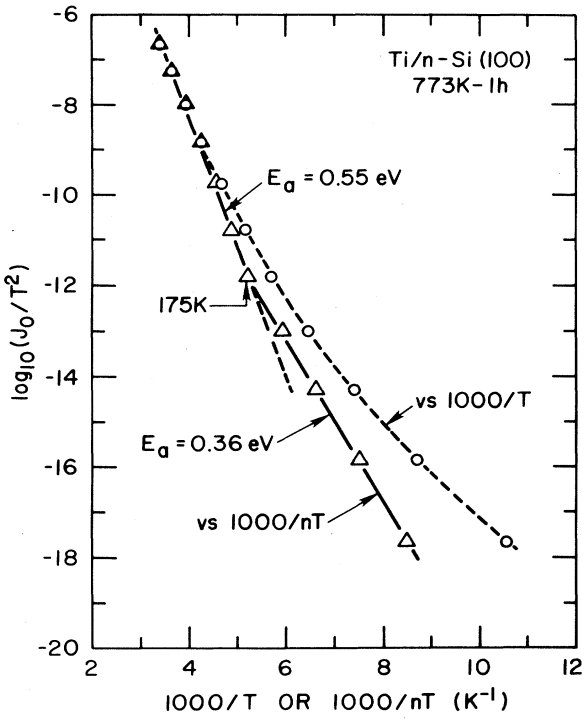

FIG. 6. Temperature dependence of forward current measured at zero applied voltage for n-type samples annealed at 773 K for 1 h.

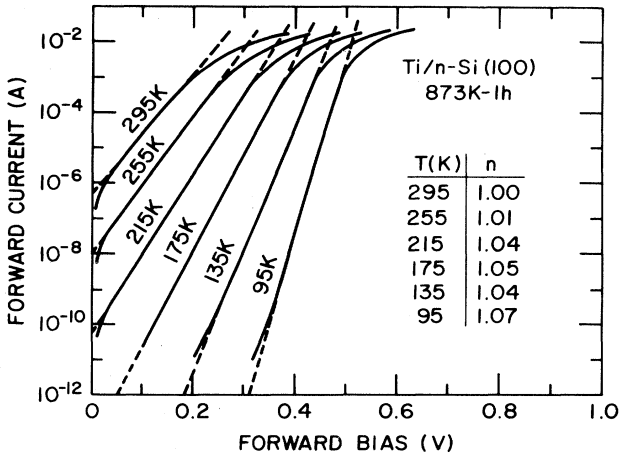

FIG. 7. Forward current-voltage characteristics of Ti on n-type Si(100) as a function of temperature for sample annealed at 873 K for 1 h. Diode area is 3.974×10^{-4} cm^2.

creasing temperature. However, above 175 K, where the thermionic emission current dominates, the barrier height decreases with increasing temperature. The temperature variation of the barrier height calculated using Eq. (1) for the 673-K annealed samples is similar, as shown in Fig. 4 by the open triangles. The forward characteristics displayed in Fig. 5 also show that at temperatures lower than 175 K the current now tends to saturate when the voltage exceeds 0.2 V whatever the magnitude of the current and the temperature may be. Therefore these results are clearly not related to any series resistance effect.

The forward I-V characteristics plotted in Fig. 7 show the results obtained after further increasing the annealing temperature to 873 K. The samples display a good ideality factor which, however, increases very slowly with decreasing temperature, reaching a value of 1.07 at 95 K. Moreover, the dependence of $\ln(J_0/T^2)$ on $1/T$ is again not linear, whereas the dependence of $\ln(J_0/T^2)$ on $1/nT$ is linear in the temperature range 95–295 K with a slope giving the barrier-height value at 0 K, as shown in Fig. 8.

X-ray photoemission-spectroscopy measurements on Ti-Si(100) samples prepared using the RCA clean with HF dip, where less than a monolayer of oxygen is present on the initial Si(100) surfaces, have been presented in a previous paper.[8] The results showed that a silicide phase is formed after a 773-K anneal. For Ti on Si(100) surfaces prepared by the RCA clean without HF dip, the XPS results were similar (and therefore they are omitted here) except that a higher-temperature annealing (873 K) was required to initiate the silicide formation reaction, consistent with the ultraviolet photoemission spectroscopy results of Taubenblatt and Helms.[3] The above results then indicate that after annealing at 873 K for 1 h the extent of silicide formation is sufficient to establish a silicide-Si interface with ideal thermionic emission behav-

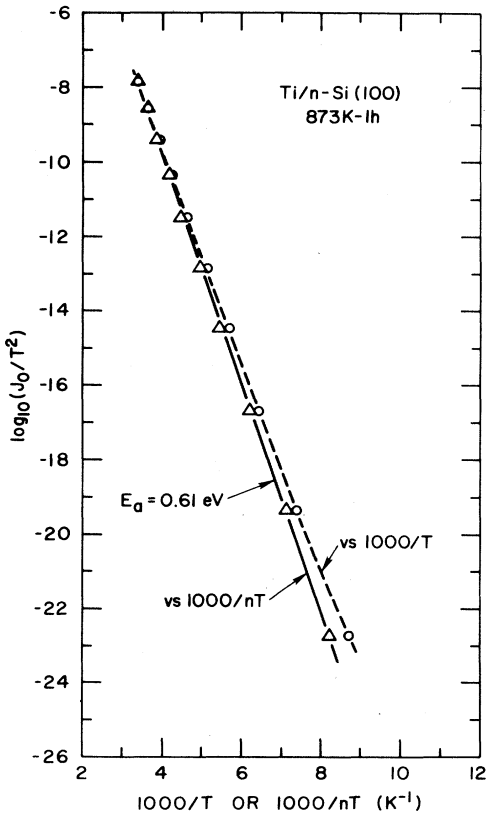

FIG. 8. Temperature dependence of forward current measured at zero applied voltage for n-type samples annealed at 873 K for 1 h.

ior in the temperature range 95–295 K. It is also clear from the open squares shown in Fig. 4 that in these samples the barrier height calculated using Eq. (1) decreases with increasing temperature, consistent with the barrier-height values reported for n-type silicon which showed a negative temperature dependence.[15]

2. *p-type Si(100)*

The forward I-V characteristics plotted in Fig. 9 as a function of temperature show examples of the results obtained for as-deposited Ti on p-type Si(100) prepared by the RCA clean without HF dip. Also shown in Fig. 9 are examples of the results obtained for as-deposited Ti on p-type Si(100) prepared by the RCA clean with HF dip.[8] The results clearly show that the current for a given voltage is reduced when a thin interfacial oxide is present. However, the samples show ideality factors which are very similar to those displayed by p-type samples prepared using the RCA clean with HF dip. The ideality factor is high (1.14 at 295 K), but it remains essentially unchanged in the temperature range 85–345 K. Moreover, in contrast to the n-type samples, the dependence of $\ln(J_0/T^2)$ on $1/T$ is linear in this temperature range as shown in Fig. 10. However, it is evident that two activation energies are governing the current behavior, 0.68 eV at temperatures higher than 175 K and 0.61 eV at temperatures lower than 175 K. These results thus indicate that the current is due to thermionic emission in combination with recombination in the depletion region and that recombination becomes relatively important as the temperature is lowered below 175 K. It can also be seen from the open circles shown in Fig. 11 that above 175 K the barrier height calculated using the relation for thermionic emission remains unchanged with increasing temperature, while below 175 K it increases with increasing temperature. It is to be noted, however, that the barrier-height value (0.69 eV) calculated using the relation for

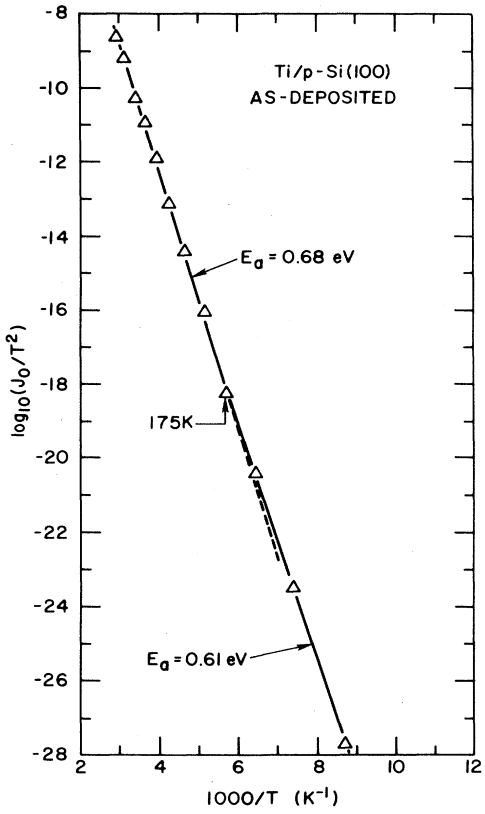

FIG. 10. Temperature dependence of forward current measured at zero applied voltage for p-type samples in the as-deposited state.

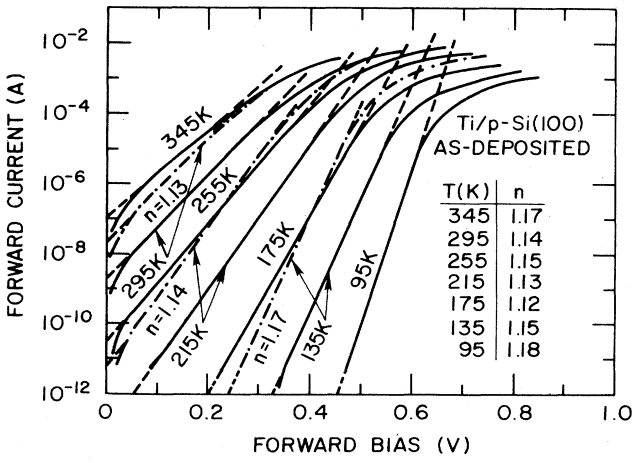

FIG. 9. Forward current-voltage characteristics of Ti on p-type Si(100) as a function of temperature for as-deposited samples prepared using the RCA clean (—·—·—·) with and (——) without HF dip. Diode area is 3.974×10^{-4} cm^2.

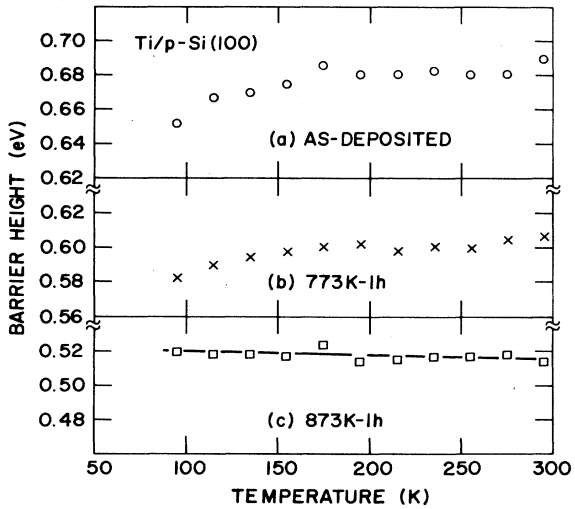

FIG. 11. Change of the barrier height of Ti on p-type Si(100) as a function of temperature for (a) as-deposited samples and samples annealed at (b) 773 K for 1 h, and (c) 873 K for 1 h. Solid line: least-squares fit to the experimental data assuming a linear variation for ϕ_{Bp} from 95 to 295 K.

thermionic emission at 295 K is only slightly lower than the value of 0.72 eV reported by Taubenblatt *et al.*[6] for Ti on *p*-type Si(100) prepared by the RCA clean without HF dip using internal photoemission measurements.

The forward *I-V* characteristics obtained after annealing the samples at 773 K for 1 h are shown in Fig. 12. Results of the annealing at 673 K for 1 h are similar. Again, the samples display a high ideality factor (1.17 at 295 K) which remains essentially unchanged in the temperature range 95–295 K. In addition, the dependence of $\ln(J_0/T^2)$ on $1/T$ is linear in this temperature range with a slope giving an activation energy of 0.58 eV, as shown in Fig. 13. These results indicate that the current is still due to thermionic emission in combination with recombination in the depletion region. The temperature variation of the barrier height calculated using the relation for thermionic emission is also similar to that for the as-deposited samples as shown in Fig. 11 by the crosses. This temperature variation is in obvious disagreement with the reported negative temperature dependence of the barrier height to *p*-type silicon.[15]

The forward *I-V* characteristics plotted in Fig. 14 show the results obtained after further increasing the annealing temperature to 873 K. The samples display a good ideality factor which is independent of temperature. Moreover, the dependence of $\ln(J_0/T^2)$ on $1/T$ is linear in the temperature range of 95–295 K with a slope giving the barrier-height value at 0 K, as shown in Fig. 15. These results indicate that the majority of the current is now due to thermionic emission. It can then be argued that after the annealing at 873 K for 1 h the extent of silicide formation is sufficient to establish a silicide-Si interface with "nearly" ideal thermionic emission behavior. It is also evident from the open squares shown in Fig. 11 that in these samples the barrier height decreases with increasing temperature. Values of the *n*- and *p*-type SBH's (ϕ_{Bn} and ϕ_{Bp}) at 295 K for the as-deposited and annealed samples are summarized in Table I. Also listed are the barrier-height values for samples prepared using the RCA clean with HF dip[8] for purpose of comparison.

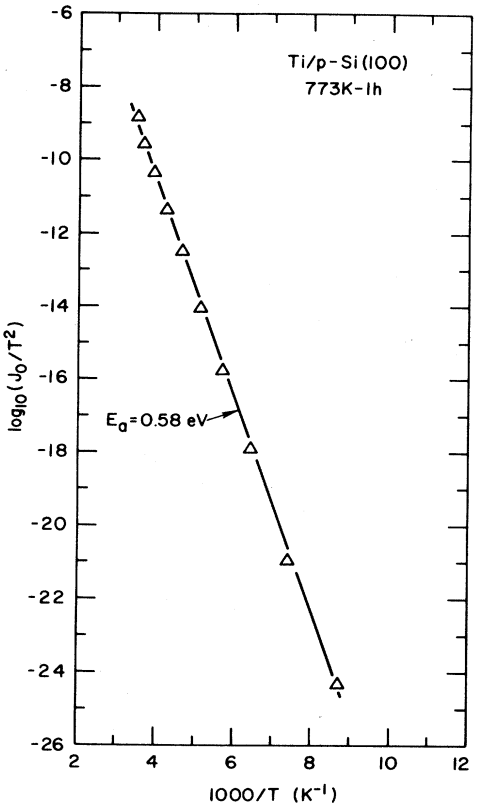

FIG. 13. Temperature dependence of forward current measured at zero applied voltage for *p*-type samples annealed at 773 K for 1 h.

The data of Figs. 4 and 11 show that "only" in the range of temperatures where the thermionic emission current dominates, the *n*- and *p*-type barrier heights decrease with increasing temperature except in the case of the as-deposited *n*-type samples where a thin interfacial

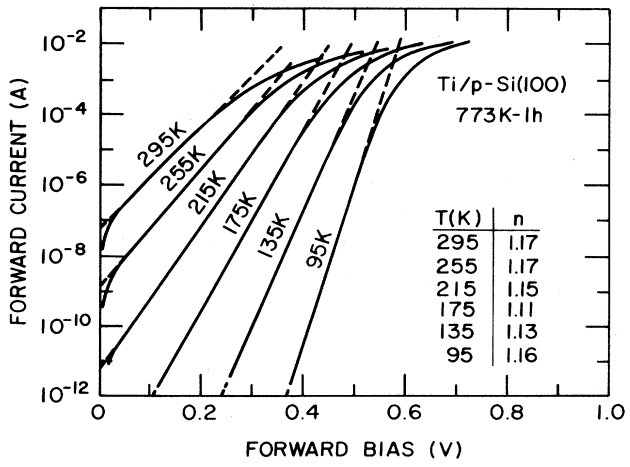

FIG. 12. Forward current-voltage characteristics of Ti on *p*-type Si(100) as a function of temperature for samples annealed at 773 K for 1 h. Diode area is 3.974×10^{-4} cm^2.

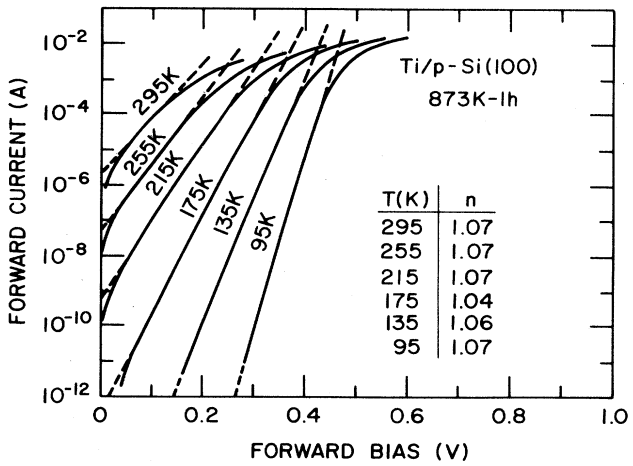

FIG. 14. Forward current-voltage characteristics of Ti on *p*-type Si(100) as a function of temperature for samples annealed at 873 K for 1 h. Diode area is 3.974×10^{-4} cm^2.

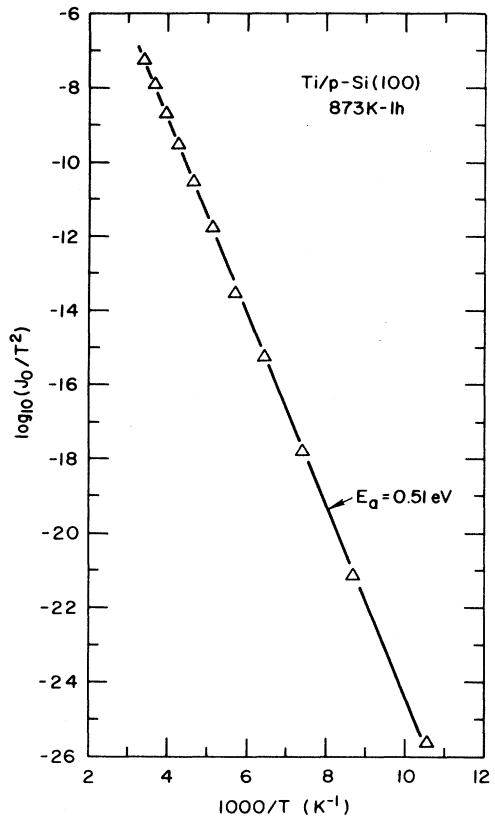

FIG. 15. Temperature dependence of forward current measured at zero applied voltage for p-type samples annealed at 873 K for 1 h.

oxide is present [Fig. 4(a)]. The temperature coefficients of the n- and p-type barrier heights as determined from these data, assuming a linear variation for the SBH's in the temperature range 95–295 K, are listed in Table II.

IV. DISCUSSION

The SBH data in Table I show that for the as-deposited samples prepared using the RCA clean with HF dip, the n- and p-type barrier-height values are similar to those on clean Si(100).[6] This indicates that a small amount (less than a monolayer) of oxygen on the initial Si(100) surface is not sufficient to change the barrier height on the clean Si(100) surface. On the other hand, the data show that only a few (2–3) monolayers of silicon oxide on the initial Si(100) surface are sufficient to cause a decrease (increase) in n-type (p-type) barrier height of about 0.12 eV. However, annealing causes this low (high) barrier height to n-type (p-type) Si(100) to increase (decrease), reaching a value similar to that on clean Si(100) at 673–773 K. It has been shown[3] that such an anneal is sufficient to reduce almost entirely the interfacial oxide by the Ti. With a further increase of the annealing temperature to 873 K, silicide is formed, and the n-type (p-type) barrier height increases (decreases) further by 0.07–0.09 eV, consistent with the results for Ti on Si(100) with less than a monolayer of oxygen present on the initial surface except that a higher temperature is required to initiate the silicide formation reaction, as can be seen in Table I. These results thus indicate that only few monolayers of silicon oxide on the initial Si(100) surface have a large effect on the barrier height, compared with that of silicide formation.

With only a few exceptions,[16,17] theoretical models of Schottky-barrier formation at metal-semiconductor interfaces have been based on the suggestion that the Fermi level is pinned at the interface by states in the semiconductor band gap. The origins of these states have been variously attributed to semiconductor surface states,[18] metal-induced interface states,[19] or any of the variety of defects[20] in the semiconductor. Recently, a simple quantitative relationship between barrier heights and measured bulk semiconductor properties has been proposed based on the suggestion of Fermi-level pinning in the center of the indirect band gap.[21] The p-type barrier height ϕ_{Bp} was given by

$$\phi_{Bp}=\frac{1}{2}\left[E_g^i-\frac{\Delta}{3}\right]+\delta_m \ , \tag{2}$$

where E_g^i is the semiconductor indirect band gap, Δ is the spin-orbit splitting (0.04 eV for Si at room temperature), and δ_m is an adjustable parameter, which allows for some shift in Fermi level from the gap center, depending upon the metal. It has previously been shown[5] that for Ti on Si(100) with less than a monolayer of oxygen present, the value of δ_{Ti} is close to 0 eV; in other words, Fermi-level

TABLE I. Values of SBH's at 295 K for Ti on Si(100).

Annealing condition	Barrier height (eV) RCA clean, HF ϕ_{Bn}	RCA clean, HF ϕ_{Bp}	RCA clean, no HF ϕ_{Bn}	RCA clean, no HF ϕ_{Bp}
None	0.501	0.601[a]	0.386[b]	0.691[c] (0.72[d])
At 673 K for 1 h	0.506	0.600	0.510	
At 773 K for 1 h	0.585	0.547	0.510	0.607[c] (0.62[d])
At 873 K for 1 h	0.596	0.504	0.581	0.514

[a]Reference 5.
[b]Value determined from I-V measurements at 215 K.
[c]In these samples the current is due to thermionic emission in combination with recombination in the depletion region, resulting in somewhat low values of barrier heights.
[d]Values determined from internal photoemission measurements (Ref. 6).

TABLE II. Temperature coefficients of the SBH's (in 10^{-4} eV/K), obtained by straight-line least-squares fits to the experimental data. Temperature coefficient of the indirect energy gap of Si, dE_g^i/dT, is $\sim -2.4\times10^{-4}$ eV/K in the temperature range studied (Ref. 5).

Annealing condition	$d\phi_{Bn}/dT$	$d\phi_{Bp}/dT$
None		
At 673 K for 1 h	−1.23	
At 773 K for 1 h	−1.25	
At 873 K for 1 h	−1.06	−0.15
At 1023 K for 1 h	−1.16	−1.28

pinning occurs near the center of the indirect gap. On the other hand, the data in Table I show that only few monolayers of silicon oxide on the initial Si(100) surface are sufficient to shift the Fermi level well above the gap center. This effect of interfacial oxygen or silicon oxide on the barrier height can be explained as due to a reduction in the density of states in the semiconductor gap which pin the Fermi level, so that they are no longer able to screen the effect of the metal electronegativity. The barrier then behaves more like an ideal Schottky barrier, with metals such as Ti with lower electronegativity than Si having low (high) barriers to n-type (p-type) silicon. Further, in the range of temperatures where the thermionic emission current dominates, the values of barrier height on n-type Si(100) do not show a temperature dependence. This implies that all the change in the Si energy gap is then reflected in the change of the p-type barrier height with temperature. Unfortunately, in the as-deposited p-type samples the current is due to thermionic emission in combination with recombination in the depletion region. As a result, the barrier-height values calculated using the relation for thermionic emission show very little or even a positive temperature dependence since departures from ideal behavior due to recombination become more pronounced as the temperature is lowered. Nevertheless, these results clearly deviate from the predictions of Eq. (2) about the temperature dependence of the barrier height, $d\phi_{Bn}/dT$.

However, with annealing to 673–773 K, the interfacial oxide is reduced by the Ti, the Fermi level shifts to near the gap center, and in the range of temperatures where the thermionic emission current dominates, the n-type barrier height decreases with increasing temperature and with a coefficient approximately equal to one half the temperature coefficient of the indirect energy gap of Si. Furthermore, the results obtained for the silicide phase formed on n-type Si(100) after the 873-K annealing are very similar, as shown in Fig. 4. These results are consistent with the predictions of Eq. (2) regarding the temperature dependence of the barrier height. On the other hand, for the silicide phase formed on p-type Si(100) after the 873-K annealing, the barrier height decreases with increasing temperature but with a coefficient much less than one half the temperature coefficient of the energy gap. It was found, however, that with higher-temperature annealing (1023 K for 1 h), the extent of silicide formation became sufficient to establish a silicide-Si interface with more ideal behavior in the temperature range 85–295 K (the ideality factor had a value of 1.02, independent of temperature). For such an interface the temperature coefficient of the barrier height was found to be approximately equal to one half that of the energy gap (see Table II), consistent with the predictions of Eq. (2) about the temperature coefficient of the p-type barrier height, $d\phi_{Bp}/dT$. The present results thus indicate that the presence of few monolayers of silicon oxide on the initial Si(100) surfaces has also a large effect on the temperature dependence of the barrier height.

In theoretical models of Schottky-barrier formation, Fermi-level pinning has been attributed to states in the gap of the semiconductor which are in equilibrium with the metal. However, many authors[22] have reported on the existence of interface states in equilibrium with the semiconductor, even for ultrahigh-vacuum cleaved Si surfaces. It has been argued[23] that these kinds of states would influence I-V characteristics; the alteration in interface charge and hence in band alignments should lead to an increase in barrier height as forward voltage increases. This effect, in turn, should involve the occurrence of I-V nonidealities, i.e., a voltage-dependent ideality factor. The increase in the ideality factor when the forward voltage exceeds 0.15 V (Fig. 2) can then be interpreted as due to the quasi-Fermi-level moving into a high density of interface states which equilibrate with the semiconductor. With annealing to 673–773 K, the I-V characteristics tend to saturate when the voltage exceeds 0.2 V (Fig. 5); this can be considered as an increase of ϕ_{Bn} from its initial value which is now 0.51 eV at 295 K. It is of interest to mention that several authors[22,24] have reported on the existence of an interface level located 0.35 ± 0.15 eV below the Si conduction-band edge, containing 10^{14} states/cm^2. However, the present results show that further annealing to 873 K causes the disappearance of these I-V nonidealities, suggesting that the states responsible for their occurrence are most likely associated with defects in Si near the interface which can be removed with sufficient silicide formation reaction. These results thus indicate clearly that the barrier height is not determined by such defect levels. Nevertheless, in addition to acting as charge storage centers, they can also act as recombination centers[25] giving rise to excess current which causes deviations from ideal thermionic emission behavior at low voltages and low temperatures as indicated by the low activation energies in Figs. 3 and 6. Furthermore, the present results clarify a role in silicide formation reaction in determining the electrical characteristics of the metal-Si interface. Finally, it is clear that more work on the impurity effect is still required in order to further clarify the picture.

V. CONCLUSION

The Schottky-barrier height of Ti on both n-type and p-type Si(100) with thin surface oxide present has been measured in the temperature range 85–355 K. The results show that only few monolayers of silicon oxide on

the initial Si(100) surfaces have a large effect on the barrier height and its temperature dependence, compared with that of silicide formation. The temperature dependence of the barrier height is found to deviate from the predictions of models of Schottky-barrier formation based on the suggestion of Fermi-level pinning in the center of the semiconductor indirect band gap. However, annealing to sufficiently high temperatures to reduce the interfacial oxide by the Ti results in values of barrier heights on both *n*-type and *p*-type Si(100) similar to those on clean Si(100) and in temperature dependence of barrier heights consistent with the predictions of these models. A higher temperature is required to initiate the silicide formation reaction for Ti on Si(100) with few monolayers of surface oxide present. For the reacted silicide phase the temperature dependence of the *n*-type and *p*-type barrier heights is also found to be consistent with the predictions of these models of barrier formation.

ACKNOWLEDGMENTS

A portion of this work was done while the author was a visiting scientist at the Department of Solid State Electronics, Royal Institute of Technology, Stockholm, Sweden. It is the author's pleasure to acknowledge F. Cardona for AES data, Central Scientific Services Material Laboratory at Yorktown for the Ti deposition, and L. Stolt and C. S. Petersson for helpful discussions.

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