Electrical study of Schottky-barrier heights on atomically clean *p*-type InP(110) surfaces

N. Newman, M. van Schilfgaarde, and W. E. Spicer
Stanford Electronics Labs, Stanford University, Stanford, California 94305
(Received 20 October 1986)

We report here a systematic study of the electrical properties of a large number of metal (Ag, Cr, Cu, Au, Pd, Mn, Al, Ni) on *p*-type InP diodes. Schottky-barrier diodes were fabricated by *in situ* metal deposition on atomically clean InP(110) surfaces in ultrahigh vacuum. Schottky-barrier heights were determined from current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements. A small, but finite, range in barrier heights (0.76—0.98 eV) is found for the metal—*p*-type InP systems investigated. When a comparison is made to our earlier work on *n*-type surfaces, we find that the interface Fermi level of *n*-type and *p*-type samples pins at the same position within the band gap for each of the metal InP systems studied. Our experimental results indicate that models that use metal-independent surface states (energy and density) and potential normalization conditions (i.e., natural band lineups) can predict the general trends in the interface Fermi-level pinning behavior. They cannot, however, successfully predict the details of this behavior to within measurement error. A theoretical method to determine the natural band lineups at the interface (using a scheme developed by Anderson) is presented within this context. Also investigated was the effect of air exposure on the electrical characteristics of diodes. For *in situ I-V* measurements, the metal semiconductor systems were characterized by a near-unity (1.03—1.10) ideality factor *n*. Upon exposure to air, a large increase in the current and ideality factor *n* was found for several (Cu, Au, Pd, Mn, Ni) metal—*p*-type InP systems at all measured biases. A detailed investigation of the Pd—*p*-type InP system indicated that the "excess" current pathway which results from exposure to air is at the periphery and can be eliminated by mesa etching.

I. INTRODUCTION

Despite the extensive number of studies which have characterized the structural, chemical, and electronic nature of the metal-semiconductor junction, the physical mechanism responsible for the formation of the Schottky barrier has not been confidently established. Recently, experimental methods have been developed which allow investigators to study properties of metal-semiconductor systems while the Schottky barrier is actually being formed. In the late 1970's it was demonstrated that for clean cleaved GaAs(110) and InP(110) surfaces, there are no intrinsic surface states within the band gap.[1] This discovery has allowed investigators to study the properties of the system *before* any band bending has occurred (on the freshly cleaved surface), *during* the formation of the Schottky barrier (once submonolayer to several monolayers of metal has been deposited on the surface), and *after* the Schottky barrier has been completely established (for thick metal coverages; typically 1000 Å).[1,2]

While a tremendous number of studies within the last 10 years have investigated clean cleaved GaAs(110) and InP(110) systems for submonolayer to several monolayer coverages of metals, only a small number have investigated the properties of systems prepared on these surfaces for thick metal coverages. We have recently determined barrier heights from electrical device measurements for thick-metal coverages on *n*-type GaAs(110) (Ref. 3) and *n*-type InP(110) (Ref. 4) surfaces. Very good agreement (i.e., within experimental error) is found when these values for thick metal coverages are compared to the Schottky-barrier height of submonolayer to several monolayer metal coverages (as determined by photoemission spectroscopy).[3–5] This data indicates that the Schottky-barrier height is almost entirely established for submonolayer coverage, suggesting that the same mechanism is responsible for pinning the Fermi level for ultrathin and thick-metal coverages on *n*-type surfaces.[5]

To date, no sample preparation technique (e.g., heat cleaning, sputtering, molecular beam epitaxy (MBE), and chemical preparation) except cleaving produces surfaces in which the Fermi level is unpinned (i.e., no band bending). For this reason, it has only been possible to study the properties of metal-semiconductor systems while the Schottky barrier is being formed on the cleavage face [i.e., (110) face]. However, the Schottky-barrier height of metal—*n*-type InP and metal—*n*-type GaAs diodes on clean cleaved (110) surfaces consistently agrees with those formed on heat cleaned (100) and air-exposed chemically prepared surfaces.[3–6] This suggests that the mechanism responsible for pinning the Fermi level on the clean cleaved (110) surface may be important in the more general case of contacts prepared on other crystal faces using other sample preparation techniques.[5]

Because almost all of the barrier height determinations for diodes formed on clean *p*-type GaAs(110) and InP(110) surfaces have been measured at submonolayer to several monolayer coverages, a number of questions have arisen. For example, what is the relationship between the pinning position for thin and thick metal coverages on *p*-type samples? And is there a difference between the pinning position for *n*-type and *p*-type samples? In earlier

compilations based on a limited amount of data, it appeared that the pinning positions of n-type and p-type samples in the thin-film regime were typically separated by approximately 0.25 eV.[2] Recently, more data has been obtained and this separation appears to be unique to metals with intermediate electronegativity (i.e., 1.5—1.7; e.g., Al, Ga, In) on GaAs.[5] In their paper, Zur, McGill, and Smith[7] focused attention on this and showed that when charge exchange between a bulk metal and semiconductor was included, such separation is unlikely for thick metals. Spicer *et al.*[8] later pointed out that this can depend on the assumptions used (location of defects; model of screening near the interface), and that there can be a significant difference in the pinning position for n-type and p-type samples in certain circumstances. This study was initiated to investigate the Fermi level pinning behavior of thick metal Schottky diodes formed on clean cleaved p-type InP(110) surfaces in UHV so that these comparisons can be made.

II. EXPERIMENT

Metal-InP(110) diodes were fabricated by *in situ* deposition on clean p-type InP(110) surfaces prepared by cleavage in UHV (base pressure 2×10^{-10}—6×10^{-10} Torr). The samples[9] used were from the same ingot which was Zn doped to $2\times10^{16}/\text{cm}^{-3}$ as specified by the manufacturer and confirmed by ourselves using the capacitance-voltage (C-V) method.[3] Diodes of ~500 μm in diameter were defined by a stainless-steel shadow mask placed just in front of the samples. Approximately 1000 Å of the metal were deposited. To avoid excessive heating or contamination and to insure that the initial rate of deposition was the same as used in the studies utilizing surface sensitive techniques, the metal deposition was performed in roughly 27 evaporation steps (typically 9 steps each of 1, 10, and 100 Å) with 20—120 s in between. The thickness of metal coverage was determined using a quartz thickness monitor placed in close proximity to the GaAs sample. Average pressures were kept below 10^{-9} Torr during the initial stages of Schottky-barrier formation ($<\sim100$ Å).

After fabricating the diodes, current-voltage (I-V) measurements were performed *in situ* at pressures of $\sim2\times10^{-10}$—6×10^{-10} Torr. After the diodes were removed from the UHV chamber, I-V and C-V measurements were also performed in atmospheric conditions. The electrical measurements were made using a computer controlled system which included a Hewlett-Packard HP4140B picoameter and a Hewlett-Packard HP4277A capacitance meter. Further details of the experimental methods used in fabricating and measuring the diodes can be found in Refs. 3 and 4.

III. RESULTS

Typical I-V data for the diodes measured in UHV are presented in Fig. 1. Note the linear log$I$ versus voltage relationship over almost 4 orders of magnitude for all of the systems studied. The thermionic emission equation can be used to determine the effective I-V barrier height from the current-voltage measurements[10]

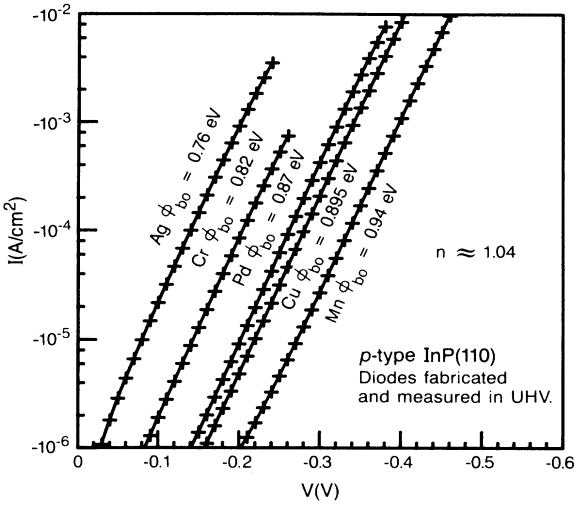

FIG. 1. An assortment of typical I-V data from thick-metal diodes which were fabricated on clean cleaved p-type InP(110) surfaces and measured *in situ*. The barrier height, Φ_b and ideality factor, n are determined from Eq. (1).

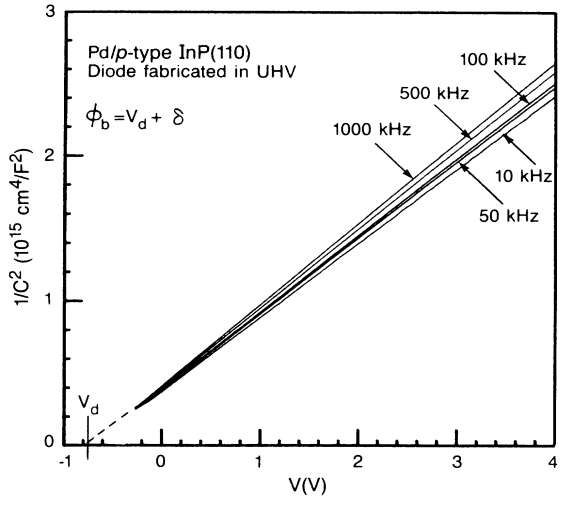

FIG. 2. Typical C-V data encountered in this study are shown. The data pictured here is from a planar Pd—p-type InP diode which was fabricated on a clean cleaved (110) surface. Electrical measurements using the C-V measurement technique were performed in atmospheric conditions at room temperature. The barrier height, Φ_b, is determined by adding the diffusion potential, V_d, to the difference between the Fermi level and the valence band maximum in the bulk δ (0.15 eV). Note that the intercept of the voltage axis is essentially identical for all of the frequencies studied. The change in slope of the curve as a function of measurement frequency can be attributed to traps within the depletion layer (estimated to be on the order of $10^{15}/\text{cm}^{-3}$) which cannot follow the higher measurement frequencies (see Ref. 10).

TABLE I. Metal-semiconductor Schottky barrier diodes fabricated on *p*-type InP.

Metal	Ag	Cr	Cu	Au	Pd	Mn	Al	Ni
			Diodes formed on clean cleaved (110)					
I-V Φ_b[a] (eV) (±0.02)	0.76	0.82	0.90	b	0.87	0.94	0.98	0.93 ±0.03
n, ideality factor[a]	1.04	1.04	1.04		1.03	1.05	1.08	1.10
C-V Φ_b[c] (eV) (±0.05)	0.77	0.74–0.82	0.86	0.86	0.87	0.95	0.97–1.00[d]	0.96
$\Phi_{b\,p\text{-type}}+\Phi_{b\,n\text{-type}}$[e] (eV) (±0.04)	1.35	1.32	1.37	1.30[f] (±0.07)	1.33	1.34	1.355	1.30 (±0.05)
PES Φ_b[g] for ultrathin metal coverages (eV) (±0.1)			0.95	0.85	0.8		1.0	0.9
			Diodes formed on chemically prepared (100)					
I-V Φ_b[h] (eV)	0.79			0.79	0.82		0.89	0.90
C-V Φ_b[h] (eV)	0.86			0.93	0.90		1.12	1.14
Pauling electronegativity[i]	1.9	1.6	1.9	2.4	2.2	1.5	1.5	1.8
Work function[j] (eV)	4.26	4.5	4.65	5.1	5.12	4.1	4.28	5.15
Internal potential[k] (eV)	−2.53	−0.84	−1.97	−2.25	−2.75	−1.62	−0.90	−2.04

[a]Effective barrier heights and ideality factors from the *I-V* data reported in this study as deduced using thermionic emission theory [Eq. (1)].

[b]The *I-V* characteristics of the Au—*p*-type InP could not be accurately modeled using Eq. (1), and therefore an accurate *I-V* barrier height could not be determined for the Au—*p*-type InP system.

[c]Barrier heights as measured in this study using the *C-V* technique. The *C-V* characteristics were measured at several frequencies (10 kHz, 50 kHz, 100 kHz, 500 kHz, 1 MHz) and the barrier height of all the systems were found to be independent of frequency (± 0.01 eV). The *C-V* barrier heights have not been corrected for the Gummel-Scharfetter factor. In order that this data can be compared to other data which includes this correction, 0.025 eV should be subtracted from $\Phi_{b\,C\text{-}V}$ in the above table.

[d]For the Al—*p*-type InP diodes, the C^{-2} vs V characteristics were only found to be linear for the lowest (10 KHz) and highest frequency (1 MHz) measured.

[e]In order that this column can be compared to the band gap of InP (1.35 eV), sum of the *I-V* barrier heights includes a correction for image force lowering of 0.05 eV (*n*-type 0.02 eV; *p*-type 0.03 eV) (Ref. 12). Barrier height determinations for dioded formed on clean cleaved *n*-type InP(110) are from Ref. 4.

[f]Because an accurate *I-V* barrier height determination was not possible, the *C-V* barrier height was used instead.

[g]Barrier heights as determined by photoemission spectroscopy (PES) for submonolayer to several monolayer metal coverages. The source of the data is Ref. 4.

[h]E. Hokelek and C. Y. Robinson, Appl. Phys. Lett. **40**, 427 (1982).

[i]L. Pauling, *The Nature of the Chemical Bond* (Cornell University Press, Ithaca, 1960), p. 93.

[j]H. B. Michaelson, J. Appl. Phys. **48**, 4729 (1977).

[k]Internal potential of metals with respect to the Fermi level. The internal potentials of the GaAs and InP valence band maximum are −1.19 and −2.09 eV, respectively. The source of calculations is given in Refs. 15 and 19.

$$I=I_0(e^{(V-IR)/nV_t})(1-e^{-(V-IR)/V_T}), \quad (1)$$

where $I_0=SA^*T^2e^{-\Phi_{b0}/V_t}$ is the saturation current. A^* is the Richardson constant modified for the effective mass of a hole in InP (48 $A\,K^{-2}cm^{-2}$). Φ_{b0}, S, T, V_t, R, and n are the *I-V* barrier height, area, temperature, thermal voltage (0.0256 eV at 25 C), series resistance, and ideality factor, respectively. The series resistance R is due to bulk and contact resistances. Table I summarizes the results of our data analysis. Note the consistent and near-unity ideality factors for the Schottky diodes.

After the diodes were removed from the chamber, *I-V* and *C-V* measurements were performed in atmospheric conditions. Typical *C-V* data are presented in Fig. 2. The diffusion potential, V_d, of the Schottky diode was determined from the intercept of the C^{-2} versus voltage curve for frequencies of 10 kHz, 50 kHz, 100 kHz, 500 kHz, and 1 MHz. A linear relationship was found between C^{-2} versus voltage for all of the systems measured and a linear least-squares fit was used over the voltage range of 0 to 2 V reverse bias. The barrier height was then inferred by adding the difference between the Fermi level and the valence band maximum in the bulk, δ (0.15 eV for these diodes), to the diffusion potential. Table I summarizes the results of our data analysis.

Upon air exposure, a large increase in the current was found for all measured biases for the Cu, Au, Pd, Mn, and

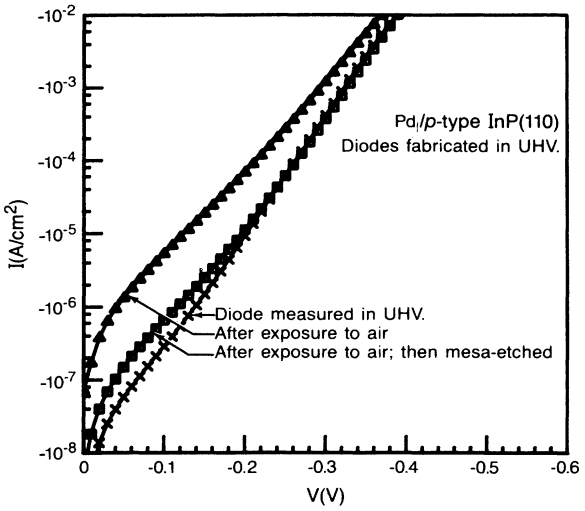

FIG. 3. *I-V* data for the thick-film Pd—*p*-type InP are shown. The electrical characteristics for diodes measured *in situ* in UHV (crosses), for diodes measured *ex situ* after exposure to air (triangles) and for diodes measured *ex situ* after exposure to air, then subsequently mesa-etched (squares). After mesa-etching, almost all of the "excess current" was removed. This clearly demonstrates that the pathway for this "excess current" in the Pd—*p*-type InP diodes is at the periphery.

Ni diodes. To determine the origin of this "excess current," a detailed investigation was performed on the Pd—*p*-type InP system. The diodes were mesa etched using a wet chemical etch (H_2SO_4:H_2O_2:H_2O in a ratio of 2:1:20 for 25 min) to selectively remove the periphery of the device. Figure 3 shows that almost all of the "excess current" was removed by this treatment, demonstrating that the pathway for this "excess current" in the Pd—*p*-type InP diodes lies at the periphery. The removal of "excess current" at the periphery using this chemical treatment has also been found for diodes prepared on *n*-type GaAs substrates.[3] Also note in Fig. 3, the current which occurs at significant forward bias (for biases < -0.2 V), and is associated with the central portion of the device, is essentially identical for the diodes measured *in situ* and after mesa etching. Using the method described in Ref. 3, no significant error in the *C-V* barrier height determinations is expected from leakage current of this magnitude. To experimentally verify this, the *C-V* characteristics of the Pd—*p*-type InP diodes were measured before and after the peripheral leakage current was removed, and the barrier heights for these measurements were found to be consistent.

IV. DISCUSSION

Table I shows that consistent agreement is found between the barrier height of thick-metal diodes formed on clean cleaved *p*-type InP(110) surfaces (as determined in this study), the barrier height of submonolayer to several monolayer metal coverages on clean cleaved *p*-type InP(110) surfaces and the barrier height of thick-metal diodes formed on air-exposed chemically prepared *p*-type InP(100) surfaces. This was also found for diodes formed on *n*-type InP and *n*-type GaAs substrates.[3–6] This is strong evidence that the same mechanism is responsible for pinning the Fermi level for ultrathin and thick-metal coverages for diodes prepared using a wide range of semiconductor surface preparations. This is in agreement with the results and conclusions from the studies on the *n*-type substrates; see Ref. 5 for a more complete discussion.

As can be seen in Table I, a small, but finite, range in barrier heights (0.76 to 0.98 eV) is found for diodes formed on the clean cleaved *p*-type InP surface. As was suggested by Zur, McGill, and Smith,[7] this can be understood by including charge exchange between the metal and semiconductor within the context of the unified-defect model. It is hypothesized in the unified defect model that the barrier height of metal—group III-V semiconductor systems is established by the energy levels of native point defects formed near the surface during metal deposition.[2] For GaAs and InP, the association of an acceptor level approximately 0.25 eV above a donor level for these defects was found to be most consistent with the available experimental data.[5] For metals with large work functions, a large negative charge will be transferred to the metal which will be compensated and pinned by the donor level. Similarly, for metals with small work functions, a large positive charge will be transferred to the metal which will be compensated and pinned by the acceptor level. Most metals lie somewhere between these extremes and the pinning position should fall within this range. Note that this is consistent with the results summarized in Table I; metals with small work functions tend to pin higher in the band gap, while metals with large work functions tend to pin lower in the band gap.

Although the models of Zur, McGill, and Smith[7] and Spicer *et al.*[8] were formulated in the context of the unified defect model,[2] the arguments and conclusions discussed here can be directly applied to any model which incorporates metal-independent surface states. For example, Tersoff proposed that the potential normalization conditions at the interface can be incorporated in the metal-induced gap state (MIGS) model by screening potential differences in the natural band lineups by a fraction (estimated to be $\sim\frac{1}{2}$) of the optical dielectric constant of the semiconductor.[11]

Also note in Table I that the barrier heights of diodes formed on *n*-type and *p*-type samples, when corrected for the image force,[12] sum within experimental error to the band gap of InP (1.35 eV). This indicates that the interface Fermi level pinning position for *n*-type and *p*-type samples are essentially identical for each of the metal-InP systems studied. This shows that the charge exchange between the metal and semiconductor is significantly greater than the charge in the depletion region, as Zur, McGill, and Smith found.

We have seen that the model of Zur, McGill, and Smith can account for several experimentally observed phenomena. Before proceeding we should note that this, or any other model which uses only the bulk metallic properties of the overlayer, cannot account for the range in pinning

positions for systems with ultrathin (submonolayer to several monolayer) metal coverages as summarized in Table I. At these coverages, the bulk metallic properties of the metal have not yet formed. As pointed out by Spicer *et al.*,[8] one can include the charge transfer due to the polarizability of the bonds near the interface to explain the range of pinning positions in the thin-film regime.

We now ask the question, can a model which accurately models the screening and polarizability at the interface completely account for the experimentally measured barrier heights of metal-GaAs and metal-InP systems using the properties of the overlayer as the only independent parameter?

Because work function and electronegativity do not accurately describe absolute energy scales within solids, we cannot expect to use these values to quantitatively predict the charge transfer at the interface.[13] Instead of using these values when modeling charge exchange between the metal and semiconductor, as is conventionally done, it is necessary to develop a more relevant set of parameters. As was suggested by Bardeen,[14] the space-averaged potential in an infinite crystal in 1947 can be used to define an absolute energy scale within solids.[15] By referencing all band calculations with respect to this potential, the "natural" (i.e., Schottky) lineup of metal Fermi levels can be determined within the semiconductor bands. An experimental method to directly measure potential has not been developed.

Recently *ab initio* electronic structure calculations have been able to make accurate predictions of the band structure,[16] lattice constant,[17] cohesive energy,[17] elastic bulk modulus,[17] and work functions.[18] However, the determination of this potential (with respect to the Fermi level in the bulk) generally eludes these calculations because this potential, since it is obtained from integration of the charge density, is undetermined to within an arbitrary constant. Recently, Anderson[15] has suggested a means to obtain a constant analogous to that suggested by Bardeen using linear muffin-tin orbital (LMTO) theory, and there-

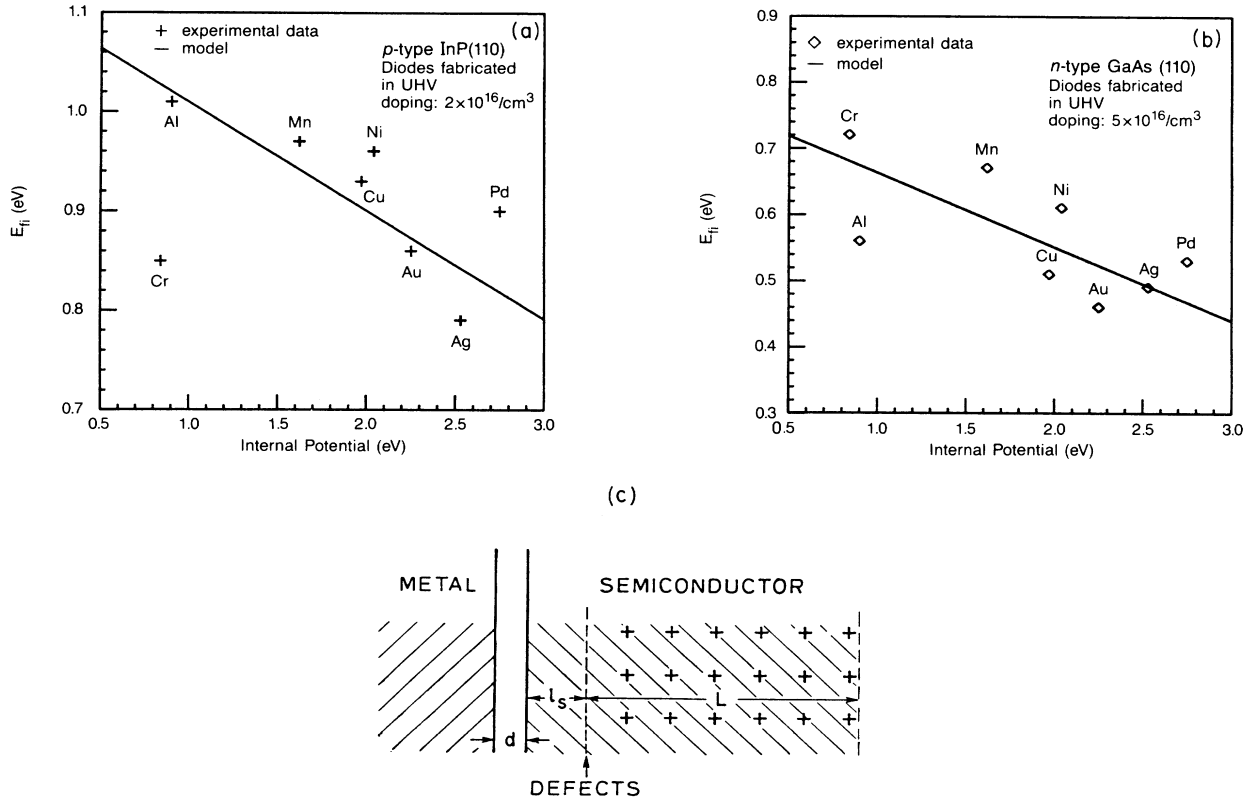

FIG. 4. The interface Fermi-level pinning position, E_{fi}, is plotted vs the internal potential for diodes formed on a InP(110) and (b) GaAs(110) substrates. The interface Fermi level pinning position, E_{fi}, is inferred from I-V electrical characteristics of thick-metal films deposited on clean cleaved substrates. The values for n-type GaAs are from our earlier work (Ref. 12). The internal potential is calculated using a scheme due to Anderson (Refs. 15 and 19). The solid lines in (a) and (b) are included to illustrate the results of the simple electrostatic model, seen in (c), which uses internal potentials to determine potential normalization conditions. Note the monotonic behavior of the solid lines with internal potential. The effective (electronic) spacing between the metal and semiconductor (0.5 Å) is denoted by d. l_S is the distance from the semiconductor surface to the defects. The defects are assumed to be located in a plane 5 Å from the semiconductor surface. L is the width of the depletion layer in the semiconductor.

fore a scheme by which the metal Fermi levels and semiconductor bands can be compared on a common scale. This calculated value will be referred to as the internal potential henceforth. In LMTO theory within the atomic-spheres approximation (ASA), the Wigner-Seitz cell is replaced with a sphere of equal volume. In the ASA, the Hartree potential is equal to the Madelung potential at the atomic sphere radius when the vacuum is defined at zero potential. This reference potential depends only on the ASA and multiple corrections due to nonspherical densities within the spheres. Since standard LMTO programs use this potential as a reference, we use data from existing calculations.[19] The internal potentials with respect to the Fermi level (for metals) and the valence band maximum (for semiconductors) are shown in Table I.

As can be seen in Fig. 4, with the exception of Cr on InP, metals with internal potentials which are large in magnitude tend to pin lower in the band gap, while metals with internal potentials which are small in magnitude tend to pin higher in the bandgap for both GaAs and InP. As discussed earlier, this trend can be understood by including charge exchange between the metal and semiconductor. To illustrate this, we have included the results of a simple electrostatic model which uses internal potentials to determine potential normalization conditions.[20] The model is a self-consistent solution using net charge neutrality and the alignment of Fermi levels. A continuous distribution of localized states (density of 5×10^{14} cm^{-2} per eV) located in a plane 5 Å (l_S) from the semiconductor surface is assumed. The interface Fermi level of the semiconductor is calculated at this plane. A neutral level E_0 (0.7 and 0.35 eV below the conduction-band minimum for GaAs and InP, respectively) is defined at which there is no net charge in the surface states when the interface Fermi level coincides with it. States above and below the neutral level are assumed to be acceptors and donors, respectively. For simplicity, the levels in this model are assumed to be completely filled if the level is below the Fermi level and completely empty if the level is above the Fermi level (i.e., thermal energies with a temperature approaching 0). The effective (electronic) separation between the metal and the semiconductor surface, d was modeled using the Thomas Fermi screening distance of a metal (0.5 Å) because over this distance electronic screening by the conduction electrons of the metal will be ineffective. For this reason, a dielectric constant of 1 (i.e., no polarizability) is expected to be appropriate in this volume; while in all other sections of the semiconductor, including the volume between the defects and the semiconductor surface, the static dielectric constant was used (GaAs, 13.1; InP, 12.4). For simplicity, the shallow levels responsible for doping the semiconductor were assumed to coincide with the conduction-band minimum and the valence-band maximum for n-type and p-type semiconductors, respectively.

Although the important physical parameters for the model (e.g., location and number of localized states, distribution of energy levels, etc.) have not been well established and the model is clearly oversimplified (e.g., oversimplified description of screening and polarization, etc.), it qualitatively can illustrate the results of a model which is based entirely on metal-independent surface states and internal potentials. Note the interface Fermi level position decreases monotonically with internal potential for the solid line in Fig. 4. These models therefore predict that the relative positions between metals will be consistent for diodes formed on different substrates (e.g., Pd should always pin lower in the band gap than Mn, although the magnitude will vary depending on the physical parameters used in the model).

As can be seen in Fig. 4, a model which uses metal-independent surface states and natural band lineups can predict the general trend that metals with internal potentials that are large (small) in magnitude tend to pin lower (higher) in the band gap. It cannot, however, explain several important points. The fact that Cr pins highest within the band gap of all nine metals on GaAs and pins lower in the band gap than all of the metals on InP (except Ag) is clearly inconsistent with a model which is based on internal potentials as the only independent parameter to predict the relative pinning positions of the metal overlayers. We can also not explain why Ag pins lower in the band gap than any other metal on InP by a significant amount ($\sim$0.09 and $\sim$0.06 eV for n-type and p-type, respectively), while on GaAs it does not. We conclude that although these models can successfully predict the general trends, the above observations indicate that details other than considerations due to natural band lineups are also important in determining the pinning positions for metal–group III-V semiconductor Schottky barriers. To date, the other relevant physical parameters have not been isolated, although the number, location, and energy level of defects, the detailed chemical environment, and the detailed electronic structure of the interface are likely candidates.

V. CONCLUSIONS

The barrier-height determinations for the thick-metal devices as reported in this study were found to be essentially identical to the barrier height of submonolayer to several monolayer metal coverages on clean cleaved p-type InP(110) surfaces and the barrier height of thick-metal diodes formed on air-exposed chemically prepared p-type InP(100) surfaces. This is strong evidence that the same mechanism is responsible for pinning the Fermi level for ultrathin and thick-metal coverages for diodes prepared using a wide range of semiconductor surface preparations. When a comparison is made to our earlier work on n-type surfaces, the interface Fermi level pinning position for n-type and p-type samples is found to be essentially identical for each of the metal-InP systems studied. Our experimental results indicate that models that use metal-independent surface states (energy and density) and potential normalization conditions (i.e., natural band lineups) can predict the general trends in the interface Fermi level pinning behavior, but cannot successfully predict the details of this behavior to within measurement error.

ACKNOWLEDGMENTS

The work was supported by the Office of Naval Research and Defense Advanced Research Agency Project under Contract No. N00014-83-0073 and the Air Force Office of Scientific Research under Contract No. AFOSR-86-0263. One of the authors (N.N.) would also like to thank Ted Granger, Mike Robbins, Lance Baldwin, Doug Thomson, and Fred Hanford for helpful discussions on sample preparation techniques.

[1]J. Van Laar and A. Huijser, J. Vac. Sci. Technol. **13**, 769 (1976); W. E. Spicer, I. Lindau, P. E. Gregory, C. M. Garner, P. Pianetta, and P. W. Chye, *ibid.* **13**, 780 (1976).

[2]W. E. Spicer, P. W. Chye, P. R. Skeath, C. Y. Su, and I. Lindau, J. Vac. Sci. Technol. **16**, 1427 (1979); W. E. Spicer, I. Landau, P. R. Skeath, and C. Y. Su, *ibid.* **17**, 1019 (1980); W. E. Spicer, I. Landau, P. R. Skeath, C. Y. Su, and P. W. Chye, Phys. Rev. Lett. **44**, 420 (1980).

[3]N. Newman, M. van Schilfgaarde, T. Kendelwicz, M. D. Williams, and W. E. Spicer, Phys. Rev. B **33**, 1146 (1986), and references therein.

[4]N. Newman, T. Kendelwicz, L Bowman, and W. E. Spicer, Appl. Phys. Lett. **46**, 1176 (1985); T. Kendelwicz, N. Newman, R. S. List, I. Landau, and W. E. Spicer, J. Vac. Sci. Technol. B **3**, 1206 (1985).

[5]N. Newman, W. E. Spicer, T. Kendelewicz, and I. Lindau, J. Vac. Sci. Technol. B **4**, 931 (1986), and references therein.

[6]R. W. Grant, J. R. Waldrop, S. P. Kowalczyk, and E. A. Kraut, J. Vac. Sci. Technol. **19**, 477 (1981); J. R. Waldrop, S. P. Kowalczyk, and R. W. Grant, Appl. Phys. Lett. **42**, 454 (1983); J. R. Waldrop, S. P. Kowalczyk, and R. W. Grant, J. Vac. Sci. Technol. **2**, 445 (1984); J. R. Waldrop, Appl. Phys. Lett. **44**, 1002 (1984).

[7]A. Zur, T. C. McGill, and D. L. Smith, J. Vac. Sci. Technol. B **1**, 608 (1983); A. Zur, T. C. McGill, and D. L. Smith, Phys. Rev. B **28**, 2060 (1983).

[8]W. E. Spicer, S. Pan, D. Mo, N. Newman, P. Mahowald, T. Kendelwicz, and S. Eglash, J. Vac. Sci. Technol. B **2**, 476 (1984).

[9]Prior to diode fabrication, two Ohmic contacts were prepared by ion implantation of Zn at a dose of 5×10^{15} cm^{-2} and an energy of 30 keV onto the back of the sample. The sample was then decreased using the conventional 1,1,1-trichloroethane (TCA)—acetone—methanol—distilled-water rinse for approximately 2 min each. The sample wad subsequently annealed in a hydrogen environment at 490 °C for 25 min, and then at 670 °C for 10 min to activate the implanted carriers. The sample was degreased again. 1-mm indium balls were then pressed on the back of the sample and the sample was subsequently annealed in a hydrogen environment for two min at 190 °C. *I-V* and *C-V* measurements were performed on the two back Ohmic contacts to insure that the contact resistance and contact capacitance would not affect the barrier-height determinations of this study.

[10]E. H. Rhoderick, *Metal-Semiconductor Contacts* (Clarendon, Oxford, 1980).

[11]J. Tersoff, Phys. Rev. B **32**, 6968 (1985).

[12]The *I-V* technique is sensitive to barrier lowering mechanisms such as the image force. If *I-V* barrier-height determinations are used to infer the interface Fermi level pinning position, a correction due to the image force should be added (for the doping referred to here; *n*-type InP, 0.02 eV; *p*-type InP, 0.03 eV; *n*-type GaAs, 0.03—0.04 eV).

[13]Although using electronegativity of work functions gives qualitatively similar results, these parameters cannot quantitively be used to determine absolute energy levels within solids. Work functions include a component due to the surface dipole which can be significantly changed when an interface is formed. Also, the values for electronegativity are defined within the context of atomic bonding and are not a property of a bulk solid.

[14]John Bardeen, Phys. Rev. **71**, 717 (1947).

[15]O. K. Anderson (private communication).

[16]For an example of band-structure calculations and their accuracy, see, Giovanni B. Bachelet and Niels E. Christensen, Phys. Rev. **31**, 879 (1985).

[17]For a brief review of calculations of physical parameters of solids and their accuracy, see M. Schluter and L. J. Sham, Physics Today **35(2)**, 36 (1982).

[18]For examples of work function calculations and their accuracy, see G. W. Fernando, B. R. Cooper, M. V. Ramana, H. Krakauer, and C. Q. Ma, Bull. Am. Phys. Soc. **31**, 482 (1986); Cheng-Quinnn Ma, M. V. Ramana, Bernard R. Cooper, and H. Krakauer Phys. Rev. B **34**, 3854 (1986).

[19]Semiconductor values are from N. Christiensen (private communication). Metal values, with the exception of Al, are from O. K. Andersen, O. Jepsen, and D. Glotzel, *Highlights of Condensed Matter Theory* (Society Italiana di Physica, Bologna, Italy, 1985), p. 116. Al was calculated by ourselves.

[20]Because the use of natural band lineups to predict charge transfer between the metal and semiconductor assumes that there is no change in the atomic charge and potential from the bulk solid at the interface, this scheme is not capable of completely describing the detailed electronic interactions at the interface. The calculation of the internal potential is however a straightforward process which has been performed on a large number of metals and semiconductors (Ref. 19) and this parameter should accurately follow the trends found when compared to more detailed calculations. For more precise quantitative calculations, an energy minimized calculation must be performed to determine the location of atoms and electronic structure self consistently. Due to computer speed and time limitations, this has not been possible for bulk-metal—semiconductor interfaces.