Electrical study of Schottky barriers on atomically clean GaAs(110) surfaces

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We report here a systematic study of the electrical properties of a large number of metal/n-type GaAs (Cr, Mn, Sn, Ni, Al, Pd, Cu, Ag, Au) diodes. Diodes were fabricated on cleaved GaAs(110) surfaces under ultrahigh-vacuum conditions with *in situ* metal deposition. Using current-voltage (I-V) and capacitance-voltage (C-V) measuring techniques, we were able to obtain very reliable and consistent determinations of the barrier height ϕ_b and ideality factor n. All of the metal-semiconductor systems formed on lightly doped ($5\times10^{16}/\mathrm{cm}^3$) n-type GaAs substrates were characterized by near-unity (1.05) ideality factors. A decrease in the effective I-V barrier height, an increase in the ideality factor in forward bias and a strong voltage dependence on the thermionic emission currents in reverse bias were found for diodes formed on the more heavily doped samples. These changes are essentially metal independent, but depend strongly on the doping of the substrate. The characterization (and elimination in some cases) of peripheral leakage currents from the thermionic emission current is found to be essential in obtaining consistent results in our work and in reinterpreting some of the prior work in the literature. The dominant leakage current flows through a small area, low barrier at the periphery of the device and can be eliminated by mesa etching. The consistent and reproducible barrier-height determinations reported in this study, when combined with the results of recent surface-sensitive studies, are a particularly critical test of models of Schottky-barrier formation. The barrier heights measured from the electrical characteristics of thick-metal-film diodes were found to be essentially identical to those reported during the initial stages (submonolayer to several monolayers of metal) of Schottky-barrier formation by photoemission spectroscopy. This agreement indicates that the physical mechanism responsible for Fermi-level pinning in the thick-metal Schottky diodes is first established at submonolayer to several-monolayer coverages of adatoms and an atomic scale model is therefore necessary to account for the available experimental data. No strong correlation between the barrier heights and the work function of the metal or chemistry at the interface was found. Also, diodes formed on clean GaAs(110) surfaces were found to have essentially identical barrier heights to those formed on clean GaAs(100) surfaces and on contaminated (i.e., chemically prepared) GaAs(100) and GaAs(110) surfaces. Several currently popular models concerned with the physical mechanism responsible for the formation of the Schottky barrier are discussed, and the unified defect model is found to be most consistent with the experimental data.

I. INTRODUCTION

Within the last 20 years, surface-sensitive studies using techniques such as photoemission spectroscopy (PES), Auger electron spectroscopy (AES), and low-energy electron diffraction have made a very significant contribution toward understanding and characterization of the chemical, structural, and electronic properties of the intimate metal-semiconductor interface during the initial stages of Schottky-barrier formation (sub to several monolayer coverages of the metal). Despite extensive effort by the surface-science community to eliminate any unnecessary variables by preparing the metal-semiconductor systems in a nearly contamination-free ultrahigh-vacuum (UHV) environment, very few complementary investigations on the electrical characteristics of clean metal-semiconductor systems using similar sample preparation methods have been performed.[1-3] In fact, almost all of the electrical studies that have been reported stem from interest by industry in chemically prepared, air-exposed, and otherwise contaminated interfaces. Because submonolayer coverages of impurities are capable of pinning the Fermi level[4] and altering the chemistry at the interface,[5,6] comparing the results from the fundamental studies on atomically clean interfaces to the results of the electrical measurements on contaminated interfaces is of questionable validity, particularly when the nature of the contaminants is not well known. Furthermore, a thin impurity layer between the metal and semiconductor may have a significant effect on the current transport mechanisms in electrical device measurements.[7] Our main goal in this work was to compare results of spectroscopic and electrical studies on samples grown under similar conditions.

To remove any unnecessary variables and to simplify the chemistry at the interface, diodes in this study were produced on clean GaAs(110) surfaces formed by cleaving under UHV conditions with *in situ* metal deposition. Cleaving has proven to be the best method of preparing stoichiometric and clean surfaces for the group-III-V compound semiconductors.[8] Slow, controlled evaporation

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rates, similar to those used by our group in photoemission experiments, were used during the initial stages of Schottky-barrier formation. As will be seen, these experimental procedures produce very clean and reproducible intimate metal-semiconductor interfaces. The electrical characteristics of the devices grown under these carefully controlled conditions were found to be extremely reproducible and consistent. Also, by comparing the electrical characteristics of diodes made with different metals and substrate doping levels, several universal features were found. For example, at a given doping level of the semiconductor substrate, the current-voltage (I-V) characteristics of all nine metals had essentially the same ideality factor, independent of the metal used. Also, the dependence of the barrier heights on the substrate doping level was essentially the same for each of the metals. Such consistency in the data allows us to report much more reliable barrier-height determinations than has been previously possible.[9] This allows us to gain new insight into the physical mechanisms involved in the formation of the Schottky barrier.

Because these diodes were produced under the same conditions and evaporation rates during the initial stages of Schottky-barrier formation as in the surface-science studies, we can confidently compare the results of measuring techniques which are macroscopic in nature (device electrical measurements) with the results of techniques which are microscopic in nature (for example, PES and LEED measurements). For a review of the advances by the surface-science community, see Refs. 10–13. The results of this electrical data when combined with the results of the surface-sensitive studies are a particularly critical test of different models of Schottky-barrier formation. It is also valuable to compare the studies of intimate Schottky diodes on GaAs and other group-III-V semiconductor systems produced with similar fabrication procedures to previous studies which use different crystal faces and different surface preparations.

II. THE EXPERIMENT

Metal/GaAs(110) diodes were fabricated by *in situ* deposition of Ni, Al, Sn, Mn, Pd, Cu, Au, Cr, and Ag on clean n-type GaAs(110) surfaces prepared by cleavage in UHV. The samples used were n-type GaAs crystals doped to 1×10^{17}, 7×10^{17}, and $9\times10^{17}/\text{cm}^3$ according to manufacturers' specifications; 5×10^{16}, 2×10^{17}, and $9\times10^{17}/\text{cm}^3$ as measured by ourselves using the capacitance-voltage (C-V) method. The doping concentrations quoted henceforth will be those determined by the C-V method.

Prior to diode fabrication, two Ohmic contacts were prepared by annealing indium contacts on the back of each sample. The sample was first degreased using the conventional 1,1,1 trichloroethane (TCE)—acetone-methanol—distilled H_2O rinse for approximately 2 min each. The sample was then etched in a 15:3:1 H_2O:NH_4OH:H_2O_2 solution for typically 5 min followed by a distilled water rinse. 1-mm indium balls were pressed onto the back of the sample. The sample was subsequently annealed in a H_2 environment for typically 10 min at 450 °C. I-V measurements were performed on the two back Ohmic contacts to insure nonrectifying behavior with low-contact resistances (typically $<2\ \Omega$).

After the Ohmic contacts were made, the crystals were loaded in a bakeable UHV chamber [base pressures of $(2-8)\times10^{-10}$ Torr]. The samples were cleaved in UHV to expose a 5 mm×5mm GaAs(110) face. The cleaving procedure consisted of using a soft (annealed) copper anvil to support the crystal while a tungsten-carbide blade on a linear feedthrough applied increasing pressure until the sample was cleaved. Flat surfaces with only a few small cleavage steps on the crystal face were consistently obtained. Metals were evaporated using resistance-type evaporators placed approximately 5 cm from the GaAs sample. The evaporation bead consisted of a small piece of the metal in a tungsten basket (Cr, Mn, Al) or a molybdenum basket (Ag, Sn), a small piece of the metal crimped on a molybdenum wire (Au, Cu), or a thin metal wire wrapped around a helical tungsten wire (Pd, Ni). These beads were identical to those used in the photoemission experiments performed by our group at Stanford, and after adequate outgassing, have proven to consistently evaporate very clean metal overlayers, free of contamination as monitored by photoemission spectroscopy. The diodes, roughly 0.5 mm in diameter, were defined by a stainless-steel shadow mask placed just in front of the sample. Approximately 1000 Å of the metal were deposited. To avoid excessive heating or contamination, the evaporations were performed in roughly 30 steps with 30 to 120 sec in between. We used several submonolayer evaporations, followed by roughly nine evaporations each of 1, 10, and 100 Å. Each evaporation step would last approximately 20 to 120 sec. The thickness of metal coverage was determined using a quartz thickness monitor placed in close proximity to the GaAs sample. Average pressures were kept below 10^{-9} Torr for the initial stages of Schottky-barrier formation (<100 Å).

After fabricating the diodes, I-V and C-V measurements were subsequently performed in atmospheric conditions. For the measurements, gentle contact with the diodes was made using a 10-mm gold ball formed on the end of a 5-mm gold wire. The I-V measurements were performed using the IMPACT system developed at Stanford.[14]

C-V measurements were performed using a Hewlett-Packard 1-MHz 4271B C-V meter and a Hewlett-Packard 6131C voltage source controlled by a Hewlett-Packard 9845B computer. An excellent description of the C-V measurement technique can be found in Ref. 15. The procedures outlined there served as an excellent guide for the C-V barrier-height determinations.

Prior to the C-V measurement, significant forward bias (typically 0.5 eV) was applied to the diodes to empty the electron traps within the depletion layer.[15] C-V measurements were then performed over a voltage ranging between large reverse bias (-4 V) and significant forward bias (0.5 eV). Parasitic circuit capacitance in series with the device under test were measured prior to making electrical contact to the device, and was subsequently subtracted from the measured capacitance to infer the diode capacitance. Caution must be used since this diode capa-

citance may not be an accurate measure of the capacitance of the junction due to the effects of series-resistance elements and the conductance of the junction[15] (and the leakage current pathway, if present). We will discuss two methods which can be used to evaluate the errors introduced by these components. The first method, described in Ref. 15, requires an independent determination of the series resistance r at a large forward bias. However, because changes in contact resistance can result during the measurement, an alternative technique is desirable. Another method is presented here that obviates the need for an independent series-resistance measurement and can be evaluated using only the parameters determined by the conventional capacitance meters during the C-V measurement.

The Schottky diode is typically modeled as a series resistance r (the sum of bulk and contact resistances) in series with a voltage-dependent junction capacitance C and a voltage-dependent junction conductance G [the barrier,[15] (see Fig. 1(a)]. However, conventional capacitance meters are only capable of measuring two parameters, a capacitance C_p and a conductance G_p [see Fig. 1(b)]. A criterion for accurate determinations of the junction capacitance C as measured by this type of equipment was described by Goodman. He showed that an accurate capacitance measurement (and therefore an accurate inference of the barrier height) can be obtained if $(rG+1)^2+\omega^2r^2C^2$ is very close to 1 (a 1% error in the barrier height for a value of 1.005), where ω is the angular measurement frequency.

A simple method which obviates the need for an independent series-resistance measurement can be evaluated using only the two parameters C_p and G_p. The uncertainty in the junction capacitance C can be bounded by evaluating C_p and C_s as shown in Figs. 1(b) and 1(c), respectively. The following equations show C_s is an upper bound and C_p is a lower bound for the junction capacitance C:

$$C_p=C[(rG+1)^2+\omega^2r^2C^2]^{-1}\ , \tag{1}$$

$$C_s=C(1+G^2/\omega^2C^2)\ . \tag{2}$$

Because $r>0$ and $G>0$,

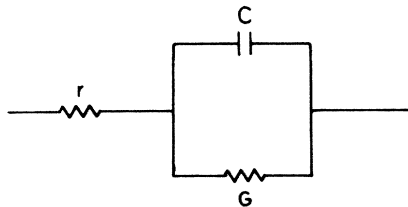
$$C_s>C>C_p\ . \tag{3}$$

C_s and C_p are related by

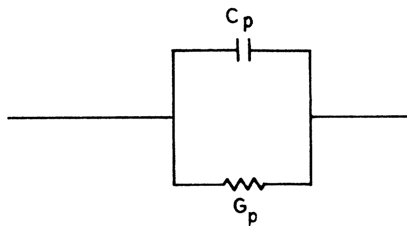
$$C_s=C_p(1+G_p^2/\omega^2C_p^2)\ . \tag{4}$$

The maximum error in the determination of the capacitance using the conventional C-V meters in terms of the parameters C_s and G_p is $C_p(G_p^2/\omega^2C_p^2)$. Therefore, the relative uncertainty in the junction capacitance is $\pm\frac{1}{2}G_p^2/\omega^2C_p^2$. The criterion $G_p^2/\omega^2C_p^2 \ll 1$ was found to be extremely valuable in distinguishing unreliable measurements due to excessively large reverse-bias currents (i.e., large conductance G, such that rG is not $\ll 1$), as well as a poor contact between the gold probe and metal of the Schottky diode (i.e., large series resistance r, so $\omega^2r^2C^2$ is not $\ll 1$). For diodes with a relatively large effective I-V barrier height (>0.5 eV) (as were encountered in this study for diodes fabricated on substrates with doping levels of 5×10^{16} and $2\times10^{17}/\mathrm{cm}^3$) and without large leakage currents, the errors in the C-V barrier-height determination due to the parallel conductance elements and the series-resistance elements were found to be insignificant. However, if electrical contact to the diode was poor or if the diode had a large parallel conductance caused by a small effective barrier [<0.5 eV, as are encountered in diodes formed on heavily doped n-type GaAs substrates and in the n-type InP (Ref. 16) and p-type GaAs systems] or large leakage currents, the errors encountered were found to be significant and an accurate C-V barrier height could not be determined. This may explain the inconsistent reports in the literature of C-V barrier-height values for low-barrier-height systems. Using the I-V and C-V technique a number of diodes, typically eight on each crystal, were measured.

(a) CIRCUIT MODEL OF SCHOTTKY DIODE



(b) PARALLEL CIRCUIT



(c) SERIES CIRCUIT

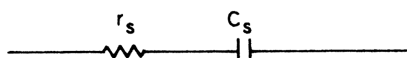


FIG. 1. Panel (a) represents the circuit model of a Schottky diode. The circuit consists of a series resistance r (the sum of the bulk and contact resistances) in series with a voltage-dependent junction capacitance C and a voltage-dependent junction conductance G (the barrier). Panel (b) shows a parallel equivalent circuit which a conventional capacitance meter is capable of measuring. Panel (c) shows a series equivalent circuit. As is shown in the text, the junction capacitance C is bound by the values C_p and C_s.

III. RESULTS

A. Thermionic emission current

Typical forward-bias data from the I-V measurements for all nine metals on the lightest doped substrates can be seen in Fig. 2. Note the linear log$I$ versus voltage relationship over almost 4 orders of magnitude of current for all of the systems studied. The results of forward- and reverse-bias measurements for the Cr/n-type GaAs diodes fabricated on substrates with several doping levels are presented in Fig. 3(a). The current was found to have an exponential dependence on the applied voltage. The thermionic emission equation can be used to determine the effective I-V barrier height from the current-voltage measurements.[1,17] Therefore we obtain

$$I = SA^{*}T^{2}e^{-\phi_b/V_t}(e^{(V-IR)/V_t}-1)\ , \quad (5)$$

where A^{*} is the Richardson constant which is modified for the effective mass of an electron in GaAs. A value of 8.1 $A/K^2\,cm^2$ was used. S, T, ϕ_b and V_t are the area, temperature, effective barrier height, and thermal voltage (0.0252 V at 293 K), respectively. The series resistance R is due to bulk and contact resistances.[1]

Typical forward- and reverse-bias data over a larger voltage range can be seen in Figs. 4(a) and 4(b), respective-

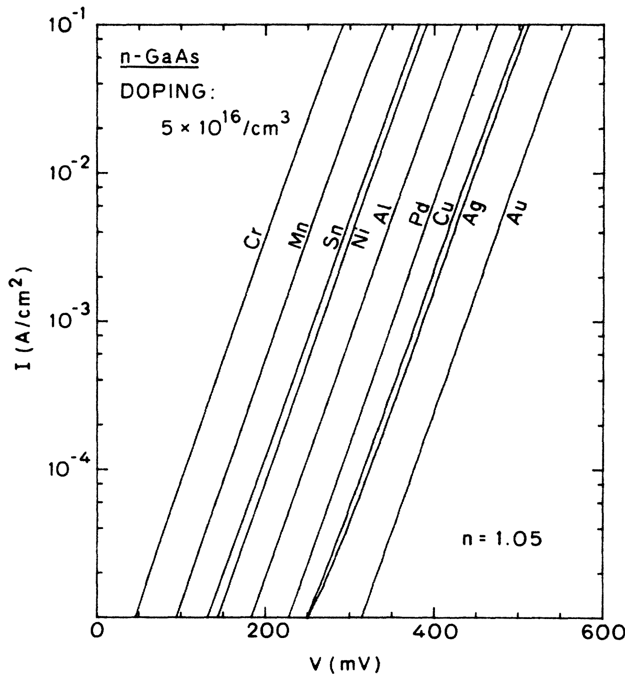
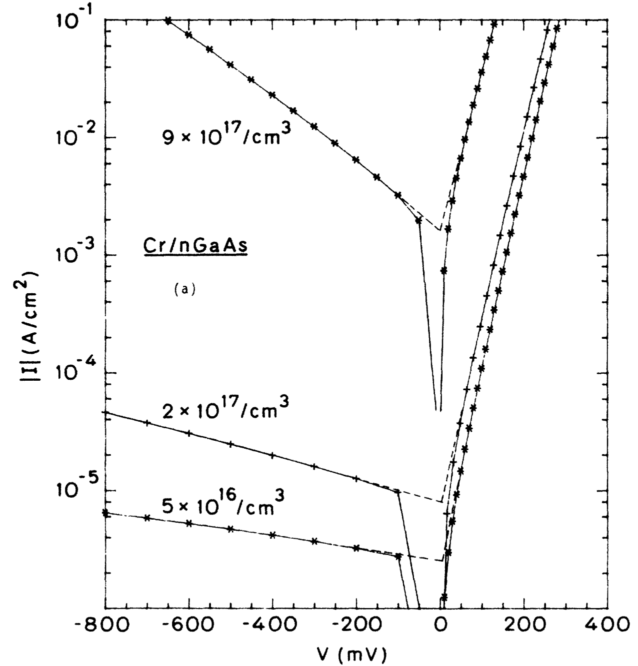


FIG. 2. Typical I-V data from a number of metal:n-type GaAs diodes which were fabricated on a clean cleaved GaAs(110) surface under UHV conditions. The exponential dependence of the voltage can be seen. A near-unity ideality factor (1.05) was found for all nine metals on the lightest doped substrate (doping: $5\times10^{16}/cm^3$). Note the linear log-I-versus-voltage relationship over almost 4 orders of magnitude of current for all of the systems studied. For current densities less than 5×10^{-5} A/cm^2, the effect of leakage currents can be seen in the electrical measurement of the Ag diode.



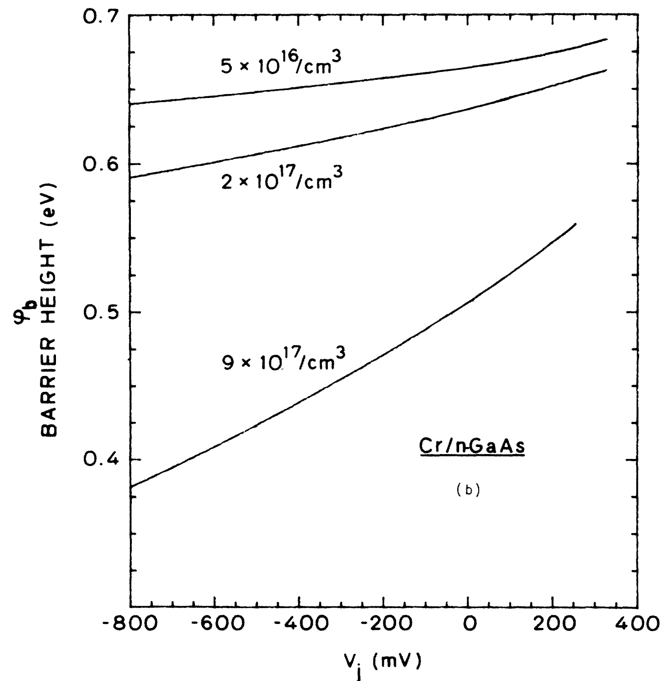


FIG. 3. (a) Typical I-V data from Cr/n-type GaAs systems using several dopings. The exponential dependence of the voltage in the forward direction can be seen. Also, note the significantly greater saturation current value I_0 (and therefore smaller effective I-V barrier height), the decrease in the slope of the forward-bias current (and therefore larger ideality factor), and the much greater voltage dependence on the current in reverse bias for the more heavily doped substrates. (b) Determination of the voltage-dependent barrier height (ϕ_b) using the ideal thermionic emission equation, Eq. (5), as a function of the voltage across the junction ($V_j = V - IR$).

ly. Because the I-V measurement technique is sensitive to barrier-lowering effects,[1–17] the effective I-V barrier height is dependent on the applied voltage and the doping of the substrate. The barrier-lowering mechanisms include the effects of the image force,[1] the effects of tunneling current through the potential barrier,[18] and an alteration of the charge distribution near the interface due to metal-induced gap states (MIGS) (Refs. 19–21) and/or the spatial distribution of charged defects.[4,22] The voltage dependence of the effective I-V barrier height as calculated using Eq. (5) for Schottky diodes fabricated on substrates with several doping levels is plotted in Figs. 3(b) and 4(c). As can be seen, the more heavily doped samples show a much stronger dependence on the effective barrier

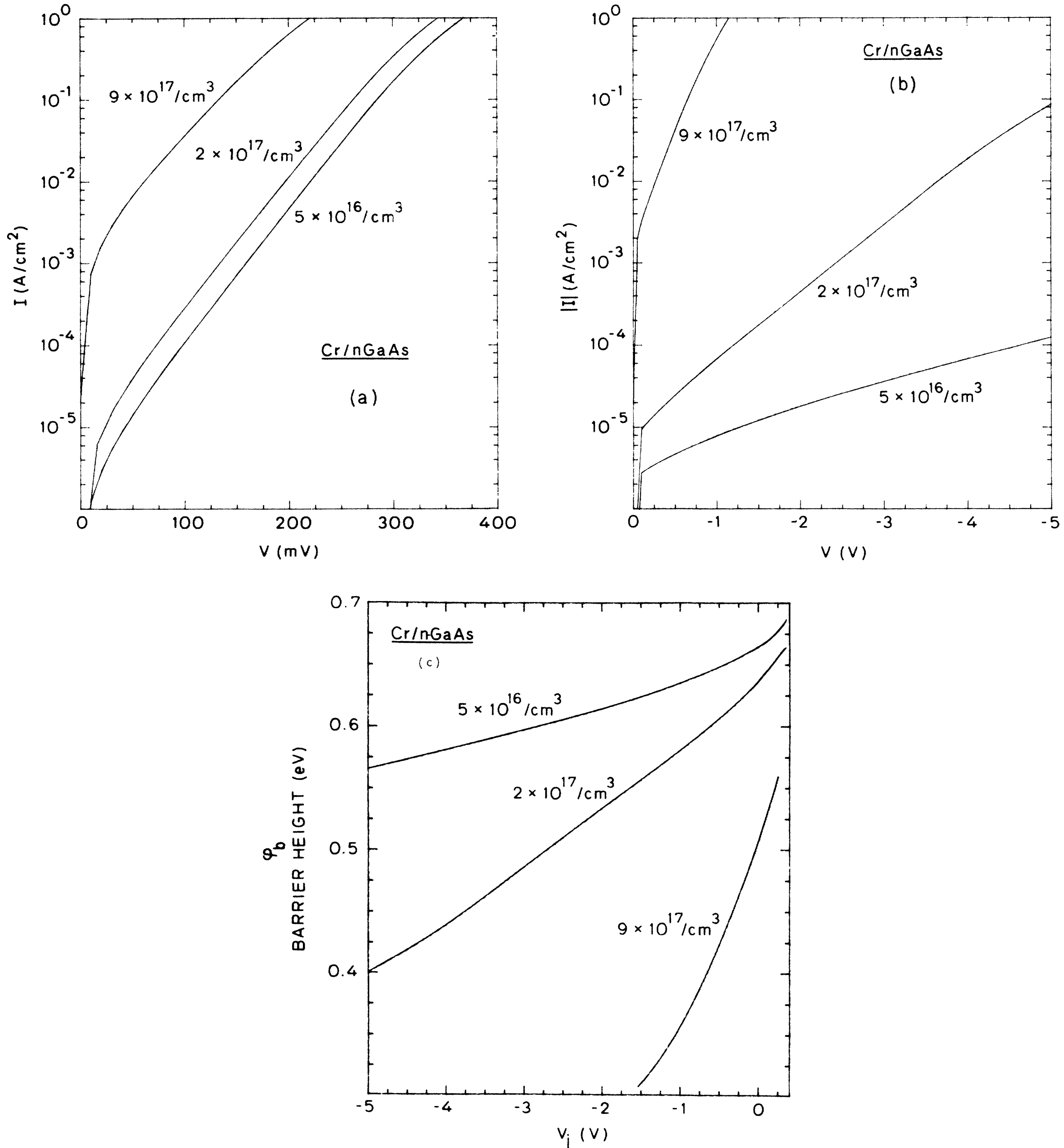


FIG. 4. In order to give a greater range in current and voltage than is shown in Fig. 3, I-V data from Cr/n-type GaAs diodes with several substrate doping levels is presented in (a) forward bias and (b) reverse bias. (c) Determination of the voltage-dependent barrier height (ϕ_b) using the ideal thermionic emission equation, Eq. (5), over a very large voltage range. Note the much stronger voltage dependence on the barrier height for the more highly doped samples. The nonlinearities in (a) at large forward bias are caused by series-resistance effects (due to the significant potential drop across the bulk and contact resistances which occurs when large currents flow).

TABLE I. n-type GaAs Schottky barriers: thick-metal coverages (1000 Å).

	Sample doping: $5\times10^{16}/\mathrm{cm}^3$			Sample doping: $2\times10^{17}/\mathrm{cm}^3$			Sample doping: $9\times10^{17}/\mathrm{cm}^3$		
	$\phi_{b0I\text{-}V}$ I-V barrier height (eV) (±0.02 eV)	n ideality factor	$\phi_{bC\text{-}V}$ C-V barrier height (eV) (±0.05 eV)	$\phi_{b0I\text{-}V}$ I-V barrier height (eV) (±0.02 eV)	n ideality factor	$\phi_{bC\text{-}V}$ C-V barrier height (eV) (±0.05 eV)	$\phi_{b0I\text{-}V}$ I-V barrier height (eV) (±0.02 eV)	n ideality factor	$\phi_{bC\text{-}V}$ C-V barrier height (eV) (±0.05 eV)
Cr	0.67	1.06	0.72	0.64	1.09	0.73	0.51	1.30	b
Mn	0.72	1.05	0.75	0.72	1.09	b			
Sn	0.77	1.06	0.83	0.72	1.12	0.81			
Ni	0.77	1.06	0.82	0.73	1.09	0.77			
Al	0.80–0.85[a]	1.05	0.85–0.90[a]	0.73[a]	1.09	0.77[a]			
Pd	0.85	1.05	0.88	0.80	1.09	0.84			
Cu	0.87	1.05	0.94–1.08	0.83	1.10	0.89			
Ag	0.89	1.05	0.97	0.85	1.08	0.89	0.68	1.32	0.93[c]
Au	0.92	1.05	1.02	0.88	1.10	0.95	0.70	1.32	0.95[c]

[a]Barrier height may be raised due to formation of $Al_xGa_{1-x}As$ at interface.

[b]The high series resistance r for the Mn/n-type GaAs ($2\times10^{17}/\mathrm{cm}^3$) and the low effective barrier (and therefore large parallel conductance G) for the Cr/n-type GaAs ($9\times10^{17}/\mathrm{cm}^3$) diodes did not allow for an accurate C-V barrier-height determination for these systems.

[c]The large conductance at significant reverse bias ($V<0.5$ V) for diodes fabricated on the heavily doped substrates ($9\times10^{17}/\mathrm{cm}^3$) only allowed the C-V measurement to be performed over a voltage range of 0 to 0.5 V reverse bias.

height as determined by Eq. (5) with doping. Note the near linear dependence of the effective barrier height over a range of applied voltage from large reverse bias to significant forward bias in Figs. 3(b) and 4(c).

The barrier height can be expanded in voltage as

$$\phi_b(V_j)=\phi_{b0}+K_1(V_j)+\cdots ,$$

where V_j is the voltage across the junction ($V_j=V-IR$) and $\cdots$ represents the higher-order terms in voltage. Typically, a linear expansion of the effective barrier height in voltage is used so that the forward I-V data can be described by two parameters, ϕ_{b0} (the effective barrier height extrapolated to zero bias) and n (the ideality factor). For significant forward bias (i.e., $e^{(V-IR)/V_t}\gg1$), the thermionic emission equation is typically written as[1]

$$I=SA^*T^2e^{-\phi_{b0}/V_t}e^{(V-IR)/nV_t} . \tag{6}$$

The ideality factor is related to K_1, the linear expansion coefficient of the barrier height by the equation, $K_1=1-1/n$. Therefore, the strong dependence of the effective barrier height on applied voltage in the forward direction is reflected in the significantly greater ideality factors for the more heavily doped substrates.

Using Eq. (6) to fit the forward-bias data, the value of the effective I-V barrier height (ϕ_{b0}) and the ideality factor (n) are presented in Table I. Note the consistent and near-unity ideality factors for the Schottky diodes produced on the most lightly doped substrates. The consistency can also be seen by noting the parallel lines in the log$I$-versus-voltage curves in Fig. 2. Also systematic increases in the ideality factor and decreases in the barrier height for the Schottky diodes produced on the more heavily doped substrates were found. The uniformity between the ideality factor for all of the diodes produced on the same substrate doping is striking. The thermionic emission current can be characterized with a constant ideality factor over the measured forward-bias voltage ranges for all of the systems studied. This is reflected in a linear log$I$-versus-voltage curve in the forward direction as can be seen in Figs. 2 and 3(a). Also, note the differences in the barrier height among the metals are essentially identical for each substrate doping level.

Low-temperature I-V measurements have been performed on several systems (Ag, Au, and Cu for the most lightly doped substrate). Preliminary results of this work indicate that the current-voltage measurements can be successfully characterized by a thermally activated process as is described by Eq. (6). Typical I-V data for various temperatures can be seen in Fig. 5. Changes on the order of the accuracy of the measuring methods and devices were found in the barrier height (<0.06 eV) and in the ideality factor (<0.05) over the temperature range from 100 to 300 K. Note that changes in the band gap over this temperature range are also on the order of 0.06 eV. Because more extensive and accurate measurements are planned, all of the details and results of these experiments are not presented here. Nevertheless, the demonstration that the current-voltage relationship of these intimate metal-semiconductor diodes is a thermally activated process with an activation barrier which is consistent with

barrier-height determinations measured at room temperature is a very important point.

B. Leakage currents

Extreme care is necessary when interpreting *I-V* data. The separation of leakage currents from the thermionic emission current is essential in obtaining consistent results. A leakage current was found which could be characterized by a small-area, low-barrier device in parallel with the large device (whose electrical characteristics were shown in the last section to be accurately characterized by thermonic emission current). The *I-V* characteristics of this leakage current were not found to be consistent with Schockley-Read-Hall recombination.[23] At room temperature, the series-resistance component, in series with Schockley-Read-Hall recombination.[23] At room temperature, the series-resistance component (presumably due to spreading resistance through the small area device), in series with the low barrier, was found to dominate the electrical characteristics for a significant portion of reverse and for small forward bias. Therefore this leakage current typically appeared as a "parallel resistive current" (especially for the large barrier devices because of the much smaller thermionic emission current in these devices).[24] Diodes fabricated over flat areas without steps were found to have the same *I-V* and *C-V* barrier height as diodes fabricated over areas with large steps and other imperfections. However, the diodes fabricated over areas with large steps and other imperfections were typically found to have much larger leakage currents of this type. An example of this can be seen in Fig. 6. Large leakage currents were also found when the periphery of the diode was not abrupt (i.e., not well defined).

The leakage current path was clearly shown to be associated with the periphery. This current path at the periphery of the device can be removed by performing a mesa etch using H_2O:H_2O_2:H_2SO_4 in a ratio of 15:1:1 for 7 min[25] as can be seen in the room-temperature measurements presented in Fig. 7. For at least one diode at room temperature and for a significant fraction of the diodes which were measured at low temperature, this current mechanism appeared as an exponential dependence on the current in a region of small forward bias which was series-resistance-limited at moderate bias. For the device which showed this relationship at room temperature, Fig. 8 shows the effect of removing the current pathway at the periphery of the device by mesa etching. Note the large decrease and eventual removal of this leakage current with each stage of mesa etching[25] using H_2O:H_2O_2:H_2SO_4 in a ratio of 15:1:1. An increase in this peripheral leakage path by over 8 orders of magnitude of current has been found when these intimate Au:*n*-type GaAs diodes are annealed to 430 °C.[26] Mesa etching was also found to successfully remove the leakage currents in the annealed Au:*n*-type GaAs diodes.[26]

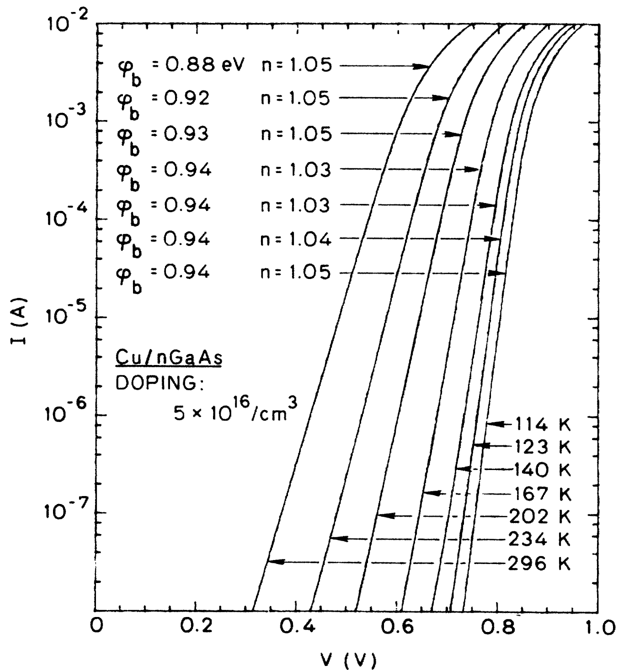


FIG. 5. Typical *I-V* data measured as a function of temperature for a Cu/*n*-type GaAs diode fabricated on a clean cleaved GaAs(110) surface under UHV conditions. Near-unity ideality factors were consistently found at each temperature. The barrier-height determination (ϕ_{b0}) at each temperature using the thermionic emission equation, Eq. (6), was found to be consistent (within experimental error and changes in band gap) with that measured at room temperature. The nonlinearities in the curves at large forward bias are caused by series-resistance effects (due to the significant potential drop across the bulk and contact resistances which occurs when large currents flow).

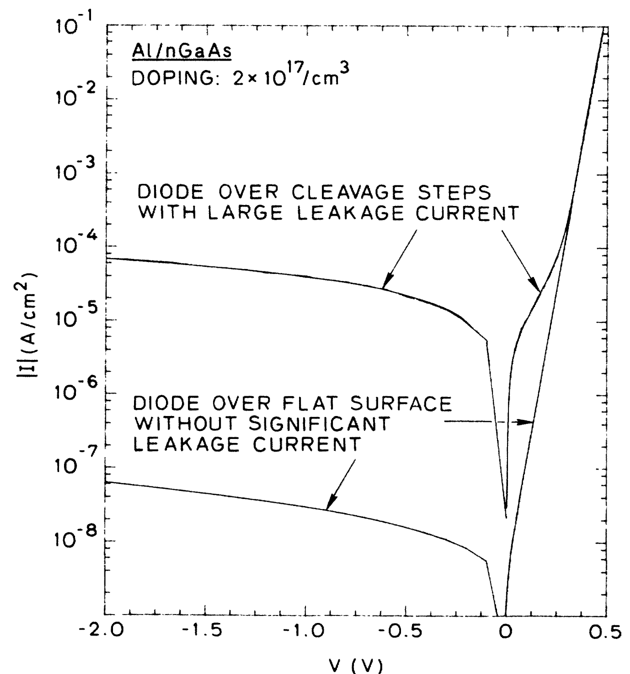


FIG. 6. Several diodes fabricated on the same substrate can be seen. Note the large leakage current which was measured for the diode fabricated over cleavage steps. For this device, the leakage current is found to dominate for reverse bias and small forward bias. Also note the essentially identical magnitude of thermionic emission current which dominates the *I-V* characteristics at significant forward bias ($V > 0.3$ V).

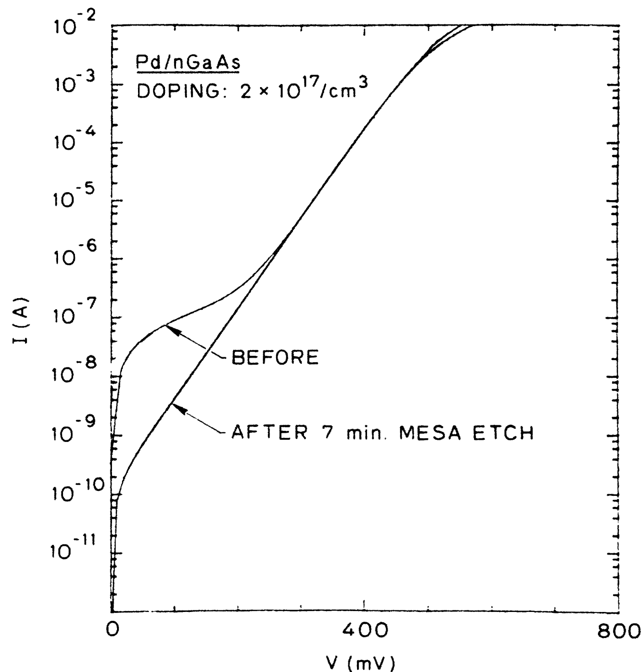


FIG. 7. Removal of the peripheral leakage current by mesa etching can be seen in this figure. Note that the thermionic emission current which dominates the I-V characteristics at significant forward bias ($V > 0.3$ V) is not affected by the mesa etch.

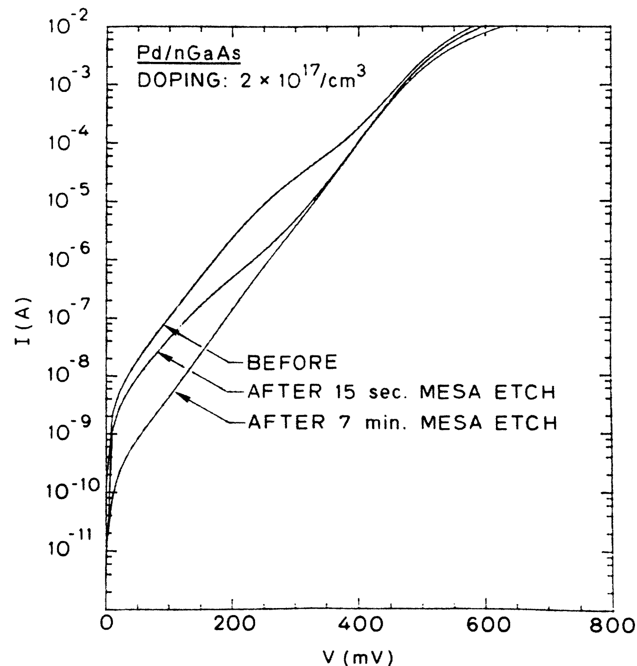


FIG. 8. The peripheral leakage current can be characterized by a small-area, low-barrier device. At small bias the leakage current appears as an exponential dependence on voltage with a near-unity ideality factor, which is attenuated at moderate bias by a large series resistance due to its small area. As can be seen, this peripheral leakage current can be removed by mesa etching. Note that the thermionic emission current at significant voltage is not affected by the mesa etch.

Such behavior is characteristic of a thermionic emission barrier (a large-area device) in parallel with a small-area, low-barrier device (the leakage current), which is attenuated at moderate bias by a large series spreading resistance due to its small area. At small bias the characteristics appeared to have a near-unity ideality factor. Because small activation barriers are attenuated exponentially less than large barriers as temperatures decrease, the leakage current, though not always detectable at room temperatures for the current ranges measured in this experiment, is often found to dominate the electrical behavior over a significant portion of the forward I-V curves at low temperatures. This can be seen in Fig. 9. However, it should be emphasized that the high barrier height dominates the electrical characteristics for all temperatures above 221 K. Similar behavior has been reported by Schwartz and Cho,[27] but that study did not find near-unity ideality factors for the leakage current and did not associate the leakage current with the periphery.

A linear dependence of $1/C^2$ on voltage was found for all of the systems studied in the voltage range of 0–2 V reverse bias. Typical data can be seen in Fig. 10. The diffusion potential of the Schottky diodes was obtained from the intercept of the $1/C^2$-versus-voltage curve[15] using a

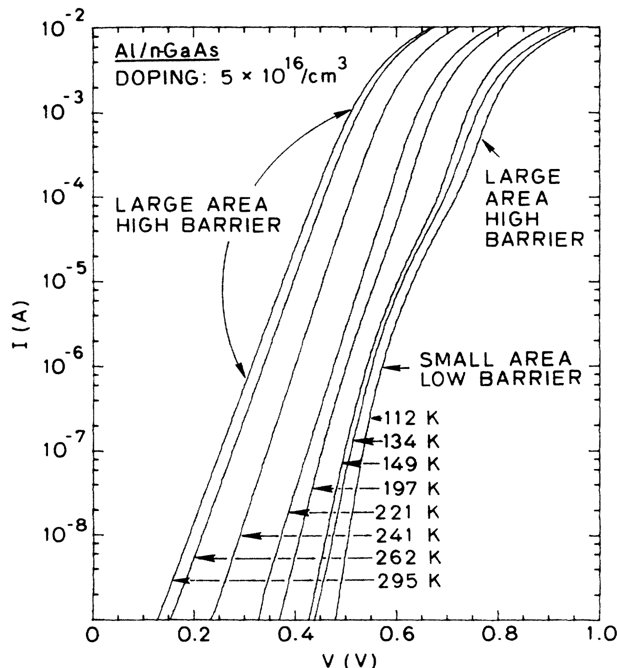


FIG. 9. This figure shows that the peripheral leakage current can be characterized by a small-area, low-barrier device with a near-unity ideality factor. As can be seen, the leakage current appears as an exponential dependence on voltage with a near-unity ideality factor, which is attenuated at moderate bias by a large series resistance due to its small area. Because small activation barriers are attenuated exponentially less than large barriers as temperatures decrease, the leakage current, though not always detectable at room temperatures for the current ranges measured in this experiment, are often found to dominate the electrical behavior over a significant portion of the forward I-V curves at low temperatures.

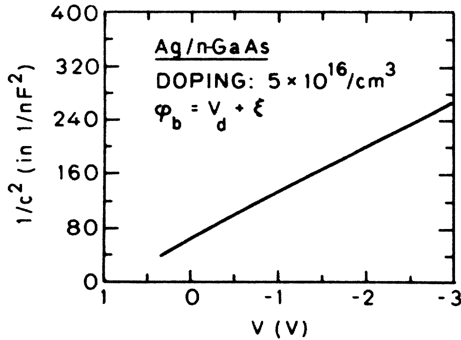


FIG. 10. Typical C-V data from a Ag:n-type GaAs diode fabricated on a clean cleaved GaAs(110) surface under UHV conditions. Note the linear $1/C^2$-versus-voltage relationship for 0 to 2 V reverse bias. The C-V barrier height ($\phi_{bC\text{-}V}$) can be calculated by adding the measured diffusion potential (the intercept of the voltage axis) to the difference between the conduction-band minimum and the Fermi level in the bulk.

least-squares fit over 0—2 V reverse bias. The C-V barrier heights ($\phi_{bC\text{-}V}$) can then be calculated by adding the difference between the Fermi level and the conduction band in the bulk (0.04, 0.02, 0.01 eV for the diodes fabricated on substrates with doping of 5×10^{16}, 2×10^{17}, and $9\times10^{17}/\text{cm}^3$, respectively) to the diffusion potential. The conduction-band density of states N_c and dielectric constant ϵ_s used in the calculations were $4.7\times10^{17}/\text{cm}^3$ and 13.1, respectively. The results of the data analysis can be seen in Table I.

IV. DISCUSSION

A. Introductory comments

In this study, the fabrication of the diodes on a clean cleaved GaAs(110) surface under UHV conditions allowed for a reproducible method of diode fabrication. The resulting consistency in the data allows us to present much more reliable barrier-height determinations using device measurements than has been previously possible. In the remainder of this paper we will concentrate on the implications of the reported barrier-height determinations to the understanding of the physical mechanisms responsible for the formation of the Schottky barrier. An analysis of the physical mechanisms reponsible for the current conduction and barrier lowering in these diodes will be presented in another paper.[28] We will use the barrier heights of diodes formed on the most lightly doped substrates since they are least influenced by the barrier-lowering mechanisms. Corrections of less than 0.04 eV would be expected due to the effects of the image force[1] and tunneling[18] for the devices fabricated on the most lightly doped substrates ($5\times10^{16}/\text{cm}^3$).

Because the metal/GaAs systems in this study were fabricated using similar sample preparation methods as used in surface-sensitive studies, the understanding of the structure and chemistry of intimate metal/GaAs systems which has been recently obtained by the surface-science community can be directly applied to the interfaces investigated in this study. In the following discussion, we will show that the results of the electrical device measurements when compared with the results of the surface-sensitive studies provide a particularly critical test of different models of the Schottky barrier.

B. Correlation of electrical device barrier-height determinations with band-bending determinations during the initial stages of Schottky-barrier formation

Photoemission spectroscopy studies, performed by our group at Stanford[4,10,22] and others,[13,29,30] can measure the amount of band bending during the initial stages of Schottky-barrier formation. For the clean cleaved GaAs surface, it has been experimentally demonstrated that there are no intrinsic surface states within the band gap,[31] and therefore intrinsic surface states cannot be responsible for pinning the Fermi level in Schottky-barrier diodes. However, the Schottky-barrier height is almost completely developed when submonolayer coverages of adatoms are deposited onto the surface.[4,10] This experimental observation that submonolayer coverages of such a broad family of adatoms[4] [including nonmetals such as oxygen (Ref. 32), Sb (Ref. 32), and Ge (Ref. 33)] pin the Fermi level at the same position in GaAs (within experimental error) can be used to rule out bulk metallic states as the primary source of Fermi-level pinning, at least for submonolayer coverages. As can be seen in Table II, the barrier-height determinations for the thick-metal devices are essentially identical to those reported at the initial stages (submonolayer to several monolayers of metal) of Schottky-barrier formation by photoemission spectroscopy. Such consistent agreement is a strong indication that the physical mechanisms responsible for Fermi-level pinning in the thick-metal Schottky diodes is first established at submonolayer to several monolayer coverages of adatoms and an atomic scale model is therefore necessary to account for the data.

In the late seventies, the results of the PES studies and device measurements led to the development of a currently popular atomic level model, the unified-defect model.[4,10] This model hypothesizes that for metal group-III-V semiconductor interfaces, the localized states responsible for pinning the Fermi level at the interface are associated with defects induced by the deposition of the adatom. PES results suggest that a defect which acts as an acceptor occurs at 0.7 ± 0.1 eV below the conduction-band minimum (CBM) and a defect which acts as a donor occurs at 0.9 ± 0.1 eV below the CBM in GaAs. The physical and electronic structure of these localized states has not been completely resolved, and the reader is referred to the literature for further discussions (for example, see Refs. 4, 10, 13, and 33—37). As can be seen in Table II, the interface Fermi-level pinning position as measured for submonolayer to several monolayer coverages of metal in the PES studies is found to be essentially identical to the interface Fermi-level pinning position as inferred by the electrical device measurements on the thick-metal-film (approximately 1000 Å) diodes as was measured in this work. This range in pinning positions is also found to

TABLE II. Group-III-V Schottky barriers. (ML denotes monolayer.)

Metal	n-type GaAs $\phi_{b0I\text{-}V}$ this study clean (110) ($\pm$0.02 eV) doping: $5\times10^{16}/cm^3$	n-type GaAs $\phi_{b0I\text{-}V}$ from Waldrop[a] clean (100) ($\pm$0.01 eV) doping: $6\times10^{16}/cm^3$	n-type GaAs $\phi_{b0I\text{-}V}$ chemically prepared (110)	(100)	Thin metal (sub to several ML) n-type GaAs ϕ_b photoemission results ($\pm$0.10 eV)	n-type InP $\phi_{b0I\text{-}V}$ from Newman *et al.*[b] ($\pm$0.02 eV) doping: $6\times10^{15}/cm^3$	Pauling electronegativity[c]	Work function[d]
Cr	0.67	0.73			0.7[k]	0.45	1.6	4.5
Mn	0.72					0.35	1.5	4.1
Sn	0.77		0.75[f]			0.35	1.8	4.48
Ni	0.77	0.73	0.78[f]		0.7[l]	0.32	1.8	5.15
Al	0.80–0.85[e]	0.81		0.73[g]	0.7[m]	0.325	1.5	4.28
Pd	0.85	0.87		0.865[h]	0.9[n]	0.41	2.2	5.12
Cu	0.87	0.92	0.86[i]		0.9[o]	0.42	1.9	4.26
Ag	0.89	0.86		0.90[f]	0.9[p]	0.54	1.9	4.26
Au	0.92	0.85	0.92[i]	0.93[j]	0.9[q]	0.42	2.4	5.1

[a]From Ref. 49.
[b]From Ref. 16.
[c]L. Pauling, *The Nature of the Chemical Bond* (Cornell University Press, Ithaca, 1960), p. 93.
[d]H. B. Michaelson, J. Appl. Phys. **48**, 4729 (1977).
[e]Barrier height may be raised due to formation of $Al_xGa_{1-x}As$ at interface.
[f]G. B. Seiranyan and Yu. A. Thorik, Phys. Status Solidi A 13, K115 (1972).
[g]From Ref. 52.
[h]E. Hokelek and G. Y. Robinson, Solid State Electron. **24**, 99 (1981).
[i]B. L. Smith, Ph.D. thesis, Manchester University, 1969.
[j]J. Gyulai and J. W. Mayer, J. Appl. Phys. **42**, 3578 (1971).
[k]From Ref. 45.
[l]From Ref. 43.
[m]From Refs. 32 and 41.
[n]From Ref. 44.
[o]From Ref. 42.
[p]From Ref. 40.
[q]From Ref. 46.

agree to first order with calculations of the energy level of several point defects including antisites[34] and vacancies.[35] The electronic interactions which determine the charge state of the defect levels (and therefore the position of the interface Fermi level) are not completely understood. The effects of a bulk metal (using a jellium model),[38] and an atomic polarizability (an atomic model)[39] have been investigated recently. Clearly additional work is needed to obtain a more complete understanding of the physical mechanisms responsible for the small differences between the barrier heights of the metal/GaAs systems.

C. Correlation of electrical data with the chemistry at the interface (or lack thereof)

Photoemission studies have demonstrated that the chemical nature of metal/GaAs interfaces are very diverse. The systems range from a nonreactive abrupt interface (Ag),[40] to interfaces which form metal-arsenide compounds (Al,[32,41] Cu,[42] Ni,[43] Pd,[44] Cr,[43] and Mn) and metal-gallium alloys (Au,[45] Ni,[43] Pd,[44] and Mn). For these metals, the microscopic chemical reactions, as monitored during the initial stages of metal deposition by photoemission spectroscopy, have been found to be consistent with bulk thermodynamic data.[46] We will refer to the thermodynamic model presented by McGilp in which metal-semiconductor anion compound formation and metal-semiconductor cation alloying are included in calculating the heats of reaction. To allow for a more quantitative comparison of the chemical reactivity, thermodynamic data are shown in Table III. Because of the limited availability and consistency in the experimental values, both experimental and theoretical values are included. As can be seen, no apparent trends in the barrier height can be found between the Schottky-barrier height and the type or extent of chemical reaction at the interface. For example, the metal-semiconductor systems in this study, with the four largest barrier heights, include a nonreactive interface (Ag), moderately reactive interfaces (Au, Cu), and a highly reactive interface (Pd). Similarly, no correlation between the barrier height and the type of chemical reactions is found. For example, in the reactive high-barrier-height systems, Au reacts to form predominantly an alloy with Ga, Cu reacts to form predominantly an arsenide, and Pd reacts to form both an alloy with Ga and an arsenide, yet the barrier heights of the Schottky diodes formed with these metals are very similar.

D. Correlation of electrical data with work function (or lack thereof)

As can be seen in Table II, no strong correlation of the barrier height with the work function of the metal overlayer is found. This can be used to rule out the original Schottky model as proposed in 1939.[47] More recently, Freeouf and Woodall have proposed a modification of this model, in which the work function is replaced by an effective work function which is a value that corresponds to an average of the chemical phases at the interface.[48] Although the lack of detailed information concerning the chemical composition at the metal-semiconductor interface and the very large uncertainty in the available work-function data (typically 0.5—1.0 eV) makes this model difficult to address; some inconsistencies are apparent. For example, in the systems which produce high barriers on GaAs, the metals have a large range in work function (4.26—5.12 eV) and quite different chemical products are formed at the interface (Ag is found to be unreactive; Au reacts to predominantly form an alloy with Ga, Cu reacts to form predominantly an arsenide, and Pd reacts to form both an alloy with Ga and arsenide), yet the barrier heights of the Schottky diodes formed with these metals are very similar. This lack of correlation between the bar-

TABLE III. Thermodynamic data.

Metal	Heat of formation, ΔH_f metal:As(1:1) theoretical[a] (experimental) (eV/As atom)	ΔH_f Ga:metal alloy (1:∞) theoretical[a] (eV/Ga atom)	Heat of reaction[b], H_r, using the theoretical data[a] (eV/GaAs molecule)	$\phi_{b0I\text{-}V}$ (doping: $5\times10^{16}/\text{cm}^3$) (eV)
Cr	−0.99	−0.03	−0.17	0.67
Mn	−1.35 (−0.59[c])	−0.62	−1.12	0.72
Sn		+0.03		0.77
Ni	−0.97 (−0.75[c])	−0.71	−0.83	0.77
Al	(−1.27[c])	+0.04	−0.42[e]	0.80—0.85
Pd	−1.55	−1.76	−2.46	0.85
Cu	−0.48 (CuAs)	−0.27	+0.10 (CuAs)	
	−0.75(−0.12[d]) (Cu_3As)		−0.17 (Cu_3As)	0.87
Ag	−0.31	−0.22	+0.32	0.89
Au	−0.48	−0.77	−0.40	0.92

[a]A. R. Miedema, F. R. de Boer, and R. Boom, CALPHAD **1**, 341 (1977); A. R. Miedema, P. F. de Chatel and F. R. de Boer, Physica **100B**, 1 (1980).

[b]Heat of reaction of metal + GaAs→metal:As(1:1) + dilute Ga:metal alloy (1:∞). A value of −0.85 eV/As atom was used for ΔH_f of GaAs (footnote d).

[c]O. Kubaschewski and C. B. Alcock, *Metallurgical Thermochemistry* (Pergamon, New York, 1979).

[d]Donald D. Wagman, William, H. Evans, Vivian B. Parker, Richard H. Schumm, Iva Hallow, Sylvia M. Balley, Kenneth L. Churney, and Ralph L. Nuttall, J. Phys. Chem. Ref. Data **11**, Suppl. 2, (1982).

[e]Theoretical value from footnote a is not available for AlAs; the experimental value from footnote c was used instead.

riers heights with the combination of the chemistry and work function of the metal makes the barrier-height determinations reported in this study difficult to understand within the context of the effective work-function model. Nevertheless, more work is needed to obtain detailed information concerning the chemical composition at the metal-semiconductor interface before this model can be critically evaluated.

E. Correlation with other group-III-V diodes, different crystal faces, and different surface preparations

As can be seen in Table II, very good agreement is found between the Schottky-barrier height of diodes formed on clean cleaved (110) (from this study), on heat-cleaned (100),[49] and on chemically prepared GaAs surfaces.

To a first approximation, the Schottky-barrier height is found to be independent of the surface orientation of the substrate. The band-bending determinations during the initial stages of Schottky-barrier formation as monitored by photoemission spectroscopy on heat-cleaned GaAs(100) (Ref. 30) and on molecular beam epitaxy grown GaAs(100) surfaces[50] are found to be essentially identical to that on clean cleaved GaAs(110) (Refs. 4, 22 and 45) surfaces. Furthermore, the values reported by Waldrop on diodes formed on heat-cleaned GaAs(100) surfaces are in almost all cases within experimental error of the values reported here for diodes formed on the most lightly doped GaAs(110) substrate. Some small, but significant differences in the electrical characteristics do exist. The ideality factors are found to vary significantly between the different metal/GaAs systems in the study of Waldrop, while essentially no differences are found in this study. Differences in the trends in the barrier heights between the metals also exist. For example, Au is found to consistently form the highest barrier height on GaAs(110) surfaces at each substrate doping, while on the (100) surface Cu is found to have a higher barrier height than Au by 0.06 eV, a significant difference.

As can be seen in Table II, the barriers heights of diodes formed on clean cleaved surfaces and contaminated (i.e., air exposed and/or chemically prepared) surfaces are found to be remarkably similar. The chemical composition and morphology of an interface which is formed when a metal is deposited on a chemically prepared and/or air-exposed surface is not very well understood. The thin GaAs native oxide has been reported to be 10—20 Å thick,[6,51] and the presence of this impurity layer has been shown to have important effects on the chemistry at the interface during the initial stages of metal deposition.[5,6] Nevertheless, the barrier-height determinations using electrical device measurements of diodes formed on clean and on chemically prepared GaAs surfaces are found to be essentially identical. (See Table II.) This is a strong indication that the same physical mechanism is responsible in pinning the Fermi level in each metal/GaAs system, independent of the surface preparation. Because submonolayer to several monolayers of an adatom can pin the Fermi level,[4,10] the diffusion of even small amounts of the metal through the oxide or the reaction of the metal with the oxide to form an interface region which consists of a mixture of metal and metal oxide[6] may explain the essentially identical interface Fermi level pinning position for metals produced on clean and contaminated GaAs interfaces.

The Al/GaAs system is an interesting exception to this. As Table II illustrates, the thick-metal-film devices fabricated on clean surfaces are found to have a significantly larger barrier height than thick-metal-film devices formed on contaminated surfaces[52] or thin-metal-film systems used in PES.[32,41] PES has shown that the deposition of Al on a clean GaAs surface at room temperature can result in an exchange reaction in which Al replaces the Ga in the GaAs lattice and free Ga is formed.[29,32,53] As was found for device measurements on direct-band-gap (i.e., small x) $Al_xGa_{1-x}As$ surfaces,[54] the Fermi level to CBM energy difference at the interface increases due to the increased band gap of $Al_xGa_{1-x}As$ (resulting in an increase in the barrier to electrons and thus the I-V barrier height), although the distance from the valence-band maximum to the interface Fermi level (which is the quantity measured by PES) may not be changed.[53] This is further substantiated by a recent study which found that upon annealing, the enhancement of the exchange reaction as monitored by photoemission spectroscopy[29,53] can be directly correlated with a significant increase (0.10 eV) in the relative I-V barrier height as measured by the electrical device measurements.[53] The PES measurement would therefore underestimate the barrier height to electrons if the smaller band gap of GaAs was used to induce the distance from the CBM to the interface Fermi level when an $Al_xGa_{1-x}As$ region is present at the interface. The significantly smaller barrier height for the Al deposited on the oxidized surface can be attributed to the reduction and possible elimination of the larger-band-gap $Al_xGa_{1-x}As$ region at the interface. The deposition of Al on the oxidized GaAs surface leads to a reduction of the native oxides, and the formation of an aluminum oxide.[6] This reaction would be expected to dominate the chemistry at the interface, and a large decrease, and possible elimination of the replacement reaction, would be expected.

We recently reported a study of Schottky barriers on clean cleaved InP(110) surfaces using the same nine metals as in this study.[16] A comparison with InP is particularly interesting because similar trends in the chemical reactions are found at the metal-semiconductor interface, although InP interfaces are, in general, more reactive.[55] The barrier heights of diodes formed on each semiconductor were found to fall within a relatively narrow range of energy (ϕ_{b0}InP: 0.32—0.54 eV; ϕ_{b0}GaAs: 0.67—0.92 eV), although the interface Fermi-level pinning position was found to fall lower in the band gap for GaAs than for InP. A strong correlation was found between metals that form a high (low) barrier height on GaAs and those which form a high (low) barrier height on InP.[56] Although the physical mechanism responsible for the small differences between the barrier heights of the metals is not very well understood, this correlation suggests that a common mechanism occurs in the GaAs and InP system.

V. CONCLUSIONS

The barrier-height determinations for the thick-metal devices, as reported in this study, were found to be essentially identical to those reported during the initial stages of Schottky-barrier formation (submonolayer to several monolayers of metal) by photoemission spectroscopy. This agreement indicates that the physical mechanisms responsible for Fermi-level pinning in the thick-metal Schottky diodes is first established at submonolayer to several monolayer coverages of adatoms and an atomic level model is therefore necessary to account for the available experimental data. No strong correlation between the barrier heights and the work function of the metal or chemistry at the interface was found. Also, the diodes formed on the clean GaAs(110) surfaces were found to have essentially identical barrier heights to those formed on clean GaAs(100) surfaces and on contaminated (i.e., chemically prepared) GaAs(100) and (110) surfaces. Several currently popular models were discussed, and the unified-defect model was found to be most consistent with the experimental data.

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[2]C. A. Mead and W. G. Spitzer, Phys. Rev. **134**, A713 (1964).

[3]The only previous systematic electrical study on cleaved semiconductor surfaces was presented over 20 years ago in Physical Review by Mead and Spitzer. This early work used diodes which were fabricated under much poorer vacuum conditions (high vacuum, 10^{-6} to 10^{-7} Torr) and at a much faster rate of evaporation than is typically used in the surface studies. With the advances in the experimental techniques (i.e., ultrahigh vacuum, 10^{-10} to 10^{-11} Torr) and in the understanding of the metal/GaAs interface on an atomic level, the need for an investigation of Schottky-barrier diodes on cleaved GaAs(110) surfaces using similar sample preparation methods as the surface-science studies became apparent. A comparison of the results of such a study with studies of diodes prepared on other clean III-V semiconductor surfaces [for example using different crystal faces (Ref. 49) and different group III-V semiconductors (Ref. 16)] is expected to be a particularly critical test of models of Schottky-barrier formation.

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[9]For example, the forward *I-V* curves of the diodes in the Mead and Spitzer study (Ref. 2) were reported to be problematic, and values for the *I-V* barrier height determination was not listed for that reason. By separating the effects of leakage currents from the thermionic emission current, we were able to obtain much more consistent and reproducible barrier-height determinations than has been previously possible.

[10]W. E. Spicer, S. Eglash, I. Lindau, C. Y. Su, and P. Skeath, Thin Solid Films **89**, 447 (1982), and literature therein.

[11]G. Margaritondo, Solid-State Electron. **26**, 499 (1983), and literature therein.

[12]I. Lindau and W. E. Spicer, in *Electron Spectroscopy: Theory, Techniques and Applications,* edited by C. R. Brundle and A. D. Baker (Academic, New York, 1981), Vol. 4, p. 197, and literature therein.

[13]L. J. Brillson, Surf. Sci. Rep. **2**, 123 (1982), and literature therein.

[14]For a description of the IMPACT system, see Robert B. Lefferts, Ph.D. thesis, Stanford University, 1981, p. 65.

[15]A. M. Goodman, J. Appl. Phys. **34**, 329 (1963).

[16]N. Newman, T. Kendelewicz, L. Bowman, and W. E. Spicer, Appl. Phys. Lett. **46**, 1176 (1985).

[17]High electric fields at the periphery of planar devices can induce large peripheral currents due to barrier-lowering effects and breakdown, especially in reverse bias. Because of the large size of the diodes in this study, and therefore a very large ratio of area to peripheral length, these edge effects are not expected to dominate the electrical characteristics of the devices. This was experimentally verified by using a mesa structure which would reduce, and even eliminate, the large electric fields at the periphery of the device. No significant differences were found in the measured thermionic emission current in both the forward- and reverse-bias data after mesa etching

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[25]The etch rate of this solution in GaAs is slightly less than 1 μm/min, and therefore only a small change (on the order of 1% or less) in the total area of the device would be expected. By monitoring the slope of the $1/C^2$-versus-voltage curve, changes in the total area of the device can be determined. These measurements also indicate that the change in area by mesa etching is very small and would not significantly affect the thermionic emission barrier-height determination.

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