

## Chemical reaction and Schottky-barrier formation at V/Si interfaces

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(Received 25 July 1983)

The behavior of the V/Si interface has been studied under atomically clean interface conditions for a variety of Si surfaces [Si(111)-(7×7), Si(111)-(2×1), and Si(100)-c(4×2)] as a function of annealing used to promote the silicide formation reaction. Interface chemistry (composition, reactivity, and electronic structure) was revealed by angle-integrated ultraviolet (UPS) and x-ray photoemission spectroscopy and by Auger-electron spectroscopy (AES); transmission electron microscopy (TEM) and low-energy electron diffraction (LEED) were used to assess interface and surface atomic structure and microstructure; and the Schottky-barrier height  $\phi_{bn}$  was monitored by synchrotron-radiation-photoemission measurements of Si(2p) core-level band bending. In contrast to the behavior for near-noble metals, the interface reactivity between the refractory metal V and the Si substrate is sufficiently low that even under atomically clean conditions no spontaneous intermixing reaction involving atomic motion across the interface occurs at room temperature. Instead, as seen by UPS and AES, simple chemisorption of V atoms on the Si substrate occurs, which is followed by the growth of polycrystalline V metal at higher V coverage. As expected from previous thin-film studies, the stable high-temperature product of the reaction at 500–550 °C is identified to be VSi<sub>2</sub> by TEM phase analysis, by AES composition analysis, and by its characteristic UPS spectrum. However, surprising new information is obtained upon annealing at lower temperatures ( $\leq 350$  °C): Strong intermixing of V and Si atoms across the initially abrupt interface proceeds even through a relatively thick layer ( $\sim 100$  Å or more). This low-temperature intermixed overlayer is characterized by an average surface composition of VSi, by UPS spectra which are different from those of VSi<sub>2</sub> and unreacted V, and by the presence of the VSi<sub>2</sub> compound phase in a matrix of V metal. This low-temperature intermixing behavior represents a new and important aspect of the metal/Si interfacial reaction, which has now been observed because of the high sensitivity of surface-spectroscopy techniques and the preparation of atomically clean, well-ordered Si surfaces and interfaces. Its implications become even more striking in view of the observation that the Schottky-barrier height  $\phi_{bn} \sim 0.64$  eV of the fully reacted VSi<sub>2</sub>/Si contact is already attained once this low-temperature intermixing process occurs. Although the character of the interfacial reaction is more complex in this case, it is clear that the basic interface reactivity associated with silicide-compound formation dominates the microscopic chemistry and properties of this refractory-transition-metal/Si interface and is strongly correlated with the Schottky-barrier electrical characteristics as well.

### I. INTRODUCTION

Although the rectifying (non-Ohmic) character of metal-semiconductor contacts has been known for over a century,<sup>1</sup> a fundamental understanding of the mechanisms which determine the electrical (Schottky-) barrier height of such contacts is still lacking. The first model, proposed by Schottky,<sup>2</sup> simply correlates the barrier height  $\phi_{bn}$  directly with the metal work function  $\phi_m$  and seems reasonably valid for ionic, large-band-gap semiconductors such as ZnO, SiO<sub>2</sub>, or Al<sub>2</sub>O<sub>3</sub>;<sup>3</sup> for covalent semiconductors such as Si, Ge, or GaAs, however,  $\phi_{bn}$  is only weakly dependent on  $\phi_m$ . Attempts have been made to explain this by surface<sup>4</sup> and interface<sup>5–8</sup> electronic states, metal wave-function tails,<sup>5</sup> interface dipoles,<sup>9</sup> and band-gap shrinkage.<sup>10,11</sup> Chemical trends in the sensitivity of  $\phi_{bn}$  to the metal work function have been assessed by introducing an interface parameter  $S$  which quantifies this sensitivity.<sup>12</sup> More recently the strong chemical reactivity of most metal/semiconductor interfaces has been recognized in

Schottky-barrier theories which invoke chemical bonding of bulk silicide compounds produced by interfacial reaction,<sup>13–16</sup> and in experimental observations of the consequences of such interface reactivity, including compound formation,<sup>17,18</sup> interface electronic states,<sup>19–22</sup> defects,<sup>19,20,23–25</sup> and metal-atom impurities.<sup>18</sup>

At the same time there has been growing fundamental interest in measuring and understanding the microscopic properties of metal/semiconductor interfaces. Over the past few years it has become possible to measure (1) interface electronic structure and composition using surface-spectroscopy techniques, (2) interface atomic structure by ion scattering, channeling, and transmission electron microscopy (TEM), and (3) interface electrical properties by photoemission core-level band bending, surface photovoltage, and work function at low metal coverage, as well as by standard electric transport techniques ( $I$ - $V$ ,  $C$ - $V$ , and photoresponse) for bulk contacts. These results may lead to significant progress in understanding interface characteristics on a microscopic scale.

Transition-metal/Si and silicide/Si interfaces represent particularly attractive metal/semiconductor interfaces for investigations of interface chemistry and Schottky-barrier questions.<sup>25–27</sup> This is because (1) Si technology dominates the microelectronics industry, (2) the chemistry is simplified somewhat by use of an elemental semiconductor, (3) considerable information on this chemistry has already been obtained from thin-film studies of silicide formation involving transition metals, (4) reacted silicide/Si contacts produce a clean interface below the initial contaminated interface which has highly reproducible electrical properties, (5) these reacted contacts have a high thermal stability and sometimes good resistance to oxidation, and (6) available Schottky-barrier heights cover a reasonable range, from  $\sim 0.5$  to  $\sim 0.85$  eV (of the 1.12-eV Si band gap). Particularly for the last three reasons, transition-metal— and silicide-contact metallurgies have become important in Si microelectronics technology.<sup>28</sup>

To date, experimental investigations using the new techniques have concentrated primarily on the near-noble transition metals,<sup>22,25</sup> especially Pd, Ni, and Pt. Here we present the results of the first detailed study of the chemistry and Schottky-barrier properties of V/Si as a representative of the refractory-transition-metal/Si interface; some preliminary results of this study have been summarized previously.<sup>29–31</sup>

Only one stable V silicide compound,  $\text{VSi}_2$ , is known to form by contact reaction at the clean V/Si interface.<sup>32,33</sup> Although bulk  $\text{VSi}_2$  formation is energetically very favorable (heat of formation  $\Delta H \sim 25$  kcal/g-at.), it has previously been observed only at relatively high temperatures ( $\sim 500^\circ\text{C}$ ) due to a fairly large activation energy for the silicide-formation process ( $\sim 2.9$  and  $1.8$  eV for the  $t$  and  $\sqrt{t}$  growth behaviors, respectively).<sup>32</sup> As a result, different kinetic behavior is expected, and observed, compared to that for the near-noble transition metals. Other manifestations of the different character of refractory-transition-metal versus near-noble transition-metal atoms in their silicide properties include a tendency for formation of Si-rich rather than metal-rich silicide phases, as well as lower ( $n$ -type) Schottky-barrier heights  $\phi_{bn}$  (i.e.,  $\phi_{bn} = E_C - E_F$ , where  $E_C$  is the energy of the conduction-band minimum and  $E_F$  is the Fermi energy). For studies of interface electronic structure, it is important to note that Auger-electron spectroscopy (AES) spectra for the Si  $L_{2,3}VV$  transitions, associated with the Si valence electronic structure, are not greatly modified by refractory-metal silicide formation (compared to the near-noble-metal case),<sup>34</sup> so that correspondingly greater reliance must be made on photoemission studies of the valence electronic structure and density of states.

## II. EXPERIMENTAL TECHNIQUES

To evaluate the chemistry, electronic properties, and microstructure of the interface and their correlation with the Schottky-barrier height, it is necessary to combine several different experimental techniques. Detailed ultraviolet-photoemission-spectroscopy (UPS) and AES studies, accompanied by some x-ray-photoemission spectroscopy (XPS) measurements, were employed to deter-

mine interface electronic structure, composition, and reactivity. These surface-spectroscopy techniques were complemented by *in situ* low-energy electron diffraction (LEED) observations of surface atomic order. Interface and overlayer lattice structure (silicide phase) and microstructure were analyzed by TEM studies on samples after removal from vacuum. Schottky-barrier-height measurements were made at low metal coverages using synchrotron-radiation-photoemission observations of shifts in Si( $2p$ ) core-level binding energies, which give changes in the Si band bending and barrier height at the interface.

The surface-spectroscopy experiments (UPS, AES, XPS, and LEED) were made in a (ultrahigh-vacuum) (UHV) chamber with an operating pressure of  $\sim 1\text{--}2 \times 10^{-10}$  Torr. The primary sample-measurement position was at the focus of a large ( $\sim 10$ -in.-o.d.) double-pass cylindrical-mirror analyzer (CMA). The CMA included an 8-keV internal electron gun for AES. Other facilities at this sample position included a differentially pumped rare-gas discharge lamp to produce ultraviolet light for UPS, a twin-anode differentially pumped x-ray source for XPS, a sputter ion gun for sputter-cleaning the sample *in situ*, and evaporation sources for the *in situ* deposition of metal overlayers. A four-grid LEED system was located at a second sample-measurement position for observation of long-range surface order. The sample was mounted on a large-stroke manipulator so it could be moved between these two positions as well as translated in the two orthogonal directions and rotated about two axes.

Si samples were prepared from  $n$ -type wafers (10  $\Omega$  cm resistivity, and 0.010 in. thick) with (111) and (100) orientations. To achieve uniform and reproducible sample heating both for annealing after sputter-cleaning and for thermal processing of the interface, a thin Ta layer ( $\sim 1000\text{--}2000$  Å) was first deposited on the back side of the wafers. The wafers were then cut into rectangular shapes measuring  $0.75 \times 0.25$  in. Clearance holes were then ultrasonically drilled in each end of the samples to accommodate Ta screw-and-nut assemblies used as high-temperature mechanical contacts. Ta wires (0.015 in. diam) were spot-welded to these assemblies to mechanically support the samples, which could thus be annealed to greater than or equal to  $1000^\circ\text{C}$  by direct resistive heating. With this arrangement, uniform heating to within  $\pm 50^\circ\text{C}$  was attained even at high temperatures over the entire region ( $\sim 0.25 \times 0.40$  in.<sup>2</sup>) between the screws, and the electrical resistance of the sample package was quite reproducible. The temperature of the sample was monitored by a Chromel-Alumel thermocouple spot-welded to one of the Ta screw contacts, and the actual sample temperature was then calibrated with a standard optical pyrometer at higher temperatures ( $> 600^\circ\text{C}$ ) and an infrared pyrometer in the range  $200\text{--}600^\circ\text{C}$ .

The Si-sample surfaces were cleaned by *in situ*  $\text{Ar}^+$  sputtering (500 eV) and consequent annealing to  $\sim 950^\circ\text{C}$  to restore the ordered crystal structure of the surface. For the Si(111) surface this gave the well-known Si(111)-(7 $\times$ 7) LEED structure, while for the Si(100) surface it gave a (2 $\times$ 1) LEED reconstruction with faint (4 $\times$ 2) spots, i.e., the Si(100)- $c$ (4 $\times$ 2) structure. Surface cleanliness was as-

essed by AES, which showed no contaminants (C, O, etc.) to a sensitivity  $\sim 0.2\%$  of the Si  $L_{2,3}VV$  intensity; under these conditions the UPS spectra (He I,  $h\nu=21.2$  eV) revealed clearly the detailed intrinsic surface-state features previously documented.<sup>35,36</sup>

Initially, thin V overlayers (0.1–20 monolayers) were deposited by direct sublimation from a pure, resistively heated V wire in the main UHV chamber. However, this procedure brought about two problems. First, the high source temperatures required to evaporate refractory metals necessitated tedious outgassing procedures prior to evaporation to prevent residual gas contamination during and after the metal deposition in the experiment. Second, since reasonable evaporation rates required temperatures near the melting point for the V-wire source, the evaporation filaments tended to develop hot spots and then fail (open at a melted region), so that stable evaporation conditions were not easy to attain.

To solve these problems, a separate evaporation chamber was built and connected to the main UHV chamber by a UHV gate valve. With a low-conductance tube between these chambers in the line of sight between the evaporation source and the sample, and with separate ion-sublimation pumping of the evaporation chamber, metal depositions could be made onto the sample in its measurement position without additional residual gas contamination from the evaporation source; the differential pumping of the evaporation chamber kept the main chamber pressure rise to  $\sim 10^{-3}$  of that in the evaporation chamber. A simple  $e$ -beam evaporation source was constructed and employed in the evaporation chamber to overcome the instabilities of the wire-sublimation technique. Use of a differentially pumped, isolatable evaporation chamber also permitted change of the evaporation source without opening the main UHV chamber and provided a convenient location for a quartz crystal-thickness monitor with sensitivity of  $\pm 5\%$  of a monolayer at the sample. Deposition rates up to  $\sim 3$  Å/min at the sample have been achieved.

Additional photoemission measurements of the Si( $2p$ ) core levels as well as valence electronic structure were made<sup>31</sup> using synchrotron radiation from the 240-MeV Tantalus-I electron storage ring at the University of Wisconsin—Madison; these studies employed a UHV toroidal-grating monochromator and a two-dimensional (2D) display-type electron spectrometer.<sup>37</sup> Since the core levels could be determined with a resolution of  $\sim 150$  meV, core-level shifts indicative of changes in Si band bending and Schottky-barrier heights as small as  $\sim 10$  meV could be detected. In these cases metal depositions were made by direct sublimation from a pure V wire; additional studies were also carried out on the Si(111)-(2 $\times$ 1) surface obtained by *in situ* cleavage of  $p$ -type 10- $\Omega$  cm bulk Si samples.

### III. CHEMICAL PROPERTIES OF THE UNREACTED V/Si INTERFACE

Knowledge of the initial microstructure and electronic properties of the as-deposited V film is a proper starting point for understanding the reaction behavior at the V/Si

interface upon thermal annealing. Therefore we first discuss the growth of the V overlayer at room temperature over a wide thickness range.

Figure 1 shows the relative AES intensities for Si and V transitions as a function of V coverage up to a value where all transitions from the Si substrate have essentially vanished. The Si  $L_{2,3}VV$  and  $KLL$  intensities decay exponentially while the V signal rises asymptotically to 1 (pure V). This behavior demonstrates that the V film achieves complete coverage, with only statistical fluctuations in thickness (no strong three-dimensional island formation), and that no V-Si mixing across the interface occurs. A numerical fit to the experimental data gives escape depths close to those obtained in previous investigations:<sup>20</sup> Si  $L_{2,3}VV$ , 8 Å; Si  $KLL$ , 20 Å; and V  $L_{2,3}M_{2,3}V$ , 7 Å. Since the Si  $L_{2,3}VV$  (more surface sensitive) and  $KLL$  (more bulk sensitive) Auger lines show the same behavior, a mixing reaction underneath the top surface but over several angstroms deep can also be ruled out.

However, with the (7–12)-Å depth resolution of these AES-intensity measurements, it is difficult to clearly ascertain the character of the film on the scale of the first  $\sim 3$  Å or less. In this regime the reactivity question may be more effectively addressed by observing the interface chemical bonding (electronic structure). Figure 2 shows the UPS spectra for clean Si(100) and for successive depositions of V at room temperature. The clean Si(100) spectrum shows bulk Si features and intrinsic surface states<sup>35</sup> near  $-0.7$  and  $-1.3$  eV (referenced to an energy zero at  $E_F$ ). Upon deposition of V the intrinsic surface states are quenched, the bulk Si emission features are suppressed, and increasing V-derived emission intensity is observed [primarily V( $3d$ ) states close to  $E_F$ ]. At high coverages the UPS spectrum for the bulk V film is dominated by a strong V( $3d$ ) peak between  $-1$  eV and  $E_F$ .

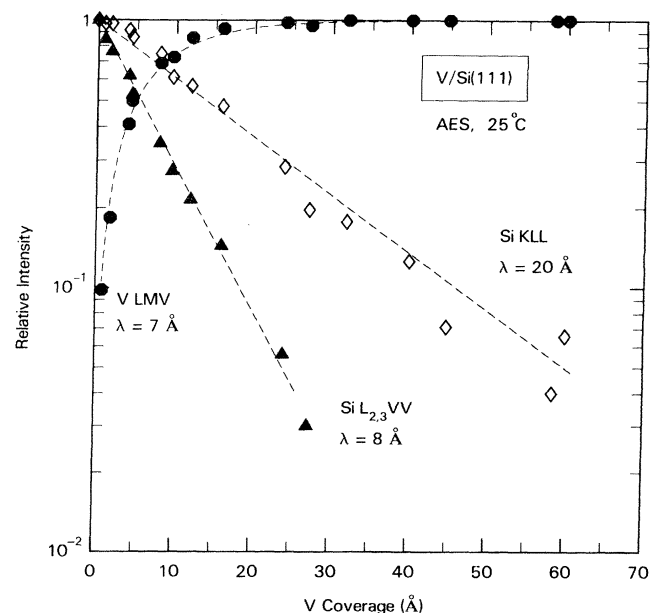


FIG. 1. AES intensity behavior of Si  $L_{2,3}VV$  and  $KLL$  and V  $L_{2,3}M_{2,3}$  transitions vs V coverage deposited at room temperature.

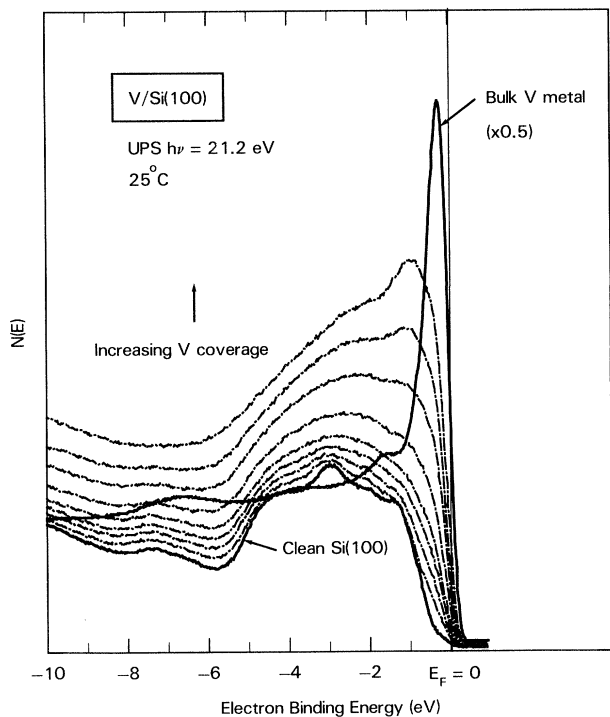


FIG. 2. UPS ( $h\nu=21.2$  eV) spectra for clean Si(100) and for increasing coverage (submonolayer to  $\sim 3$  monolayers) of V deposited at room temperature.

The chemical bonding at low coverage is best evaluated from the incremental difference curves (IDC's) obtained by subtracting successive UPS spectra, as shown in Fig. 3. These IDC's are observed to consist of two parts: (1) valleys which appear at the energy positions of peaks in the clean Si spectrum [shown in Fig. 3(a)] and are caused by attenuation of Si substrate emission and quenching of intrinsic surface states, and (2) strong emission enhancement in the energy region between  $-1$  eV and  $E_F$ . Since the latter bears strong similarity to the characteristic UPS spectrum of bulk V metal, we conclude that the V/Si interface is indeed unreacted at very low coverage (i.e., very close to the Si interface) at room temperature. Also shown, in Fig. 3(g), is the UPS spectrum of the  $\text{VSi}_2$  reaction product obtained by annealing as described below; the low-coverage IDC's clearly do not resemble the  $\text{VSi}_2$  spectrum, in which the emission maximum is at  $-1.6$  eV; this again confirms the conclusion that the V/Si interface is unreacted at room temperature.

Upon V deposition only minor changes are observed in the low-energy tail of the Si  $L_{2,3}VV$  Auger spectrum. The V Auger spectra are virtually identical to those for bulk V metal, except for the appearance of weak additional features which appear at low coverage between the  $L_{2,3}M_{2,3}M_{2,3}$ ,  $L_{2,3}M_{2,3}V$ , and  $L_{2,3}VV$  transitions of V, as discussed below. A small shift ( $\sim 0.2$  eV) of the Si  $L_{2,3}VV$  spectrum to higher energies also occurs, while the V Auger transitions shift in the opposite direction. The chemical shifts of the Si and V core levels observed by XPS are less than 0.2 eV.

Additional insight into the electronic properties and microstructure of the growing V film is obtained from the

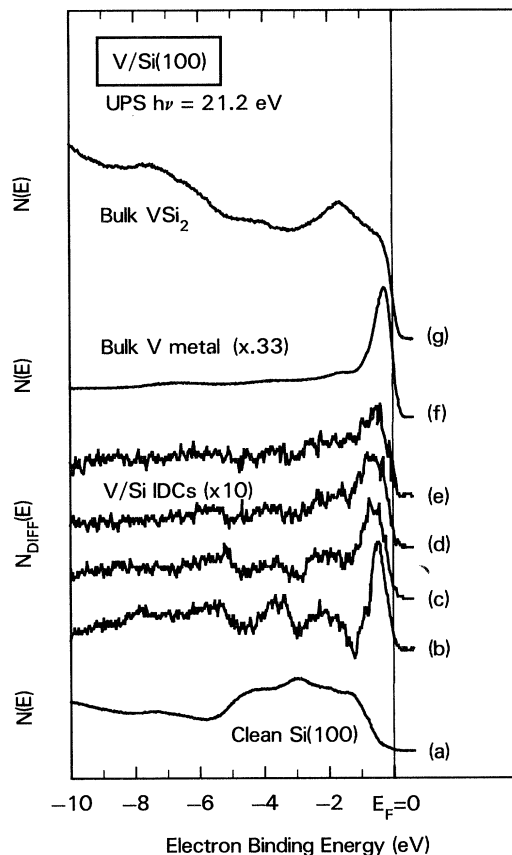


FIG. 3. UPS ( $h\nu=21.2$  eV) spectra: (a) clean Si(100), (b)–(e) successive V depositions in the submonolayer range, (f) bulk V metal; (g)  $\text{VSi}_2$  compound.

valence-band UPS spectra shown in Fig. 4 for V depositions on the cleaved Si(111)-(2 $\times$ 1) surface. Consistent with the results for Si(100)-c(4 $\times$ 2) in Fig. 2, the intrinsic surface states are already quenched at  $\sim 1$  Å V coverage. However, Fig. 4 shows that a distinctive Fermi-Dirac line shape at  $E_F$ , which is characteristic of a metallic overlayer, is not established until  $\sim 4$  Å V coverage; this behavior can also be seen in the low-coverage IDC's in Fig. 3 for the Si(100)-c(4 $\times$ 2) surface. Energy-band formation and metallic character of the overlayer are not expected at least until the local coordination of atoms is well established, i.e., at less than or equal to angstroms of coverage.

As seen in Fig. 4, the V 3d states produce a broad structure which develops a maximum at  $-0.95$  eV first visible at  $\sim 4$  Å coverage. With higher coverage the emission from these states increases considerably while the maximum shifts closer to  $E_F$  toward its position in bulk V metal (seen in Fig. 4). At  $\sim 20$  Å thickness the intensity has reached nearly its final value. However, the final valence-band line shape is not attained until 40–50 Å coverage. V deposition beyond  $\sim 20$  Å induces a strong narrowing of the d band, reducing the measured full width at half maximum (FWHM) to  $\sim 0.8$  eV. An additional peak emerges at  $-2.0$  eV while the shape of the dominant peak suggests a doublet structure involving a weak shoulder near  $-0.7$  eV. The band narrowing is accompanied by a

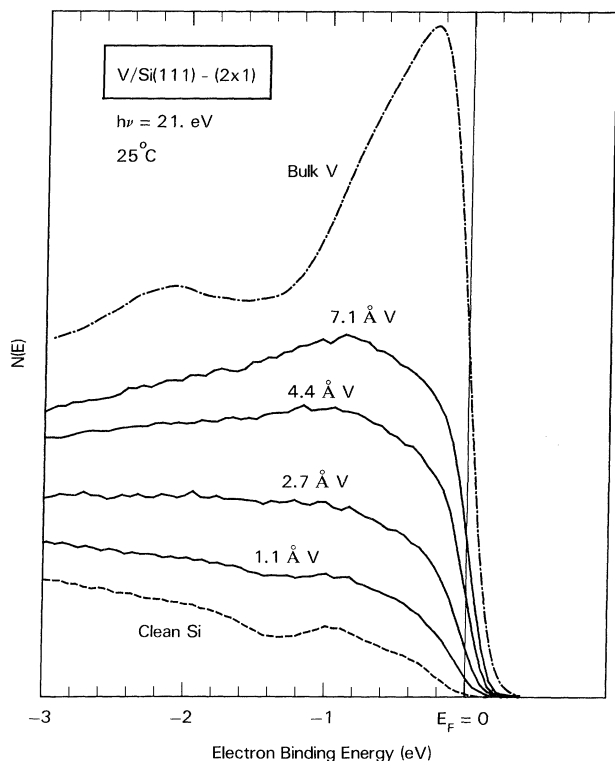


FIG. 4. UPS ( $h\nu=21.2$  eV) valence-band spectra in the vicinity of  $E_F$  for the clean cleaved Si(111)-(2 $\times$ 1) surface and for various V coverages deposited at room temperature.

considerable reduction of the secondary electron emission intensity, perhaps as a result of final-state effects.

At sufficiently high coverage the UPS spectra should reveal the evolution of the bulk V valence-band density of states. Since UPS measurements are not available for single crystal V, our data can only be compared with early UPS work<sup>38</sup> and more recent XPS (Ref. 39) and soft-x-ray emission<sup>40</sup> investigations on evaporated thin films. While the early data show much broader structures, the recent XPS study agrees fairly well with our findings for bulk V, although the peak at  $-2$  eV is much less pronounced in our UPS data.

According to the AES-intensity dependence (Fig. 1) and the UPS incremental difference curves (Fig. 2), at room temperature the V/Si interface remains unreacted, i.e., no motion of V and Si atoms has occurred across the original interface. At first sight, the absence of interfacial reaction upon deposition may be surprising in view of the large heat of formation of the silicide ( $\Delta H \sim 25$  kcal/g-at.), particularly because other transition-metal/Si interfaces with smaller heats of formation do react spontaneously upon deposition (e.g., Cr/Si is known to react<sup>41</sup> but has  $\Delta H \sim 8-11$  kcal/g-at. Thus it appears that the activation-energy barrier to the initial stage of silicide formation at the interface is larger for V than for Cr. This may be considered consistent with the higher activation energies for bulk V, Ti, and Ta silicide growth than for growth of Cr and Mo silicides. Furthermore, the possibility has been suggested<sup>42,43</sup> that the high initial reactivity

of transition-metal/Si interfaces such as Pd/Si, Ni/Si, and Cr/Si may be simply a consequence of the heat released during chemisorption of the metal atom on Si, which could then drive the reaction over the activation-energy barrier; however, the heats of chemisorption are not sufficiently well known to assess this possibility in detail at present.

#### IV. CHEMICAL PROPERTIES OF THE REACTED V/Si INTERFACE

In the process of interfacial reaction which leads to the formation of silicide compounds, atoms must move across the initial metal/Si interface. In the following discussion we use the term "intermixing" to refer generally to motion of atoms across the initial interface (whether this is part of silicide formation or some other process such as diffusion), and we use the word "reacted" to indicate that atoms have already moved across the initial interface.

From thin-film studies it is known that bulk silicide ( $\text{VSi}_2$ ) formation occurs above  $\sim 500^\circ\text{C}$ . This system is one of the few which have shown an initial growth rate which is linear in time, suggesting interface-controlled kinetics; this changes to the usual  $\sqrt{t}$  dependence at larger thickness (suggesting diffusion-controlled kinetics). Since the present studies involve thin layers (up to 200 Å), we may expect to observe those interface reaction steps which also play a role in the initial thin-film growth of  $\text{VSi}_2$  studied previously.

Figure 5 shows UPS spectra for a bulk V overlayer film

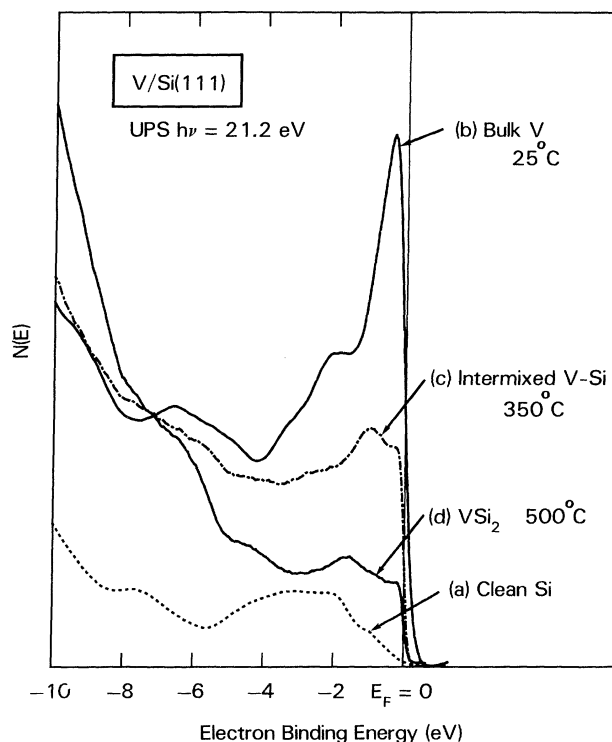


FIG. 5. UPS ( $h\nu=21.2$  eV) valence-band spectra for (a) clean Si(111)-(7 $\times$ 7), (b) unreacted V deposited at room temperature, (c) "intermixed" V-Si (350°C reaction), and (d) fully reacted  $\text{VSi}_2$  compound (500°C reaction).

( $\sim 200$  Å thick) on Si(111)-(7 $\times$ 7) annealed for a given time to successively higher temperatures up to 500°C. Thermal processing at 200°C has little effect on the electronic structure and composition. However, a marked change in the UPS density of states and strong AES composition changes are already observed at 350°C, revealing a high Si content (of order 40 at. %) in the overlayer. The dominant emission just below  $E_F$  is strongly suppressed, while a much smaller peak develops at  $\sim 1.0$  eV and a pronounced metallic Fermi edge remains. At the same time additional transitions emerge in the V AES spectrum.

The sensitivity of the surface-spectroscopy techniques used here and the cleanliness conditions of the interface have enabled us to observe this intermixing reaction at temperatures well below those normally used for compound formation. This low-temperature intermixing involves a marked change in composition several hundred angstroms from the initial V/Si interface. Further experiments to evaluate the significance and possible implications of this low-temperature reactivity at the V/Si interface are described in Sec. V.

Upon annealing to relatively high temperatures typical of those normally employed for bulk silicide formation by contact reaction, the UPS spectrum changes markedly. As seen in Fig. 5, a brief ( $\sim 3$ -min) anneal at 500°C produces much lower overall intensity and an emission peak at  $-1.6$  eV, with additional features at  $-4.0$ ,  $-6.0$ , and  $-7.5$  eV. This spectrum is then stable with annealing to  $\sim 600$ °C. It agrees well with that of bulk polycrystalline  $\text{VSi}_2$  fractured *in situ*.<sup>44</sup> At this point the relative AES intensities indicate a composition very close to  $\text{VSi}_2$ .

Corresponding UPS results for annealing of a V film ( $\sim 200$  Å thick) on the Si(100)-c(4 $\times$ 2) surface are shown in Fig. 6. These results are fairly similar to those for Si(111)-(7 $\times$ 7). However, the spectra for intermediate-temperature annealing (350°C) differ considerably since the state of the intermixed material formed at lower temperatures is less well defined than that of the bulk-silicide reaction product.

The V AES spectra for V/Si(111)-(7 $\times$ 7) are shown in Fig. 7 for thin (2-Å) and thick (51-Å) V depositions at room temperature as well as for annealing of a 65-Å layer at various temperatures. These spectra show a satellite feature (indicated by arrows)  $\sim 18$  eV below the main  $L_{2,3}M_{2,3}V$  and  $L_{2,3}VV$  lines in V/Si layers reacted at 350°C and above. The existence of this satellite seems to reflect the presence of Si atoms in a local V-atom environment. This feature is also seen in the unreacted case (25°C) for thin layers, because the V atoms are very close to the Si atoms on the other side of the abrupt interface.

After reaction on V overlayers on Si(111)-(7 $\times$ 7) at  $\geq 500$ °C and subsequent removal from the UHV chamber, TEM studies identified the  $\text{VSi}_2$  lattice structure, as shown in Fig. 8(b). The  $\text{VSi}_2$  grains [Fig. 8(a)] have an average diameter of a few hundred angstroms. They are randomly oriented since no texture is observed along the respective diffraction rings. A small contribution of unreacted V metal is still present. As expected, the silicide ( $\text{VSi}_2$ ) formation observed at  $\sim 500$ °C under standard thin-film processing conditions<sup>32</sup> is also found in the

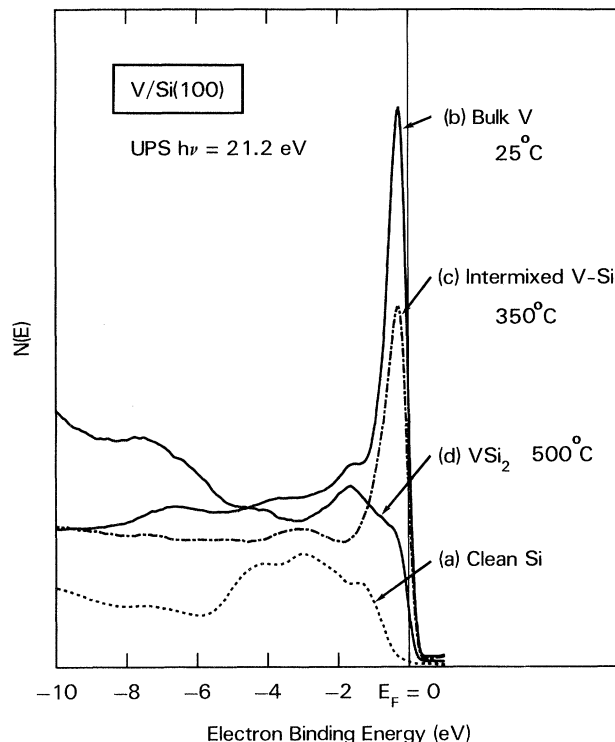


FIG. 6. UPS ( $h\nu=21.2$  eV) valence-band spectra for (a) clean Si(100)-c(4 $\times$ 2), (b) unreacted V deposited at room temperature, (c) "intermixed" V-Si (350°C reaction), and (d) fully reacted  $\text{VSi}_2$  compound (500°C reaction).

present investigations of the atomically clean V/Si interface. The  $\text{VSi}_2$  compound has been indicated by AES composition analysis and by its characteristic valence electronic structure as revealed in UPS. Its lattice structure has been confirmed by TEM analysis; these results show that only one compound phase,  $\text{VSi}_2$ , is formed under clean, ordered UHV conditions, while the diffraction rings indicate polycrystalline  $\text{VSi}_2$  grain sizes of several hundred angstroms.

The observation of a V/Si interfacial reaction (atomic mixing across the initial interface) at temperatures well below those usually employed for silicide formation is not surprising since other transition metals (the near-noble metals Pd, Pt, and Ni) also show a low-temperature reaction. What is surprising for the V/Si interface is that this low-temperature reaction proceeds through much thicker layers (several hundred angstroms thick).

#### V. V-Si INTERMIXING AT INTERMEDIATE TEMPERATURES

To better understand the nature of the low-temperature reactivity (i.e., at  $\sim 350$ °C), several different experiments were carried out. As indicated by the example in Fig. 5(c), this annealing produced spectra which were quite notably different from those for  $\text{VSi}_2$  and pure V metal for all initial V thicknesses from a few angstroms to 75 Å on both Si(111) and Si(100) surfaces. From TEM studies as well as from the Auger composition analysis, we can rule out the possibility that this stage is  $\text{V}_3\text{Si}$ . The low-

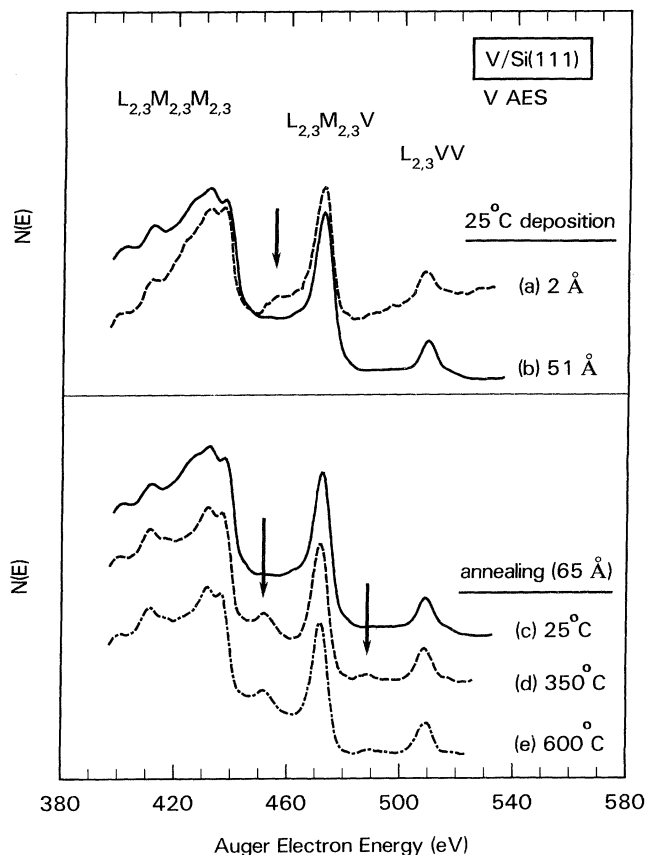


FIG. 7. V AES spectra for (a) thin and (b) thicker unreacted V overlayers at room temperature on Si(111)-(7×7) and for a 65-Å overlayer (c) at room temperature, (d) annealed at 350°C, and (e) annealed at 600°C (3 min each). Arrows indicate the satellites (~18 eV below main spectral features) which appear to reflect Si atoms in the local V-atom environment.

temperature reactivity is not dependent on the growth details either: Rather similar spectra appeared for both sequential 350°C annealing treatments of a thick V film and for sequential deposition steps on a heated (350°C) Si substrate.

Further information about the low-temperature reaction has been obtained from the following Auger analysis. A 75-Å-thick V film was deposited on the automatically clean Si(111)-(7×7) surface, essentially quenching the Auger signals from the Si substrate. The sample was then annealed at three different temperatures to promote an interfacial reaction. UPS and AES spectra were taken after each annealing step. Figure 9 shows the resulting relative intensity of the Si  $L_{2,3}VV$  and  $KLL$  and the V  $L_{2,3}M_{2,3}V$  Auger lines, which have been normalized to the clean Si or thick V intensities. These Auger intensities provide an approximate indication of the composition in the film averaged over the probing depth (electron escape depth) of each Auger transition separately. Since the Si  $KLL$  spectrum has an escape depth more than twice that of the other two Auger transitions, comparison of the relative intensities for the  $KLL$  with those for the  $L_{2,3}VV$  and  $L_{2,3}M_{2,3}V$  lines gives a useful measure of the depth uni-

formity of the overlayer. Annealing at 300°C for 20 min already induces strong material exchange across the initially abrupt interface and through the entire overlayer thickness. Further processing at 350°C for 30 min increases the Si overlayer content slightly to ~50 at. % and produces a UPS spectrum typical of the intermediate phase [Fig. 5(c)]; in both cases the three Auger intensities agree fairly well, showing that the depth distribution of the overlayer is reasonably homogeneous at least within the top 30–40 Å.

However, upon an extended (12-h) anneal at 350°C, the overall overlayer stoichiometry changes further. The  $L_{2,3}VV$  and  $L_{2,3}M_{2,3}V$  transitions then indicate a  $VSi_2$  composition, which is confirmed by the corresponding UPS spectrum. In contrast, the Si  $KLL$  intensity indicates a much higher Si content. Since the Si  $KLL$  spectrum samples a region (~20 Å) more than twice as deep as the Si  $L_{2,3}VV$  and V  $L_{2,3}M_{2,3}V$  spectra sample (~7–8 Å), this might suggest that the approximate  $VSi_2$  composition is restricted to a region ~10 Å thick near the surface, while the material below it (the next 10–15 Å) has a more Si-rich composition. This might be taken as evidence that some of the initial V has diffused into the Si substrate during the long anneal at 350°C. Such an inference would be quite surprising, and further experiments are required to clarify this issue.

For a reasonably thick (~100 Å) V overlayer the intermixing is observed at the top surface rather quickly, but gradual changes continue for much longer times and for small changes in temperature, as seen in Fig. 9. This slow change in the surface composition is in contrast to the rapid transformation of the surface upon formation of a bulk silicide compound which consumes the metal overlayer, such as seen for  $Pd_2Si$  growth.<sup>21</sup> It seems, therefore, that the reaction at 350°C is not a typical interfacial reaction process in which a well-defined silicide interlayer of essentially uniform composition grows in thickness until the unreacted metal is consumed. Instead, the reaction appears more complex in character.

TEM phase analysis gives further information on the nature of the material formed by a low-temperature reaction. Figure 10(a) shows the diffraction pattern for the intermixed layer produced by a short anneal at intermediate temperature (350°C for 20 min), while Fig. 10(b) shows that for fully reacted  $VSi_2$  obtained by a brief anneal at high temperature (550°C for 5 min). Both patterns look surprisingly similar despite the marked difference seen in both UPS and AES. Ring structures revealing  $VSi_2$  formation are clearly visible in both cases, with a slight texturing for Fig. 10(a). In addition, all samples show some rings from unreacted V and other weak unidentifiable rings, but there is no structure specific to the material reacted at low temperature which would indicate the presence of a new phase. The overlayer contains a mixture of reacted  $VSi_2$  grains in a matrix of unreacted V. Such an intermixed layer would be consistent with the spectroscopy results described above.

In addition to the normal Si diffraction spots, unexpected extra reflections corresponding to  $Si \frac{1}{3}(422)$  are observed. The most significant difference between the two diffraction patterns in Fig. 10 is the much higher intensity



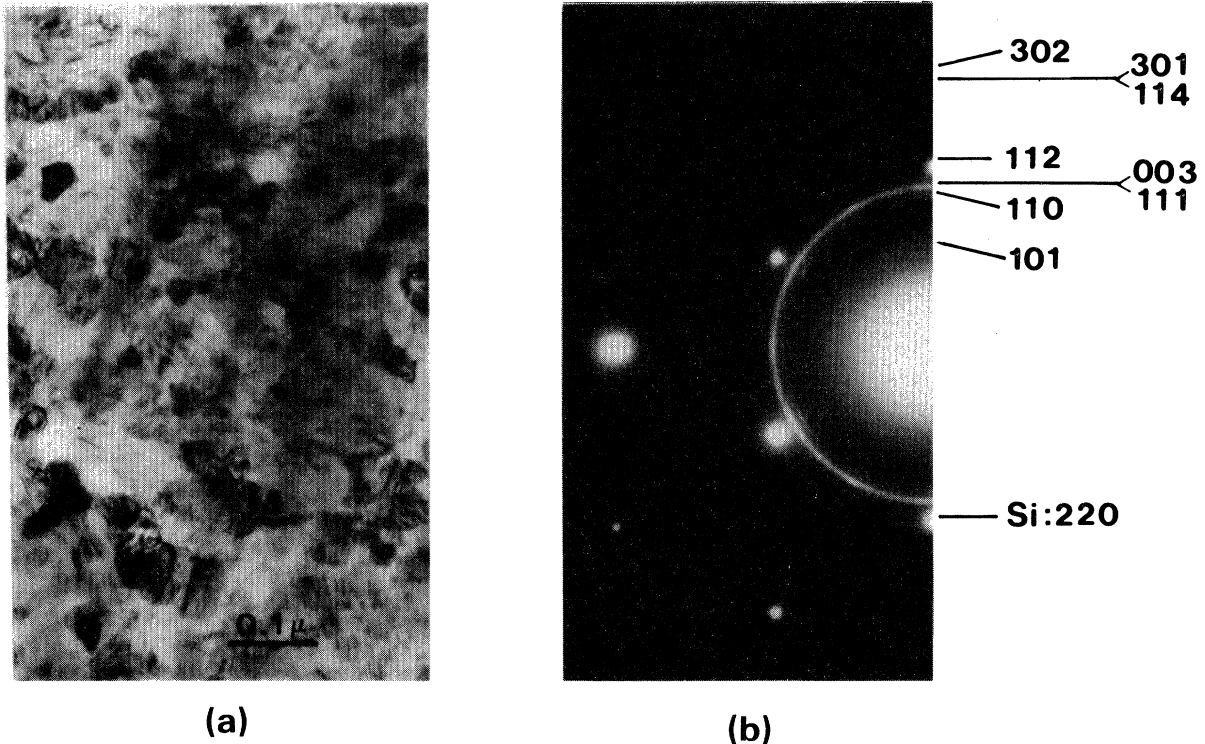


FIG. 8. (a) TEM micrograph of a thick V film reacted to  $\text{VSi}_2$  at  $550^\circ\text{C}$ . (b) Diffraction pattern indexed for  $\text{VSi}_2$ .

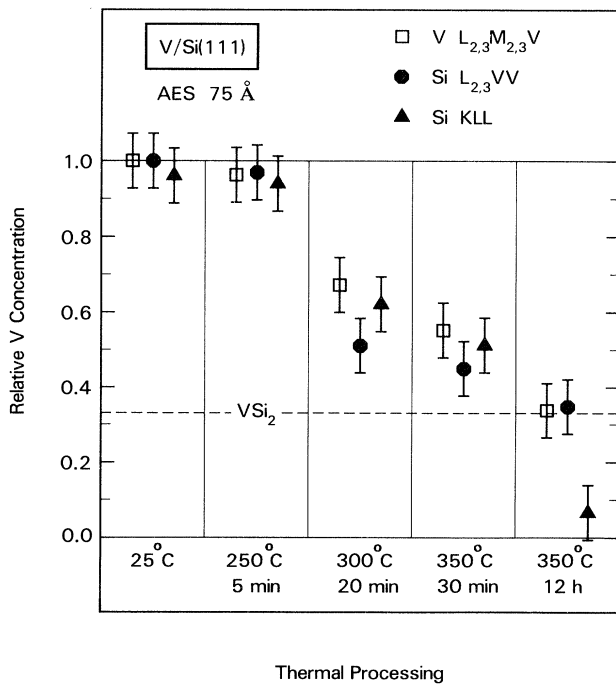


FIG. 9. AES intensity behavior of  $\text{Si } L_{2,3}VV$  and  $KLL$  and  $\text{V } L_{2,3}M_{2,3}$  transition for a 75-Å overlayer thermally processed at different temperatures.

of these extra reflections for the sample with the intermixed overlayer [Fig. 10(a)]. With a prolonged (12-hr) anneal at  $350^\circ\text{C}$ , the extra reflections have an intensity level between that shown in Figs. 10(a) and 10(b).

These reflections are unexpected because they do not belong to the bulk-Si lattice. To explain their presence, we need to invoke the existence of some extraneous material at the interface. Because of the exact positioning of the reflections at  $\frac{1}{3}(422)$ , these material layers must have a pseudomorphic relationship with the underlying Si bulk and a structure very similar to that of bulk Si (e.g., diamond cubic or hcp type.)

In principle, the presence of the extra reflections might be explained by two other alternatives, but neither of these appears likely. Firstly, the extra reflections could appear if the  $\text{Si}(111)$  substrate is composed of  $3n \pm 1$  atomic layers, where  $n$  is an integer and a layer is meant to be, e.g.,  $Aa$ , as in the  $\text{Si}(111)$  plane stacking sequence  $AaBbCc \dots$ . This possibility can be ruled out because TEM examinations of virgin  $\text{Si}(111)$  foils have revealed no such extra reflections. Secondly, twins in the Si bulk could produce the extra reflections, and such twinning of the top Si substrate layers might conceivably be caused by the ion-bombardment and annealing processes used to produce the initial clean, ordered Si surface. However, this possibility can also be eliminated because high-resolution LEED observations<sup>45</sup> have found no indication of twinning after such procedures.

This leaves only one reasonable explanation for the ex-



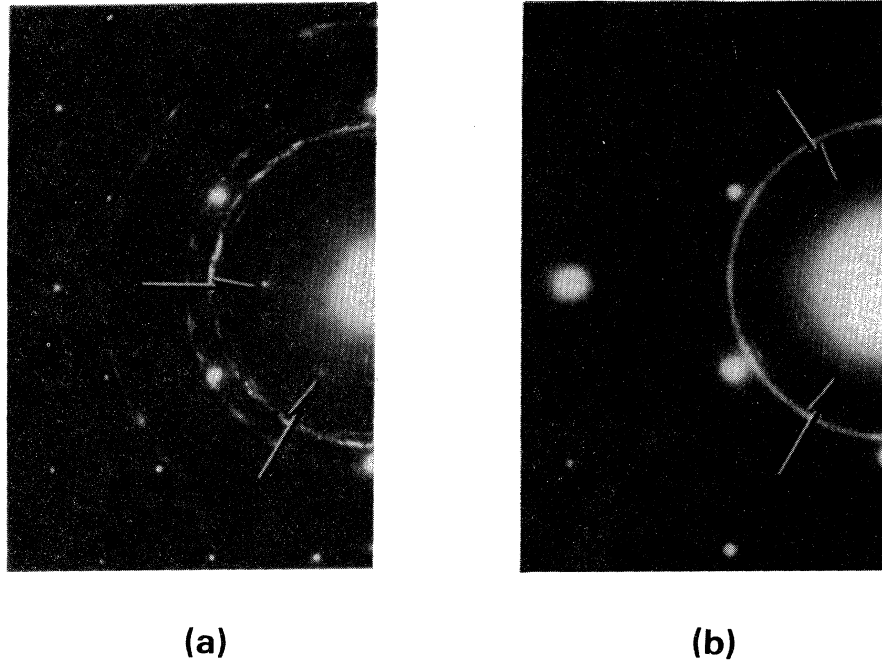


FIG. 10. TEM diffraction patterns for (a) "intermixed" V:Si (reacted at 350°C) and (b) fully reacted  $\text{VSi}_2$  overlayers (reacted at 550°C). Arrows indicate some of the extra reflections.

tra reflections—namely, the existence of a few layers of extraneous material having a Si-type structure and a pseudomorphic relationship with the Si substrate. The simplest way this extraneous material might arise is by periodic replacement of some Si atoms in these few layers by vacancies or V atoms, either of which could result from the motion of atoms during reaction.

## VI. CORRELATION OF SCHOTTKY-BARRIER FORMATION AND INTERFACIAL REACTION

The behavior of the V/Si Schottky-barrier height shows important correlations to the reaction state at the interface. As described previously,<sup>31,46</sup> the changes in the Si(111) Schottky-barrier height  $\phi_{bn}$  with V deposition and annealing have been investigated in the initial stages of interface formation [(0–10)-Å metal coverage]. These studies were carried out using high-resolution synchrotron-radiation-photoemission measurements of the Si(2p) core levels to detect changes in interface band bending and thus changes in  $\phi_{bn}$ ; with Si(2p) core levels  $\sim 300$  meV wide (FWHM), changes in  $\phi_{bn}$  of  $\sim 10$  meV are detectable.

A summary of these results is shown in Fig. 11, in which the Si(2p) binding energies are referenced to a Schottky-barrier height of 0.79 eV for the cleaved Si(111)-(2×1) surface.<sup>47–51</sup> The clean Si(111) surface shows a fairly strong dependence of  $\phi_{bn}$  on surface reconstruction, with a variation of  $\sim 180$  meV between the barrier heights on the cleaved Si(111)-(2×1) surface and on the sputter-cleaned Si(111)-(7×7) surface; in addition,  $\phi_{bn}$  varies over a range of  $\sim 100$  meV depending on the step density of the specific cleave.

In spite of these variations, deposition of only  $\sim 1\text{--}2$  Å V metal brings  $\phi_{bn}$  to essentially the same value, which is dependent of the initial clean-surface atomic structure. With increasing coverage or mild ( $\sim 200^\circ\text{C}$ ) annealing,  $\phi_{bn}$  rises slightly; since the spectroscopy measurements

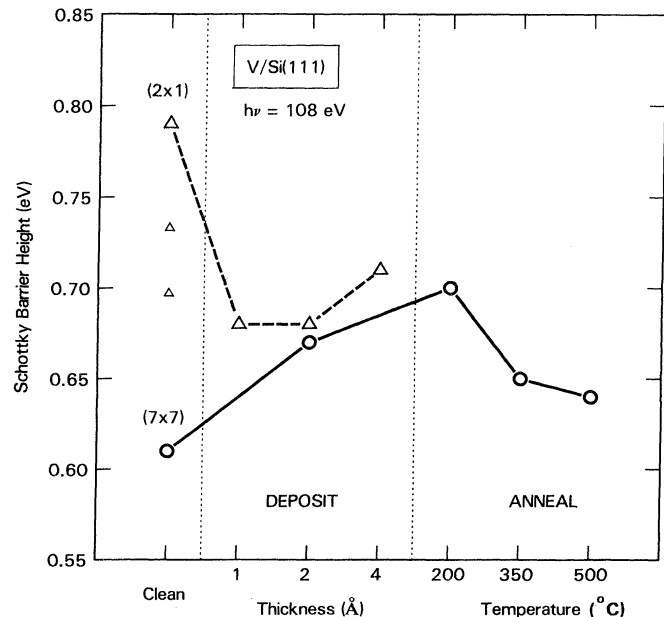


FIG. 11. Schottky-barrier height  $\phi_{bn}$  ( $n$ -type barrier) for the as-deposited and reacted V/Si(11) interface as determined from synchrotron-radiation-photoemission studies of core-level band-bending shifts.

described previously show that no reaction occurs in these cases, the attendant changes in  $\phi_{bn}$  are attributed to changes in metal-overlayer morphology or to a rather mobile interface condition.

A dramatic change in the behavior of  $\phi_{bn}$  is observed upon interfacial reaction. With 350°C annealing to promote atomic mixing of Si and V atoms across the interface, the increasing  $\phi_{bn}$  suddenly decreases, essentially to the value found for the fully reacted (500°C) VSi<sub>2</sub>/Si interface; this value agrees very well with recent findings for bulk VSi<sub>2</sub>/Si interfaces of  $\phi_{bn}=0.64$  eV.<sup>52</sup> This demonstrates clearly that different mechanisms or different chemical bonds control the barrier height for the reacted versus the unreacted V/Si contacts. Furthermore, the lower-temperature intermixing process appears to already provide the Fermi-level pinning mechanism responsible for  $\phi_{bn}$  at the VSi<sub>2</sub>/Si interface. Thus the correlation of Schottky-barrier formation and interfacial reaction is displayed very clearly.

These observations of Schottky-barrier behavior have implications for current models of the Schottky-barrier height, at least as applied to the V/Si or perhaps the refractory-transition-metal/Si interface system. Since (~1–2)-Å metal deposition shifts  $\phi_{bn}$  to a value which is independent of initial clean-surface reconstruction, corresponding intrinsic surface electronic states are unimportant to  $\phi_{bn}$ . Instead, the barrier height of the unreacted V/Si interface appears to be a consequence of the basic chemical bonds between V and Si atoms at the interface.

For the case of the reacted V/Si interface, a different Fermi-level pinning mechanism must be operative, since the behavior of  $\phi_{bn}$  changes markedly when interfacial reaction occurs. Since  $\phi_{bn}$  is nearly the same for reaction at lower temperature as for the usual VSi<sub>2</sub> formation by contact reaction at higher temperature, the Schottky barrier seems to be unaffected by the detailed nature of reacted V–Si bonds or by the microstructure of the reacted material and the interface.

Again the role of the basic chemical bonds between V and Si atoms may be the dominant feature in Schottky-barrier formation, but here the character of these bonds—for the reacted interface—is quite different than for the unreacted interface. Alternatively, defects in the interfacial region could be crucial in determining the barrier height.

## VII. CONCLUSIONS

These investigations give important new information about the chemical behavior and Schottky-barrier formation at a refractory-transition-metal/Si interface. They also demonstrate similarities and contrasts with near-noble transition-metal Si interfaces (Pd, Pt, and Ni). The main conclusions can be summarized as follows.

(1) Under atomically clean conditions the V/Si interface remains unreacted at room temperature, i.e., no significant mixing of atoms across the interface occurs. Instead, the

V–Si bonds are more like a simple chemisorption state, which is stable to 200°C.

(2) With annealing to high temperatures, ~500°C as normally required for this film silicide formation, reaction occurs at the clean V/Si interface and produces single-phase VSi<sub>2</sub> (as expected) with its corresponding lattice structure (observed by TEM) and electronic structure (revealed by UPS).

(3) As in the case of the near-noble metals, reaction begins at the V/Si interface for temperatures well below the normal silicide-formation temperature. For the V/Si case this is observed at 350°C, while for the near-noble metals it occurs at less than 25°C.

(4) The low-temperature reactivity of the V/Si interface is somewhat more complex than that for the near-noble transition-metal/Si interfaces. It extends over a considerably larger distance from the interface (several hundred angstroms; cf. ~10 Å) and involves a more complicated microstructure with VSi<sub>2</sub> grains embedded in a background of V metal.

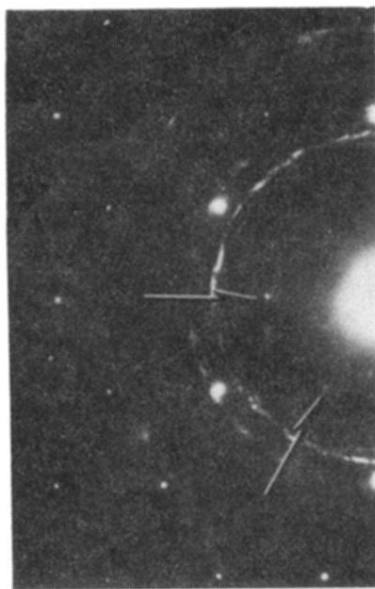
(5) The Schottky-barrier height of the unreacted V/Si contact appears to be determined simply by the basic bonding between V and Si atoms. Upon interfacial reaction, the barrier height becomes controlled by a fundamentally different mechanism (different interface chemical bonds or other consequences of the reactivity) which dominates the Schottky-barrier properties for contacts reacted at either low temperatures (350°C) or at usual silicide-formation temperatures ( $\geq 500^\circ\text{C}$ ).

By using highly sensitive surface-spectroscopy techniques and atomically clean, ordered Si surfaces and interfaces, these experiments have provided new microscopic information about the reactivity and properties of the V/Si interface. In addition, the value of these studies has been enhanced by combining different techniques together, including surface-spectroscopy techniques (for electronic structure, composition, and reactivity), TEM studies (for interface microstructure and lattice phase), and Schottky-barrier-height measurements (for electrical characterization). This combined approach seems essential to effectively address the underlying issues of interface chemical behavior and Schottky-barrier properties. In the case of the low-temperature reactivity, for example, the UPS and AES results alone would have led to incorrect conclusions if no structural information were available, and clearly no conclusion about Fermi-level pinning could have been drawn without correlations between measured interface chemical properties and corresponding Schottky-barrier heights.

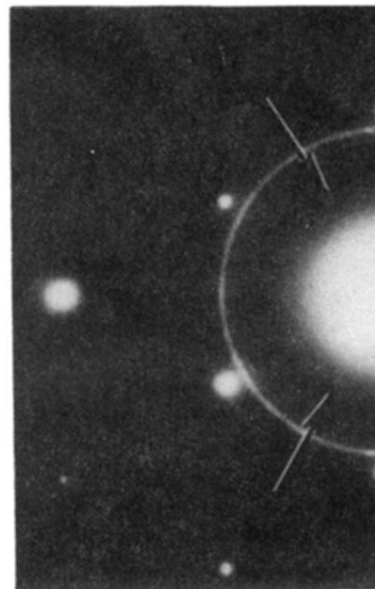
## ACKNOWLEDGMENTS

We appreciate valuable discussions with P. S. Ho and R. J. Purtell. This work was supported in part by the U.S. Office of Naval Research.

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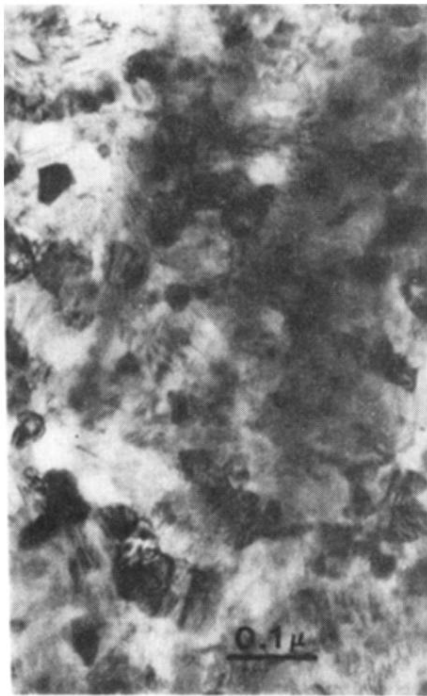


**(a)**

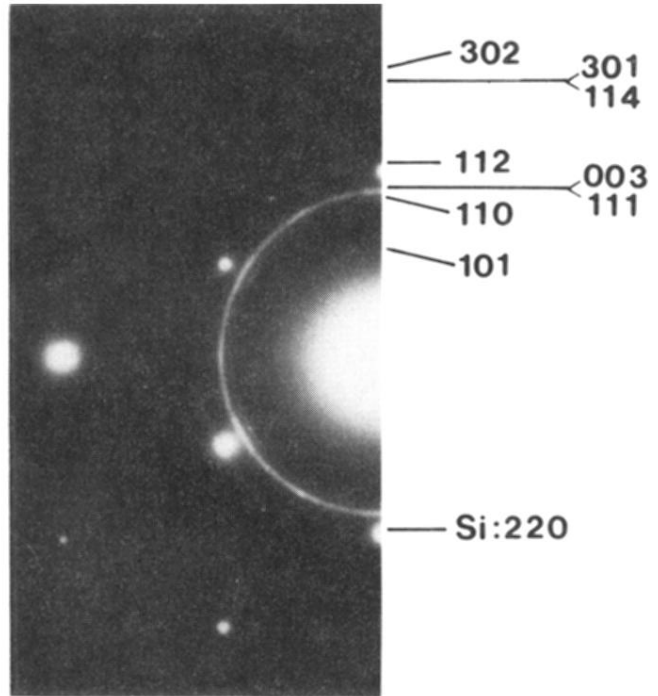


**(b)**

**FIG. 10.** TEM diffraction patterns for (a) "intermixed" V:Si (reacted at 350°C) and (b) fully reacted VSi<sub>2</sub> overlayers (reacted at 550°C). Arrows indicate some of the extra reflections.



(a)



(b)

FIG. 8. (a) TEM micrograph of a thick V film reacted to  $\text{VSi}_2$  at  $550^\circ\text{C}$ . (b) Diffraction pattern indexed for  $\text{VSi}_2$ .