

## Barrier heights and silicide formation for Ni, Pd, and Pt on silicon

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Deposited Ni, Pd, and Pt films on *n*-type Si have been annealed up to 700 °C. Silicide formation was monitored by MeV <sup>4</sup>He Rutherford backscattering and glancing-angle x-ray diffraction. Barrier-height measurements were performed mainly using forward *I-V* characteristics. The values of the barrier heights are 0.66 eV for Ni<sub>2</sub>Si and NiSi, 0.75 eV for Pd<sub>2</sub>Si; 0.85 eV for Pt<sub>2</sub>Si, and 0.87 to 0.88 eV for PtSi. The barrier heights depend primarily on the metal deposited and not on the particular silicide phase.

### I. INTRODUCTION

In 1874 an asymmetric electrical conduction was observed across a metal-semiconductor couple.<sup>1</sup> Only seventy years later, in 1939, an interpretation of the rectifying behavior of such contacts was given by Schottky<sup>2</sup> and Mott<sup>3</sup>; the concept of Mott was that the rectifying barrier was due to the difference in the work function of the metal and the electron affinity of the semiconductor. Schottky introduced the space-charge-region concept. Since this time and because of the many applications of Schottky-barrier diodes in semiconductor devices, a large amount of experimental data has been collected.<sup>4,5</sup> It was observed that the Schottky model does not account for all of the data and new theories which have been developed that focus on the electronic structure of the metal-semiconductor interface with the common assumption of an ordered and abrupt junction. Recent studies have suggested that the junction is not abrupt but graded in composition with a 10–20 Å thick interfacial layer.<sup>6–8</sup> This situation applies to a reactive interface and, in particular, to the silicides formed by the near-noble metals Ni, Pd, and Pt.

In order to develop a consistent theory it is necessary to establish the relevant parameters affecting the barrier height. One approach to identify the parameters is the comparison of the barrier height of silicides produced by metals lying in the same column or line of the periodic table.<sup>9</sup> Another approach identifies the heat of formation as the main parameter governing barrier heights<sup>10</sup>; as a consequence, in most cases different phases of the same metal should produce a different barrier height. Yet another approach is the comparison of the barrier heights produced by different silicide phases of the same metal. All these comparisons depend on the reliability of the experimental data, a reliability which is not

well established. In the literature, a large spread in values for barrier heights can be found for the same metallization. For Au contacts to *n*-type silicon, the accepted value for the barrier height,  $\phi_B$ , is 0.81 eV (Refs. 4 and 11); however, data ranging from 0.81 to 0.5 eV can easily be found.<sup>12</sup> Most of this confusion is generated by the lack of detailed metallurgical characterization of the systems investigated. The availability of sophisticated analytical techniques has led to a better control of the structure and to an improvement in the consistency of the experimental measurements.

The near-noble-metal silicides are attractive in that more than one phase can be formed, and the heats of formation differ between the phases. In contrast, the refractory metals on silicon form only one phase. The near-noble-metal silicides form at low temperatures (100 to 400 °C) compared to those (500 to 700 °C) required for refractory metals.<sup>13–15</sup> In addition, problems with interface contamination are not as severe with the near-noble-metal silicides, where metal atoms are the main diffusing species in the growth of the first phase; with the refractory metals silicon is the diffusing species. For Ni and Pt, the second phase, the monosilicide, does not form until all the metal is consumed in forming the first phase. Consequently, structures can be consistently formed with either the first or second phase next to the silicon. The purpose of this paper is to measure the Schottky barrier height when different phases are formed and to correlate these values with the phase identification and spatial localization provided by x-ray diffraction and Rutherford backscattering measurements on the same sample.

### II. EXPERIMENTAL PROCEDURE

The samples were prepared by depositing 1000–2000-Å metal layers on 5–10 Ω cm, 300-microme-

ters-thick, *n*-type Si wafers. For Pd and Pt(111) oriented and for Ni(100) oriented wafers were used. The formation of Ni<sub>2</sub>Si is strongly dependent on substrate orientation with the growth about four times faster on (100) as compared to Si(111) oriented.<sup>13</sup> The *e*-gun depositions were performed in a vacuum of 10<sup>-7</sup> Torr at a rate of 10–30 Å/sec. Buffered HF was used to clean the wafers before they were loaded in the deposition chamber.

During the same deposition, three types of samples were made: bare Si samples for x-ray and Rutherford backscattering spectrometry (RBS) analysis, SiO<sub>2</sub> covered and patterned Si samples for *I*-*V* characteristics, and bare Si samples held under a metal mask with openings of 2-mm diameter. For the *I*-*V* measurements the depositions were also made through a metal mask having 2-mm-diameter openings but the active area of the diodes was defined by oxide windows with diameters of 25, 100, 225, and 400 micrometers. The samples were processed together and annealed in a furnace with flowing, purified helium.

The reaction kinetics and the phase sequence in compound formation were measured using MeV <sup>4</sup>He Rutherford backscattering spectrometry, with a 20-keV energy resolution. Positive phase identification was made by Seeman-Bohlin glancing-angle x-ray diffraction measurements.

Barrier-height values were determined by extrapolating the forward *I*-*V* characteristics to zero applied voltage. The extrapolation was made by a linear fit over three orders of magnitude or greater of current on the semilog *I*-*V* characteristics. The measurements were made on all four diode areas. The same value was found in all diodes processed at temperatures less than 500 °C. The deviation from ideal diode behavior is given by the ideality factor  $n = (q/kT) (dV/d \ln I)$ . In all diodes except those processed at temperatures higher than 600 °C, the values of *n* were less than 1.1. An anomalously high reverse current was observed in diodes with ideality factors greater than 1.1. Barrier heights were determined from reverse bias *C*-*V* measurements in some cases for each metal from extrapolation of the linear portion of the 1/*C*<sup>2</sup> vs *V* data to the intercept on the voltage axis. The measurements were used as a cross check on the *I*-*V* measurements. Owing to the low impurity concentration in the samples the magnitude of the correction to the measured barrier height was 0.2 to 0.3 V for *C*-*V* measurements and less than 0.05 V for *I*-*V* measurements. In fact, for the Pt-Si sample annealed at 300 °C for 120 min, the *I*-*V* measurements given an intercept value of 0.84 eV and a correction factor for the image force effect of 0.01 eV giving a value for the barrier height of 0.85 eV. For the same sample, *C*-*V*

measurements give an intercept value of 0.59 eV and the total correction factor is now 0.25 eV giving a barrier-height value of 0.84 eV. Four-point probe measurements were made to evaluate the sheet resistivity of the various compounds. Resistivity values were obtained using the thickness data from RBS measurements. All electrical measurements were made with the samples held at room temperature.

### III. EXPERIMENTAL RESULTS

#### A. Platinum-Si(111) system

The low-temperature reaction of Pt with Si is shown in Fig. 1 by the growth at 265 °C of a 600-Å-thick Pt<sub>2</sub>Si layer interposed between Si and unreacted Pt. Further annealing produces an increase in the thickness of Pt<sub>2</sub>Si. The growth kinetics measured at 265 °C are in substantial agreement with those reported for Pt deposited at 10<sup>-7</sup> Torr.<sup>16</sup> When all the Pt is consumed, PtSi starts to form at the Si-Pt<sub>2</sub>Si interface.<sup>17</sup> At 300 °C, a 1200 Å layer of PtSi is formed and all the Pt<sub>2</sub>Si is consumed after the sample is annealed at 400 °C. X-ray diffraction data for these samples is shown in Fig. 2. The indexed peaks refer to Pt in the upper, Pt<sub>2</sub>Si in the next, and PtSi in the bottom segment of the figure. The phases correspond to those in RBS spectra shown in Fig. 1.

Barrier-height measurements are shown in Fig. 3 for as-deposited and annealed samples. The phase identification refers to the phase, Pt<sub>2</sub>Si or PtSi, that is next to Si as determined by backscat-

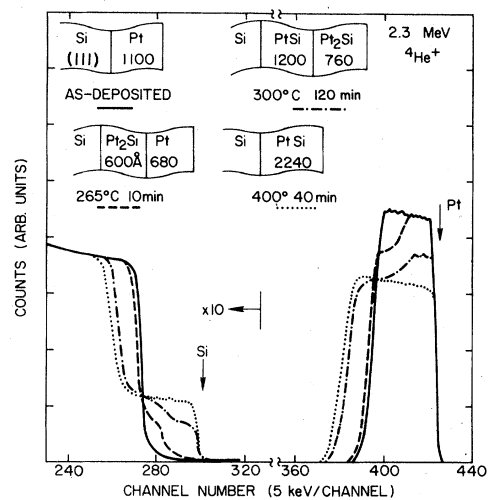


FIG. 1. Backscattering spectra showing the sequential reactions between a Pt film of 1100 Å and Si(100): (a) as-deposited, (b) forming Pt<sub>2</sub>Si after 265 °C for 10 min, (c) forming both Pt<sub>2</sub>Si and PtSi after 300 °C for 2 h, and (d) a complete formation of PtSi after 400 °C for 40 min.

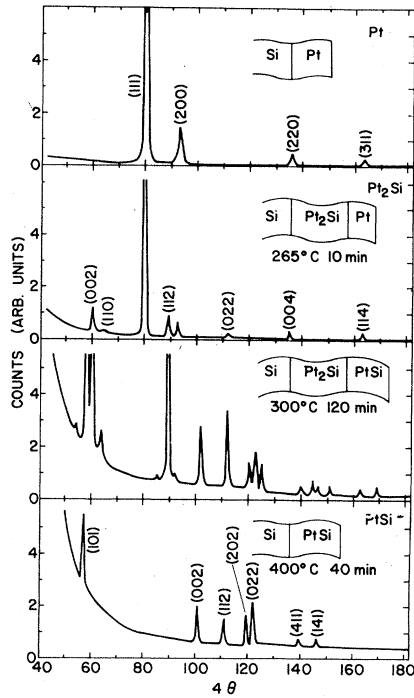


FIG. 2. X-ray diffraction spectra of samples analyzed by backscattering as shown in samples shown in Fig. 1.

tering measurements similar to those in Fig. 1. In the bottom part of the figure the measured ideality factors are shown.

The barrier-height values for the as-deposited samples are grouped around 0.84 eV and those for Pt<sub>2</sub>Si around 0.85 eV. When the second phase PtSi is formed the barrier height increases by 0.02 to 0.03 eV. There is a systematic decrease in the barrier height and increase in the value of the ideality factor at increased processing temperatures.

The resistivity of Pt<sub>2</sub>Si (labeled M<sub>2</sub>Si) and PtSi (MSi) is given in Table I along with the values for Ni and Pd silicides. For all three metals, the re-

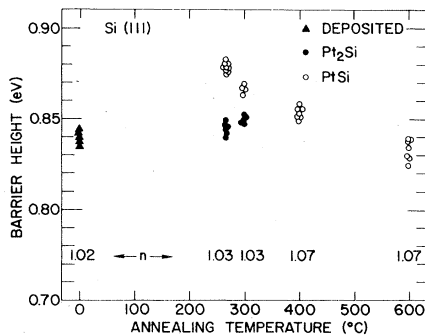


FIG. 3. Schottky barrier height of Pt, Pt<sub>2</sub>Si, and PtSi diodes with the same annealings used in Fig. 1.

TABLE I. Resistivity and barrier heights of silicide layers on *n*-type Si(Pd,Pt)(111) and Si(Ni)(100).

Compound	Resistivity ( $\mu\Omega$ cm)	Barrier height <sup>a</sup> (eV)
Pt		0.84
PtSi	30	0.85
Pt <sub>2</sub> Si	35-40	0.87-0.88
Pd		0.75
Pd <sub>2</sub> Si	30-40	0.75
PdSi	20	
Ni		0.66
Ni <sub>2</sub> Si	25	0.66
NiSi	14	0.66
NiSi <sub>2</sub>	40	

<sup>a</sup>Work function of the metals are 5.4, 4.8, and 4.5 eV to Pt, Pd, and Ni, respectively.

sistivity increases with an increase of the relative Si concentration in the silicide.

#### B. Nickel-Si(100) system

The low-temperature reaction of Ni with Si is shown in Fig. 4 by the growth at 300 °C of a 1100 Å thick Ni<sub>2</sub>Si film interposed between Si and unreacted Ni. Further annealing produces an increase in the thickness of Ni<sub>2</sub>Si. The growth kinetics measured at 300 °C are in substantial agreement with those reported in the literature for Si(100) oriented. At 350 °C for 20 min, all the Ni is consumed and NiSi can form at the Si-Ni<sub>2</sub>Si interface after

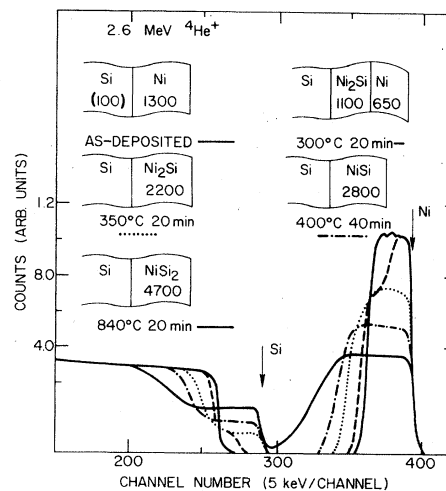


FIG. 4. Backscattering spectra of a 1300-Å Ni on Si(100) at various stages of reaction: (a) as-deposited, (b) forming Ni<sub>2</sub>Si after 300 °C for 20 min, (c) a completion of Ni<sub>2</sub>Si formation after 350 °C for 20 min, (d) a completion of NiSi formation after 400 °C for 40 min, and (e) a completion of NiSi<sub>2</sub> formation after 840 °C for 20 min.

longer annealing times. At 400 °C for 40 min, all Ni<sub>2</sub>Si is converted to NiSi. The system is stable up to 800 °C. At 840 °C for 20 min, 4700 Å of NiSi<sub>2</sub> is formed. The deep trailing edge of the Ni signal in the spectrum is indicative of the nonuniform nature of the NiSi<sub>2</sub>/Si interface.<sup>18</sup> X-ray diffraction data for these samples is shown in Fig. 5. The indexed peaks refer to Ni, Ni<sub>2</sub>Si, and NiSi, and NiSi<sub>2</sub> in the four segments (Fig. 5). The presence of only one diffraction peak for NiSi<sub>2</sub> is an indication of the epitaxial nature of the disilicide phase.

The values of the barrier height cluster around 0.66 eV for as-deposited Ni layers and for samples heat treated at temperatures up to 450 °C (Fig. 6). The ideality factor is 1.03 for these diodes. At higher processing temperatures there is a decrease in the measured barrier height, an increase in the ideality factor, and a strong degradation in the reverse *I-V* characteristics. Moreover, the reverse current is proportional to the square root of the voltage suggesting the presence of deep levels in the Si substrate. In these samples it was not possible to obtain reliable values for the last phase, NiSi<sub>2</sub>, which required even higher processing temperatures.

### C. Palladium-Si(111) system

The reaction of Pd with Si is characterized by the formation of Pd<sub>2</sub>Si at low temperatures and a wide temperature interval, where the Pd<sub>2</sub>Si phase is stable in contact with Si(111) (Fig. 7). At a temperature of 840 °C a uniform PdSi is formed.

The phase Pd<sub>2</sub>Si forms epitaxially on Si(111) as

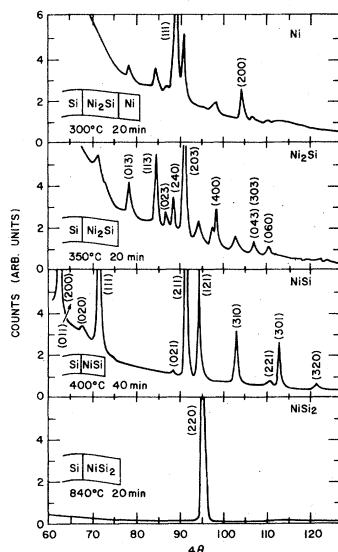


FIG. 5. X-ray diffraction spectra of samples analyzed by backscattering as shown in Fig. 4.

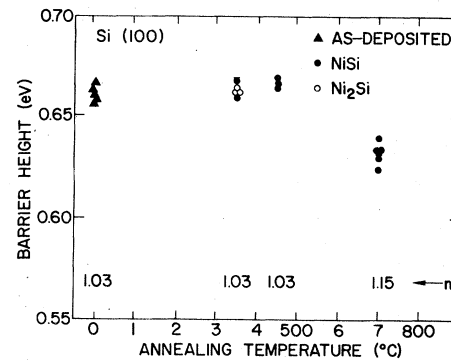


FIG. 6. Schottky barrier height of Ni, Ni<sub>2</sub>Si, and NiSi of diodes with the same analysis used in samples shown in Fig. 4.

indicated by the x-ray diffraction data of Fig. 8. This work and other reports show that epitaxial quality of the layer improves with an increase in annealing temperature.

The barrier heights have a value of about 0.75 eV for the as-deposited and 200 °C annealed samples (Fig. 9). The value of the barrier height decreased with no change in the ideality factor after samples were annealed to 500 °C. Samples annealed at 700 °C showed a pronounced change in the ideality factor as well as a decrease in barrier height. In these samples it was not possible to obtain reliable values for the barrier height of PdSi due to the degradation of the current-voltage characteristics.

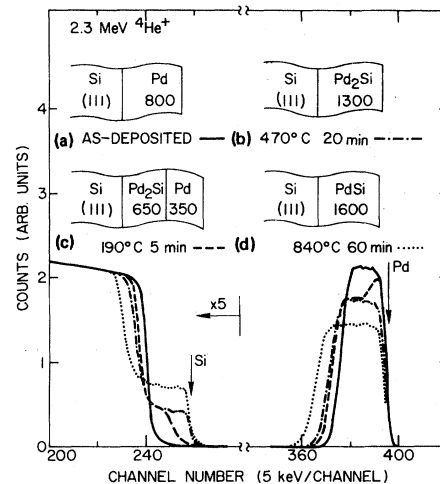


FIG. 7. Backscattering spectra of 800-Å Pd film on Si(100) at various stages of reaction: (a) as-deposited, (b) forming Pd<sub>2</sub>Si after 190 °C for 5 min, (c) a completion of Pd<sub>2</sub>Si formation after 470 °C for 20 min, and (d) a completion of PdSi formation after 840 °C for 60 min.

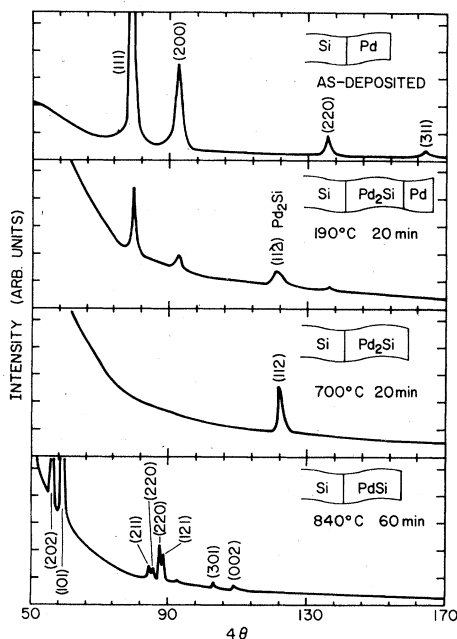


FIG. 8. X-ray diffraction spectra of samples analyzed by backscattering as shown in samples shown in Fig. 7.

#### IV. DISCUSSION

For the near-noble metals Ni, Pd, and Pt, the barrier heights on *n*-type silicon depend on the metal deposited and are relatively insensitive to the silicide phase. Other measurements on Co,<sup>19</sup> Ni,<sup>20,21</sup> Ir,<sup>22,23</sup> and Rh (Ref. 20) indicate that the barrier height does not depend on the silicide phase. The values listed in Table I show that there is a systematic increase in barrier height from Ni to Pd to Pt.

Comparison of the resistivity values with the barrier heights given in Table I shows that the sheet resistivity changes in a more pronounced

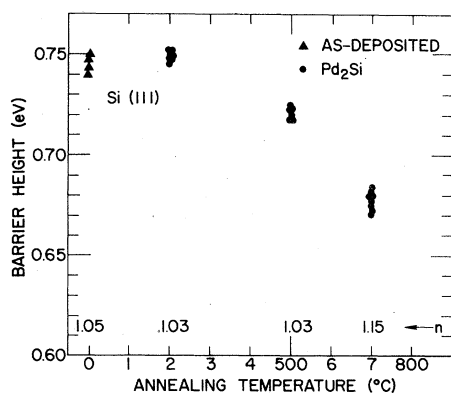


FIG. 9. Schottky barrier height of Pd and Pd<sub>2</sub>Si diodes with the same annealings used in Fig. 7.

manner with phase than does the barrier height. The resistivity depends on the bulk properties of the silicides and changes in resistivity reflect the changes in the silicon content of the silicide layer. The barrier height, on the other hand, apparently does not depend strongly upon the specific silicide phases.

The depth resolution of the RBS measurements is sufficient to identify the depth location of phases thicker than a few hundred angstroms but is not sensitive enough to identify thinner phases at the silicide-Si interface. The glancing-angle x-ray diffraction measurements can detect the presence, but not depth location, of silicide phases thicker than a few hundred angstroms. Consequently, these techniques do not allow identification of an interfacial layer, if present, having a thickness less than 100 Å. Many investigations have been reported concerning the presence, as well as structure, composition, and electron configuration, of a layer between Si and silicide. A clear understanding of the nature of the interface has not been achieved and indirect arguments must be used.

For the as-deposited case, Ni (Refs. 24 and 25) and Pd (Refs. 24, 26, and 27) can react with Si during deposition. Therefore, the barrier-height measurements must be interpreted on the basis of a reacted interfacial layer rather than for metal in contact with Si. This is consistent with the data in Table I that show the same barrier-height values for the as-deposited and first-phase cases.

During heat treatment, the first phase,  $M_2Si$ , forms between the Si substrate and the unreacted metal. This is not sufficient information to specify the nature of the silicide-Si interface. However, for Ni and Pt, with clean deposition and annealing procedures the second phase, the monosilicide, does not form until all the metal has been consumed in the formation of the first phase.<sup>17</sup> In these studies only two phases,  $M_2Si$  and  $M$  or  $MSi$ , have been identified in the early stages of heat treatment unless the metal layer was heavily contaminated with impurities. Since the growth kinetics of the present films followed normal behavior, we conclude that the barrier-height values given in Table I are for only one phase  $M_2Si$  or  $MSi$  in contact with Si. The transition from Pt<sub>2</sub>Si to PtSi in contact with Si(111) results in only a small change in barrier height of 0.02 to 0.03 eV. For Ni we find no measurable variation in barrier height with the transition from Ni<sub>2</sub>Si to NiSi in contact with Si(100).

There is only one silicide phase at the interface, but there can be a compositional gradient between the silicide phase and Si. There is evidence in Ni<sub>2</sub>Si structures for graded interfaces and interst-

itial Ni in the Si near the interface. It is likely that the nature of this interfacial layer can control the electronic properties of the silicon-silicide structure. We conclude that the interface layer is important because there is no correlation between the value of the barrier height and the known properties of the silicide phase.<sup>28</sup>

The decrease in the barrier height at high temperature can be due to differences in composition of the interfacial layer. This is not likely because a change in silicide phase should be reflected in the composition of the interfacial layer and in different values for the barrier height. This is contrary to the results reported in Table I. The decrease in the barrier height is more likely due to other phenomena such as diffusion of metal in the Si, stress effects, or development of lateral non-uniformities.

#### V. CONCLUSION

Near-noble metals deposited on silicon react at low temperatures to form well-defined phases. In

this study we monitored the growth of these phases and measured the value of the barrier height on *n*-type Si. We conclude that the barrier height depends on the particular metal deposited and is not sensitive to the particular phase that can be detected in the structure. We observe that the barrier height of the as-deposited metal is the same as that when the phases are formed, and hence believe that a reaction occurs between Si and the near-noble metal during deposition at room temperature. These results support the hypothesis of the presence of an interfacial layer which controls the electrical properties of the barrier in silicide-Si systems.

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