Flux-charge symmetric theory of superconducting circuits

Andr[e](https://orcid.org/0000-0003-4386-5947)w Osborne \bullet^* and Andrew Lucas[†]

Department of Physics and Center for Theory of Quantum Matter, [University of Colorado, Boulder,](https://ror.org/02ttsq026) Colorado 80309, USA

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The quantum mechanics of superconducting circuits is derived by starting from a classical Hamiltonian dynamical system describing a dissipationless circuit, usually made of capacitive and inductive elements. However, standard approaches to circuit quantization treat fluxes and charges, which end up as the canonically conjugate degrees of freedom on phase space, asymmetrically. By combining intuition from topological graph theory with a recent symplectic geometry approach to circuit quantization, we present a theory of circuit quantization that treats charges and fluxes on a manifestly symmetric footing. For planar circuits, known circuit dualities are a natural canonical transformation on the classical phase space. We discuss the extent to which such circuit dualities generalize to nonplanar circuits.

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I. INTRODUCTION

An ordinary nondissipative circuit, when sufficiently cooled such that all wires become superconducting, will exhibit macroscopic manifestations of quantum mechanics with a finite number of degrees of freedom. Such circuits are referred to as superconducting circuits; they are of interest for a variety of reasons, not least of which is the design and implementation of qubits for use in a future quantum computer $[1-5]$. To that end, the theory of superconducting circuits has been very successful in producing a number of qubits with desirable properties, including the transmon, $0-\pi$, and fluxonium qubits [\[6–9\]](#page-19-0). On more fundamental grounds, superconducting circuits are also of use for quantum simulation of exotic physics, such as particle motion on spaces with negative curvature [\[10\]](#page-19-0).

In the theory of superconducting circuits, charges and fluxes take the role of momenta and positions in classical Hamiltonian mechanics [\[11\]](#page-19-0). More formally, they are canonically conjugate degrees of freedom. For simple circuits, it is often straightforward to identify the conjugate pairs of charges and fluxes, and then promote these variables to operators, as in textbook quantum mechanics. This procedure is referred to as circuit quantization. However, for complicated circuits, namely, those containing both phase slips [\[12\]](#page-19-0) and Josephson junctions $[13,14]$, the standard approach $[15]$ to circuit quantization relies on using a *Lagrangian formulation* of the problem that breaks the explicit structure, such as the presence of canonical transformations that do not change the underlying structure behind Hamiltonian mechanics. In fact, only very recently have some authors [\[16–18\]](#page-19-0) begun to develop an intrinsically Hamiltonian [\[19\]](#page-19-0) approach to describing the classical (and quantum) mechanics of superconducting circuits.

Still, these approaches have continued to treat charge and flux on an arguably asymmetric footing.

This paper presents a theory of circuit quantization that is manifestly symmetric under the exchange of charge and flux degrees of freedom, and treats capacitors and inductors on an equal footing. An advantage of this approach is that it makes certain "mysterious" properties of the algorithmic method of [\[16\]](#page-19-0), such as the appearance of conserved quantities, more manifest. Moreover, our approach provides an extremely transparent description of *circuit dualities* [\[20,21\]](#page-19-0) for planar circuits, and—in some special cases—for nonplanar circuits as well.

II. CLASSICAL THEORY OF CIRCUITS

We consider circuits made out of elements that are either purely inductive or purely capacitive. An inductive element has a constitutive relation of the form

$$
I = \frac{\partial E}{\partial \phi},\tag{2.1}
$$

where *E* is the energy stored in the element and ϕ is the magnetic flux through it. Likewise, a circuit element with a constitutive relation

$$
V = \frac{\partial E}{\partial q} \tag{2.2}
$$

is a capacitor: here, *q* is the charge accumulated across the capacitor, while *V* is the voltage. Note that these definitions include arbitrary nonlinear elements such as the Josephson junction and the quantum phase slip junction. From the perspective of circuit quantization, these nonlinear elements are no obstruction to any of the results that we present.

Loosely speaking, $I = \dot{q}$ and $V = \dot{\phi}$ (here, dots denote time derivatives). This suggests that inductors and capacitors host conjugate degrees of freedom in a superconducting circuit.

^{*}andrew.osborne-1@colorado.edu

[†]andrew.j.lucas@colorado.edu

A. Symplectic geometry approach to circuit quantization

It is our goal to produce a quantization prescription for superconducting circuits that treats capacitors and inductors (equivalently, charges and fluxes) on equal footing. To ensure full generality in our construction, we will begin with a short review of a recently developed [\[16\]](#page-19-0) symplectic approach to the quantization of circuits, which is applicable to arbitrarily nonlinear circuits built out of inductors and capacitors. Besides having the advantage of being more general (the new approach can quantize circuits for which a standard Lagrangian does not exist), we will show in this paper that the approach of $[16]$ also beautifully encodes the mathematics of circuit duality, when rewritten in a flux-charge symmetric manner.

In [\[16\]](#page-19-0), it was found that a Hamiltonian dynamical system—namely, a Hamiltonian function *H* and a symplectic form and/or Poisson bracket on a suitable phase space—is neatly encoded in a simple Lagrangian that depends on the incidence matrix of a circuit. A circuit can be thought of mathematically as a directed graph with vertices *v* and directed edges *e*, which have a start and end vertex. On each edge *e*, we place either an inductive or capacitive element whose energy *E* depends either on the flux difference ϕ_e across the circuit element or on the charge *qe* which has accumulated due to current flow across the edge. The directedness of each edge is important to capture the correct sign of ϕ_e and q_e . For the remainder of this manuscript, we will use the symbol $\mathcal E$ to refer to the set of edges in a circuit. Generally, the circuit to which $\mathcal E$ pertains will be clear from context. We define the incidence matrix

$$
A_{ev} = \begin{cases} 1, & e \text{ arrives at } v \\ -1, & e \text{ leaves from } v \\ 0, & \text{otherwise,} \end{cases}
$$
 (2.3)

which encodes a convention for positive current and voltage across an edge. There is another closely related matrix Ω , called the reduced incidence matrix, which is a restriction of *A* to edges containing only capacitors. In terms of Ω , the action encoding the dynamics of *G* may be written as

$$
S = \int dt \left[\sum_{e \in C, v} q_e \Omega_{ev} \dot{\phi}_v - \sum_{e \in C} E_e^C(q_e) - \sum_{e \in \mathcal{I}} E_e^L(A_{ev} \phi^v) \right],
$$
(2.4)

with capacitive branches in the set C and inductive branches in the set *I*. Note that $\mathcal{E} = \mathcal{C} \cup \mathcal{I}$. Here, E_e^C (E_e^L) is the energy of the capacitor (inductor) on branch *e* for a given configuration.

Quantization of a circuit is achieved by enumerating and removing the null vectors of Ω and the corresponding variables. The resulting invertible matrix Ω can be related to a symplectic form and Poisson bracket, which then formally lead to a canonical quantization prescription of the circuit [\[16\]](#page-19-0).

B. Topology of a graph

In this paper, we will need to review a little more graph theory than was presented above. Indeed, in the language of mathematics, circuits are directed graphs where the edge set $\mathcal{E} = \mathcal{C} \cup \mathcal{I}$ has a decomposition into capacitors and inductors.

We now briefly review some of the relevant graph theory and refer the reader to Appendix [A](#page-12-0) for a more formal discussion.

The most important aspect of a graph for us here will be the structure of cycles, or loops. For an undirected graph, it is possible to define cycle addition $[22,23]$ as an additive operation on a vector space over the field \mathbb{Z}_2 . This operation imbues us with a natural notion of linear independence between cycles. This notion of independence will remain relevant for circuits, which are directed graphs, since the "arrow" on each edge is used to keep track of the direction of current flow, but not whether or not an object is a loop.

For a circuit with $|\mathcal{E}|$ edges and $|\mathcal{V}|$ vertices, there are $|\mathcal{E}|$ – $|\mathcal{V}| + 1$ linearly independent loops, assuming that the circuit is connected. For reasons that will become clear, we will find it expedient to find a basis for this space with *one redundant loop*, i.e., we choose $|\mathcal{E}| - |\mathcal{V}| + 2$ loops and collect them into set

$$
\mathcal{L} = \{l_1, l_2, \dots, l_{|\mathcal{E}|-|\mathcal{V}|+2}\}.
$$
 (2.5)

To each loop, assign an orientation such that an edge in the loop *l* may either be oriented with *l* or against *l*. Such assignments are encoded in an *orientation matrix*,

$$
B_{le} = \begin{cases} 1, & l \text{ and } e \text{ are oriented alike} \\ -1, & l \text{ and } e \text{ are oriented unalike} \\ 0, & e \text{ does not lie on the boundary of } l. \end{cases}
$$
 (2.6)

For an example, consider the graph drawn in Fig. $1(a)$. The orientation matrix for this graph is given by

$$
B = \begin{pmatrix} e_1 & e_2 & e_3 & e_4 & e_5 & e_6 & e_7 & e_8 & e_9 & e_{10} \\ 1 & 0 & 1 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 1 & 0 & 1 & 1 & -1 & -1 \\ 0 & 0 & -1 & 1 & 0 & 1 & 0 & -1 & 0 & 0 \\ -1 & 1 & 0 & -1 & -1 & -1 & 0 & 0 & 1 & 1 \end{pmatrix} \begin{matrix} l_1 \\ l_2 \\ l_3 \\ l_4 \end{matrix} \tag{2.7}
$$

Since we have defined $\mathcal L$ in such a way that it always contains $|\mathcal{E}| - |\mathcal{V}| + 2$ elements, it is always the case that

$$
|\mathcal{L}| - |\mathcal{E}| + |\mathcal{V}| = 2. \tag{2.8}
$$

Euler's formula should be called to mind by (2.8) . As we will see, this is no accident.

Every graph (and thus every circuit) can be drawn (more formally, embedded) on some closed, orientable surface¹ with no crossing edges. One can always find such a surface, wherein this drawing of a graph partitions the surface of embedding into some number of regions that are isomorphic to the unit disk. We will call every such two-dimensional disk a *face* of the circuit. For a particular drawing of a circuit on a surface of genus *g*, we will write that the number of faces

¹The surfaces one should keep in mind are the Riemann surfaces of genus *g*, including the sphere ($g = 0$) and the torus ($g = 1$). Such surfaces will always be sufficient since the topology of two-dimensional orientable manifolds is fully characterized by their genus.

FIG. 1. Examples of faces and edges in a (a) planar and (b) nonplanar graph. (a) An embedding of a graph with orientations chosen for faces and branches. The outer face is labeled f_4 . All faces are oriented alike if we consider this plane to be a patch of a sphere (namely we identify points at infinity as the same point). (b) An embedding of K_5 on the torus. The vertical border at the top of the drawing is to be identified with the vertical border at the bottom of the drawing. Likewise, the horizontal boundaries are to be identified. K_n is the fully connected graph on *n* vertices, and for $n \geq 5$, K_n is nonplanar. Nonplanar graphs cannot be embedded on the sphere, but only on a torus with a postive number of handles. A valid choice of "topological loops" (see footnote 2) is given by the blue and red edges.

induced by the drawing is $|\mathcal{F}|$. Euler's formula reads

$$
|\mathcal{F}| - |\mathcal{E}| + |\mathcal{V}| = 2 - 2g.
$$
 (2.9)

Evidently, (2.9) together with (2.8) implies that

$$
|\mathcal{L}| = |\mathcal{F}| + 2g. \tag{2.10}
$$

Of course, one may have suspected from the outset that $|\mathcal{L}|$ was closely related to $|\mathcal{F}|$ since the boundary of a unit disk is a circle, i.e., a one-dimensional object.

We emphasize that the distinction between loops and faces (at least for planar graphs) is very minor. For planar graphs, there is a precise correspondence between faces and loops since there is a (contractible) loop at the boundary of each face. For nonplanar graphs such as K_5 [see Fig. 1(b)], there are necessarily some number of loops which are topological.² As we will discuss in later sections, the presence of such "topological" loops is of some import to the existence of a dual circuit; more precisely, the set of loops at the boundary of some face in a drawing of a planar graph on the sphere (or the plane) number $|\mathcal{E}| - |\mathcal{V}| + 2$, and every edge exists in the common boundary of exactly two faces. Moreover, it is possible to demand that all the loops chosen in this way are "oriented alike" such that planar graphs satisfy 3

$$
\sum_{l \in \mathcal{L}} B_{le} = 0. \tag{2.11}
$$

As we will see, choosing loops in correspondence with faces will be of great utility for us, even for nonplanar graphs. It will always be our convention to choose $|\mathcal{F}|$ loops corresponding to the faces of some embedding of a circuit, and we will also always choose them to be oriented alike.

Another important matter of convention arises when considering the sign of B_{le} when it is nonzero. Consider Fig. 1(a) with the loop consisting of edges e_1 , e_3 , and e_7 . Intuitively, it should be the case that a suitable definition of *B* for this graph has the property that B_{l_1e} is nonzero only for *e* in {*e*₁, *e*₃, *e*₇}. With this preference in mind, it remains to fix the sign of B_{l_1e} for such edges *e*. Our convention will be that an orientation should be chosen for l_1 so that B_{l_1e} is equal to positive one if e is oriented like l_1 , and negative one otherwise. In this particular example (as determined by the semicircular arrow surrounding the label f_1), the matrix elements of *B* should be $B_{l_1e_1} = B_{l_1e_3} = -B_{l_1e_7} = 1.$

For nonplanar graphs, it is always possible to choose an embedding such that every edge appears on the boundary of precisely two faces (and thus is included in precisely two

²By referring to a loop as "topological," we mean to denote that the loop is not contractible on the surface of embedding. For planar graphs, all loops can be expressed as some combination of contractible loops.

³We emphasize that this particularly simple redundancy in $|\mathcal{L}|$ is a consequence of choosing loops in correspondence to faces. In principle, it is possible to choose a spanning set of loops with a less trivial redundancy, but this complicates calculations and provides no simplification. Any choice of loops for a planar graph can be shown to correspond to the faces of *some* drawing, so this choice is also perfectly general.

loops chosen in correspondence with the faces). However, it is not always possible to choose an embedding such that every edge appears in precisely two loops in \mathcal{L} . As an example, consider edge *e*⁹ in the circuit drawn in Fig. [1\(b\).](#page-2-0) Here, *e*⁹ appears on the boundary of f_5 , and on the boundary of no other face. However, e_9 appears on the boundary of f_5 twice. When this occurs, we take the convention that $B_{l_5e_9} = 0$, since "each" side" of e_9 is seen by the same face and $+1 - 1 = 0$.

In order to define an orientation matrix for a nonplanar graph, one needs to choose appropriate topological loops and repeat the procedure. For the graph drawn in Fig. $1(b)$, one topological loop is drawn in blue, while the other is drawn in red. The orientation matrix for this graph is given by

$$
B = \begin{pmatrix} e_1 & e_2 & e_3 & e_4 & e_5 & e_6 & e_7 & e_8 & e_9 & e_{10} \\ 0 & 1 & -1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & -1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 1 & 0 & 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & -1 & 1 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 1 & 0 \end{pmatrix} \begin{matrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \\ I_7 \end{matrix} \tag{2.12}
$$

It turns out that *B* (for any drawing of *G*) has the property that

$$
\sum_{e} B_{le} A_{ev} = 0. \tag{2.13}
$$

In the case of (circuits that can be embedded as) planar graphs, this is an elementary result from algebraic topology [\[23\]](#page-19-0): *B* and *A* are the discrete differential acting on 0-forms (defined on vertices) and 1-forms (defined on edges), respectively (see Appendix [A\)](#page-12-0). For nonplanar graphs, the matrix *B* includes the discrete differential acting on 1-forms *and* the nontrivial elements of the first cohomology group. While we are not aware of any elegant geometric interpretation of this combined object, (2.13) continues to hold. Note, however, that for nonplanar graphs, the condition [\(2.11\)](#page-2-0) cannot hold. However, there is some analogous expression corresponding to the set of "facelike" loops in $\mathcal L$. In the case of the circuit drawn in Fig. [1\(b\),](#page-2-0) (2.12) admits

$$
\sum_{i=1}^{5} B_{l_i e} = 0.
$$
 (2.14)

It is always possible to incorporate some such condition into a choice of loops in \mathcal{L} .

We now introduce our third and final matrix. First, note that it follows from (2.13) that for a set $P \subset \mathcal{E}$,

$$
\sum_{e \in P} B_{le} A_{ev} = -\sum_{e \notin P} B_{le} A_{ev}.
$$
 (2.15)

This fact will be of great use to us. In particular, there will be a natural partition *P* for a circuit: simply count only the capacitive, or only the inductive, edges. Hence for any circuit, we define the *connection matrix*

$$
M_{lv} = \frac{1}{2} \sum_{e \in C} B_{le} A_{ev} - \frac{1}{2} \sum_{e \in \mathcal{I}} B_{le} A_{ev}.
$$
 (2.16)

FIG. 2. A circuit with four faces (counting the external face), six edges, and four vertices. For this circuit, $\mathcal{I} = \{e_1, e_6, e_2\}$ and $C = \{e_3, e_4, e_5\}$. To see that all faces are "oriented alike," imagine the circuit embedded on the sphere: all faces are oriented into the sphere.

Consider the circuit drawn in Fig. 2, which we will call *G*. In the following discussion, we will repeatedly return to *G* as an example for the sake of concreteness. As we will see, the connection matrix of a circuit has a number of remarkable properties. For the circuit *G* in Fig. 2,

$$
A = \begin{pmatrix} v_1 & v_2 & v_3 & v_4 \\ -1 & 1 & 0 & 0 & e_1 \\ 0 & -1 & 1 & 0 & e_2 \\ 1 & 0 & -1 & 0 & e_3 \\ -1 & 0 & 0 & 1 & e_4 \\ 0 & 0 & 1 & -1 & e_5 \\ 0 & -1 & 0 & 1 & e_6 \end{pmatrix}
$$
 (2.17)
\ne₁ (2.17)
\ne₂ e₃ e₄ e₅ e₆
\n
$$
\begin{pmatrix} e_1 & e_2 & e_3 & e_4 & e_5 & e_6 \\ 1 & 0 & 0 & -1 & 0 & 1 \end{pmatrix} l_1
$$

$$
B = \begin{pmatrix} 1 & 0 & 0 & -1 & 0 & 1 \\ 0 & 1 & 0 & 0 & -1 & -1 \\ 0 & 0 & 1 & 1 & 1 & 0 \\ -1 & -1 & -1 & 0 & 0 & 0 \end{pmatrix} \begin{matrix} l_1 \\ l_2 \\ l_3 \\ l_4 \end{matrix}
$$
 (2.18)

and

$$
M = \begin{pmatrix} v_1 & v_2 & v_3 & v_4 \\ 1 & 0 & 0 & -1 \\ 0 & 0 & -1 & 1 \\ 0 & 0 & 0 & 0 \\ -1 & 0 & 1 & 0 \end{pmatrix} \begin{matrix} l_1 \\ l_2 \\ l_3 \\ l_4 \end{matrix}
$$
 (2.19)

It is possible to build a robust theory of circuit quantization using *B* in place of the incidence matrix of a circuit *A* or, indeed, in conjunction with *B*. While this point is conceptually appealing on its own, it also turns out to be necessary to understand circuit duality in full generality. The main result of this paper is that the matrix *M*, containing information inherited from both *A* and *B*, encodes the symplectic

⁴Here, l_5 is used to denote the loop on the boundary of the face f_5 .

form of the classical phase space, which may be used to quantize a Hamiltonian without requiring the user to proclaim that charges are more fundamental than fluxes, or vice versa.

C. A symmetric circuit Lagrangian

The charge accumulated on a particular capacitive branch is given by $q_e = \sum_l q_l B_{le}$, which may be used to connect to the formalism of $\overline{[16]}$ $\overline{[16]}$ $\overline{[16]}$, as we will see later. Moreover, these loop charge variables are precisely the ones described in [\[20\]](#page-19-0), with the exception of the fact that we "count" the external loop. Of course, this is only a matter of convenience since one is always free to fix one loop charge to vanish as a gauge degree of freedom, in direct analogy with one's freedom to choose a ground. Now, for any circuit,

$$
\frac{1}{2} \sum_{e \in C} q_l B_{le} A_{ev} \dot{\phi}_v - \frac{1}{2} \sum_{e \in \mathcal{I}} q_l B_{le} A_{ev} \dot{\phi}_v
$$
\n
$$
= \sum_{e \in C} q_l B_{le} A_{ev} \dot{\phi}_v = - \sum_{e \in \mathcal{I}} q_l B_{le} A_{ev} \dot{\phi}_v, \tag{2.20}
$$

according to (2.15) . While (2.20) contains only trivial mathematical information, we notice that the first expression in (2.20) is not preferential toward inductive or capacitive branches, while the second two expressions *are*.

For the remainder of this manuscript, we will write E_e^L (E_e^C) to denote the energy of an inductive (capacitive) branch *e* in some circuit. We assume that such energies may only depend on the flux across (the charge on) some branch.⁵ Explicitly, we require that for $e = (v_1, v_2)$, E_e^I depends only on $\phi_{v_1} - \phi_{v_2}$. Analogously, for a branch adjacent to the loops l_1 and l_2 , we require that E_e^C may depend only on $q_{l_1} - q_{l_2}$. As we will show shortly, this demand is equivalent to the imposition of Kirchoff's rules. We claim that the Lagrangian

$$
L = \sum_{l,v} q_l M_{lv} \dot{\phi}_v - \sum_{e \in C} E_e^C \left(\sum_l q_l B_{l e} \right)
$$

$$
- \sum_{e \in \mathcal{I}} E_e^L \left(\sum_v A_{ev} \phi_v \right) \tag{2.21}
$$

is a general Lagrangian which can be used to describe arbitrary LC circuits, and which contains a Hamiltonian which is easily quantizable.

Let us examine the equations of motion implied by the principle of least action applied to $S = \int dt L$:

$$
0 = \frac{\delta S}{\delta q_l} = \sum_{v} M_{lv} \dot{\phi}_v - \sum_{e \in C} \frac{\partial E_e^C}{\partial q_l},
$$

$$
0 = \frac{\delta S}{\delta \phi_v} = -\sum_{l} \dot{q}_l M_{lv} - \sum_{e \in \mathcal{I}} \frac{\partial E_e^L}{\partial \phi_v}.
$$
 (2.22)

We rewrite the first line using the definition of *M*, to see that

$$
0 = -\sum_{e \in \mathcal{I}, v} B_{le} A_{ev} \dot{\phi}_v - \sum_{e \in \mathcal{C}} \frac{\partial E_e^C}{\partial q_l}.
$$
 (2.23)

Another way of writing (2.23) is

$$
0 = \sum_{e \in \mathcal{C}, v} B_{le} A_{ev} \dot{\phi}_v - \sum_{e \in \mathcal{C}} \frac{\partial E_e^C}{\partial q_l}.
$$
 (2.24)

Further, since we have demanded that E_e^C may only depend on $\sum_l B_{l}q_l$, we can see that (2.24) implies $\sum_l B_{l}q_l$, we can see that (2.24) implies

$$
0 = \sum_{e \in C} B_{le} \left[\sum_{v} A_{ev} \dot{\phi}_v - \frac{\partial E_e^C(q)}{\partial q} \right].
$$
 (2.25)

Given that $\sum_{v} A_{ev} \dot{\phi}_v$ can be interpreted as a voltage difference across branch e , we see that (2.25) is compatible with the constitutive relation for capacitors,

$$
\sum_{v} A_{ev} \dot{\phi}_v = \frac{\partial E_e^C(q)}{\partial q}.
$$
 (2.26)

In fact, we will show in Corollary $B2$ that (up to a certain exception to be discussed later) the *only* solution to (2.25) is (2.26). Substituting

$$
\sum_{e \in C} \frac{\partial E_e^C}{\partial q_l} = \sum_{e \in C, v} B_{le} A_{ev} \dot{\phi}_v, \tag{2.27}
$$

we can see that (2.23) becomes

$$
\sum_{e,v} B_{le} A_{ev} \dot{\phi}_v = 0.
$$
 (2.28)

In other words, (2.23) is also consistent with Kirchoff's voltage rule around a particular loop *l*.

Likewise, we rewrite the second line of (2.22) as

$$
0 = -\sum_{l,e \in C} \dot{q}_l B_{le} A_{ev} - \sum_{e \in \mathcal{I}} \frac{\partial E_e^L}{\partial \phi_v}
$$

=
$$
\sum_{l,e \in \mathcal{I}} \dot{q}_l B_{le} A_{ev} - \sum_{e \in \mathcal{I}} \frac{\partial E_e^L}{\partial \phi_v}.
$$
 (2.29)

A similar manipulation to the one in (2.23) and (2.24) can be used to show that (2.29) correctly incorporates the constitutive relation for inductors, as well as Kirchoff's current law on a particular node *v*.

D. A Hamiltonian theory from a Lagrangian theory

Classically, the dynamics of a circuit are entirely determined by the Lagrangian in (2.21) . In order to quantize, however, we must produce a symplectic form, which will in turn imply quantum commutation relations between charge and flux operators. Practically, this is a matter of enumerating the null vectors of *M* and integrating out related nondynamical variables, as was done in $[16]$. One of the notable properties of the formalism at hand is that the null vectors of *M* do not asymmetrically depend on inductors and capacitors.

⁵Ideal nonreciprocal circuit elements such as gyrators do exist that are not of this form [\[24\]](#page-19-0). We leave any possible generalization of our results to such circuits for future work.

In lieu of a formal discussion, we will focus on a particular example to demonstrate the simplicity of our results. For a formal discussion, see Appendix [B.](#page-15-0) For the time being, we will consider the circuit drawn in Fig. [2,](#page-3-0) which we will call *G*. We will suppose that all circuit elements are linear and equal, though we emphasize that this is purely a matter of convenience. The Lagrangian for *G* is

$$
L = (q_{l_3} - q_{l_4})(\dot{\phi}_{v_1} - \dot{\phi}_{v_3}) + (q_{l_3} - q_{l_1})(\dot{\phi}_{v_4} - \dot{\phi}_{v_1})
$$

+ $(q_{l_3} - q_{l_2})(\dot{\phi}_{v_3} - \dot{\phi}_{v_4})$
- $\frac{1}{2C}(q_{l_3} - q_{l_4})^2 - \frac{1}{2C}(q_{l_3} - q_{l_1})^2 - \frac{1}{2C}(q_{l_3} - q_{l_2})^2$
- $\frac{1}{2L}(\phi_{v_2} - \phi_{v_1})^2 - \frac{1}{2L}(\phi_{v_3} - \phi_{v_2}) - \frac{1}{2L}(\phi_{v_4} - \phi_{v_2})^2.$
(2.30)

 $\sum_l \gamma_l M_{lv} = 0$ for all *v*, correspond to cycles either made Left null vectors of M , namely, those vectors γ_l such that entirely of capacitors or entirely of inductors. In *G*, there is only a single such cycle, namely, the cycle bounding the loop *l*3. Constraints of this kind may involve the resolution of some constraint, as is the case now,

$$
0 = \frac{\delta S}{\delta q_{l_3}} = \frac{1}{C}(q_{l_3} - q_{l_4}) + \frac{1}{C}(q_{l_3} - q_{l_1}) + \frac{1}{C}(q_{l_3} - q_{l_2}).
$$
\n(2.31)

The constraint in (2.31) corresponds to the demand that voltage must vanish about a loop, and further that q_{l3} must be determined by the other loop charges. In other words, q_{l_3} is not dynamical. If, instead of capacitors, there was a cycle of inductors so that there was no voltage constraint, the relevant *q* variable would simply be canceled in *L*. This corresponds to a row of *M* which is identically zero in every entry.

On the other hand, right null vectors of *M* correspond to *cuts* of *G* which are entirely inductive or entirely capacitive. A cut of G is a set of edges that connects a subset of V to its complement. In *G*, there is a single such example, namely, the cut consisting of the branches incident upon v_2 . Notice that $\dot{\phi}_{v_2}$ does not appear in (2.30) at all, so ϕ_{v_2} plays the role of a Lagrange multiplier. Recognizing that

$$
0 = \frac{\delta S}{\delta \phi_{v_2}}\tag{2.32}
$$

gives rise to another constraint. This constraint may be interpreted as a demand that current must be conserved at the node v_2 , and that ϕ_{v_2} must therefore be fixed in terms of other fluxes.

There is another pair of null vectors which is omnipresent in the theory of circuits. Namely, energies may only depend upon differences of loop current (node flux), so the sums $\sum_{v} \phi_v$ and $\sum_{l \in \mathcal{F}} q_l$ are fixed by a so-called gauge freedom.⁶ Explicitly,

$$
0 = \sum_{v} \frac{\delta S}{\delta \phi_{v}} = \sum_{l} \frac{\delta S}{\delta q_{l}}.
$$
 (2.33)

Since both of these functional derivatives vanish identically, a constraint can never be imposed by these particular null vectors.

After resolving the constraints in (2.31) and (2.32) , we are left with

$$
L = Q_1 \dot{\Phi}_1 + Q_2 \dot{\Phi}_2 - \frac{1}{3C} (Q_1^2 - Q_1 Q_2 + Q_2^2)
$$

-
$$
\frac{1}{3L} (\Phi_1^2 - \Phi_1 \Phi_2 + \Phi_2^2),
$$
 (2.34)

with

$$
Q_1 = q_{l_2} - q_{l_4},
$$

\n
$$
Q_2 = q_{l_2} - q_{l_1},
$$

\n
$$
\Phi_1 = \phi_{v_1} - \phi_{v_3},
$$

\n
$$
\Phi_2 = \phi_{v_4} - \phi_{v_1},
$$
\n(2.35)

and

$$
\{\Phi_j, Q_i\} = \delta_{ij}.\tag{2.36}
$$

Therefore, we are free to write

$$
H = \frac{1}{3C} (Q_1^2 - Q_1 Q_2 + Q_2^2) + \frac{1}{3L} (\Phi_1^2 - \Phi_1 \Phi_2 + \Phi_2^2),
$$
\n(2.37)

with quantum commutation relations

$$
[\Phi_j, Q_i] = i\hbar \delta_{ij}.
$$
 (2.38)

The process of "integrating out" degrees of freedom associated to null vectors that arise during this process is conceptually straightforward. Still, as was the case in [\[16\]](#page-19-0), nonlinear constraint equations may arise in the presence of nonlinear circuit elements without accompanying parasitic elements; these nonlinear equations may not have unique solutions, implying ambiguities in the correct phase space to quantize. Since it was argued in $[25]$ that the addition of parasitic elements (which are present in any real experiment) qualitatively changes the spectrum, we do not focus on the technical question of picking the correct phase space in the presence of nonlinear constraints further in this manuscript.

There is another subtlety that arises in an attempt to formalize a generic quantization algorithm. In some circuits, there are conjugate pairs corresponding to a two-dimensional subspace of phase space that is not isomorphic to \mathbb{R}^2 . The most readily available example is the transmon qubit (see Sec. VB), where the flux across the Josephson junction is thought to be compact, which implies that the charge across the capacitor is integer valued. Physically, this implication can be understood by the fact that the energy on the capacitor is a function of the number of Cooper pairs in the condensate on the plates of the capacitor. Mathematically, the consequence of this fact is that the operator Φ is not Hermitian. The problem of quantizing a Hamiltonian on a phase space of arbitrary topology is beyond the scope of this paper. However, we remark that the particular (and most experimentally relevant) example of a phase space

⁶We remark that $\sum_{l \in \mathcal{L}} q_l$ is not necessarily nondynamical. This leads to subtleties when discussing circuit dualities, which are discussed in Sec. [IV.](#page-7-0)

isomorphic to $\mathbb{R} \times S^1$ is understood [\[26\]](#page-19-0), and the resolution is that the operator algebra (2.38) is replaced by

$$
[e^{i\Phi}, Q] = i\hbar e^{i\Phi}.
$$
 (2.39)

We will remark on the implications of this fact on circuit duality in Sec. [IV.](#page-7-0)

III. EQUIVALENCE TO OTHER FORMULATIONS

Formally, it is true that the circuit Lagrangian [\(2.21\)](#page-4-0) encodes all of the necessary physics: Kirchoff's rules are either manifestly obeyed or correspond to the Euler-Lagrange equations of (2.21) . It must then be true that the predictions of [\(2.21\)](#page-4-0) are equivalent to previous theories in the literature. This equivalence is formally demonstrable, as we now summarize; see Appendix \bf{B} \bf{B} \bf{B} for details and/or justifications of the claims made in this section.

A. Branch-node formalism

The most common approach to circuit quantization involves writing a Lagrangian in terms of fluxes that live on vertices alone: ϕ_v . If we have linear capacitors, then one can directly integrate out q_l in [\(2.21\)](#page-4-0) to obtain a Lagrangian for ϕ ^{*v*} alone with quadratic terms in $\dot{\phi}$.

However, it was recently pointed out in [\[16\]](#page-19-0) that more general circuits could be quantized by instead starting with a Lagrangian that depends on both $q_{e\in\mathcal{C}}$ (charges on capacitive edges) and ϕ_v . Comparing the flux-charge symmetric formulation to this one is slightly more subtle. Recall that we may write

$$
M_{lv} = \sum_{e \in C} B_{le} A_{ev}.
$$
 (3.1)

Introduce a set of Lagrange multipliers λ*^e* on capacitive edges and write

$$
L' = \sum_{e \in C} q_l B_{le} A_{ev} \dot{\phi}_v - \sum_{e \in C} E_e^C(Q_e) - \sum_{e \in \mathcal{I}} E_e^L\left(\sum_v A_{ev} \phi_v\right) + \sum_{e \in C} \lambda_e \left(Q_e - \sum_l q_l B_{le}\right).
$$
 (3.2)

The functional derivative

$$
0 = \frac{\delta S}{\delta q_l} = \sum_{e \in \mathcal{C}} B_{le} \left[\sum_v A_{ev} \dot{\phi}_v - \lambda_e \right]
$$
 (3.3)

implies that the quantity

$$
\gamma_e = \sum_v A_{ev} \dot{\phi}_v - \lambda_e \tag{3.4}
$$

forms a right null vector of the matrix *B* restricted to the set of capacitive edges. Corollary **[B1](#page-15-0)** shows that there is one such null vector for each capacitive cut of *G*. As a consequence, there exist *m* vectors $|n_i\rangle = \sum_{e \in C} \sigma_{e,i} |e\rangle$ with $\sigma_{e,i} \in$ {−1, 0, 1}, with *i* = 1, 2, 3,..., *m*, such that

$$
|\gamma\rangle = \sum_{i=1}^{m} \mu_i |n_i\rangle, \qquad (3.5)
$$

and thus

$$
\lambda_e = \sum_{v} A_{ev} \dot{\phi}_v - \sum_{i=1}^{m} \mu_i \sigma_{e,i}, \qquad (3.6)
$$

for some parameter μ . Thus, it follows that L' may be rewritten,

$$
L' = \sum_{e \in C} Q_e A_{ev} \dot{\phi}_v - \sum_{e \in C} E_e^C(Q_e) - \sum_{e \in \mathcal{I}} \left(\sum_v A_{ev} \phi_v \right)
$$

$$
- \sum_{i=1}^m \mu_i \sum_e \sigma_{e,i} Q_e.
$$
(3.7)

A functional derivative

$$
0 = \frac{\delta S}{\delta \mu_i} = \sum_e \sigma_{e,i} Q_e \tag{3.8}
$$

is easily understood as a consequence of

$$
\sum_{l,e} q_l B_{le} \sigma_{e,i} = 0, \qquad (3.9)
$$

and can be recognized as a constraint that would follow from a Noether current in [\[16\]](#page-19-0). Borrowing the terminology used in $[16]$, the right null vectors of *B* restricted to edges in C corresponded to a "capacitively shunted island." In the end, after using the Lagrange multiplier μ_i to fix the charges across capacitive cuts, we see that (3.7) reproduces [\[16\]](#page-19-0).

B. Face-edge formalism

A possibly undesirable feature of the Lagrangian in (3.7) is that capacitors are treated differently than inductors. With the flux-charge symmetric framework, however, we can produce a similarly universal theory of circuits that treats inductors as preferential. We write

$$
M_{lv} = -\sum_{e \in \mathcal{I}} B_{le} A_{ev}.
$$
 (3.10)

In direct analogy with the discussion in Sec. III A, we again introduce Lagrange multipliers λ_e , but this time they exist only on inductive edges,

$$
L' = -\sum_{e \in \mathcal{I}} q_l B_{le} A_{ev} \dot{\phi}_v - \sum_{e \in \mathcal{C}} E_e^C \left(\sum_l q_l B_{le} \right)
$$

$$
- \sum_{e \in \mathcal{I}} E_e^L \left(\sum_v \psi_e \right) + \sum_{e \in \mathcal{I}} \lambda_e \left(\psi_e - \sum_v A_{ev} \phi_v \right).
$$
(3.11)

By taking functional derivatives and exploiting the properties of *A*, it is possible to perform a calculation very closely mirroring the one in Sec $III \land$ to produce

$$
L' = -\sum_{e \in \mathcal{I}, l} q_l B_{le} \dot{\psi}_e - \sum_{e \in \mathcal{C}} E_e^C(Q_e) - \sum_{e \in \mathcal{I}} E_e^L(\psi_e). \quad (3.12)
$$

Of note, the role of matrix *A* in (3.7) is filled by −*B* in (3.12). From a formal perspective, the matrix *B* is less well behaved than *A* since, for nonplanar graphs, *B* may have less trivial null vectors than *A*, and there is no corresponding

subtlety for the structure of *A*, even for nonplanar graphs. Equation (3.12) is a so-called loop-branch⁷ Lagrangian.

In the special case when the circuit corresponds to a planar graph, it was noted in $[20]$ that Lagrangians of the form (3.12) are dual to Lagrangians of the form (3.7) , as we discuss in Sec. IV. This fact is intimately related to the appearance of *B* in [\(3.12\)](#page-6-0) instead of *A*. Using the flux-charge symmetric Lagrangian [\(2.21\)](#page-4-0), we will see a more straightforward derivation of such duality.

IV. CIRCUIT DUALITY

The fact that we are able to describe a circuit in either a framework that "prefers" capacitors *or* inductors is reminiscent of classical discussions of circuit duality [\[21,27–30\]](#page-19-0); see [\[20\]](#page-19-0) for a discussion of such circuit dualities in the context of Lagrangian mechanics of superconducting circuits. We now show that these dualities are especially transparent in our framework. A formal discussion of the results that follow is found in Appendix [C.](#page-17-0)

First we make a few general comments. Any sensible notion of duality should be an involution (operation which is the identity when applied twice) on classical phase space (or quantum Hilbert space) of a circuit. A circuit is said to be selfdual if its Hamiltonian is invariant under this transformation.

One kind of duality arises by a mere "relabeling transformation" on (2.21) . With the Lagrangian (2.21) in mind, consider the transformation given by

$$
\phi_v \rightarrow \phi_v^* = q'_v,
$$

\n
$$
q_l \rightarrow q_l^* = \phi'_l,
$$

\n
$$
A \rightarrow A^* = B^T,
$$

\n
$$
B \rightarrow B^* = A^T,
$$

\n
$$
C \rightarrow C^* \simeq \mathcal{I},
$$

\n
$$
\mathcal{I} \rightarrow \mathcal{I}^* \simeq C,
$$

\n
$$
\mathcal{V} \rightarrow \mathcal{V}^* \simeq \mathcal{L},
$$

\n
$$
\mathcal{F} \rightarrow \mathcal{L}^* \simeq \mathcal{V}.
$$

\n(4.1)

The table in Fig. 3 illustrates the transformation (4.1) . Informally, (4.1) swaps fluxes with charges, capacitors with inductors, and nodes with faces. Under (4.1) , the connection matrix of *G* transforms as⁸

$$
M \to M^* = -M^{\mathrm{T}}.\tag{4.2}
$$

Therefore, the Lagrangian in (2.21) transforms as

$$
L \to L^* = \sum_{l,v} q_l^* M_{fv}^* \dot{\phi}_v^* - \sum_{e \in C^*} E_e^C \left(\sum_l q_l^* B_{fe}^* \right)
$$

$$
- \sum_{e \in \mathcal{I}^*} E_e^L \left(\sum_v A_{ev}^* \phi_v^* \right)
$$
(4.3)

FIG. 3. A number of examples showing how the transformation (4.1) affects various aspects of a circuit. We emphasize that from the perspective of this formalism, nonlinear inductors may be treated simply as inductors on equal footing with linear inductors. In particular, a Josephson junction would be dual to a quantum phase slip.

or

$$
L^* = \sum_{l,v} q'_v M_{vl} \dot{\phi}'_l - \sum_{e \in \mathcal{I}} E_e^C \left(\sum_{l \in \mathcal{V}^*} A_{el} \phi'_l \right)
$$

$$
- \sum_{e \in \mathcal{C}} E_e^L \left(\sum_{v \in \mathcal{F}^*} q'_v B_{ve} \right), \tag{4.4}
$$

where we have integrated the first term by parts after carrying out the substitutions in (4.1).

It appears from (4.1) that duality is an involution (operation that squares to the identity) on phase space. However, we emphasize that this interpretation can be subtle when the phase space is not equivalent to \mathbb{R}^{2n} . The most common scenario relevant for superconducting circuits is, as discussed before, the case where some of the coordinates are periodic. In particular, if the classical phase space where a conjugate pair (Q, Φ) lives is $\mathbb{R} \times S^1$, then the phase space associated with the dual conjugate pair (Φ^*, Q^*) is $S^1 \times \mathbb{R}$. Physically, this means that a quantum Hamiltonian with a compact flux variable Φ and integer valued conjugate Q has a dual with a compact charge variable Φ^* and an integer valued flux Q^* . We conclude that in this example, duality maps one phase space to another.

The nontrivial question is whether *L*[∗] can be interpreted as the Lagrangian for an *actual circuit*, where q_l^* represent physical loop charges and ϕ_v^* represent physical node fluxes. We address this for the remainder of the section.

⁷In the literature, it is sometimes said that any Lagrangian involving charges defined on a loop is called a "loop-charge Lagrangian."

⁸We remark that *X*[∗] is the dual of some object *X* under the transformation (4.1) and not, for example, complex conjugation.

FIG. 4. The black circuits in (a) and (b) are simply redrawings of the same circuit. The duals of the circuits (a) and (b) are drawn in gray. In both subfigures, labels correspond to the circuit in black.

A. Planar circuits

One way to understand the subtlety of this duality transformation is to ask whether it behaves "nicely" on the *drawings* of a circuit. In other words, does *L*[∗] describe a physical circuit that we can easily draw? In what follows, we will assume that capacitances and inductances have the same units or, equivalently, that charges and fluxes have the same units. This is a matter of convenience that can be adapted to a physical system by making suitable variable redefinitions. The discussion in this section only applies to planar circuits, and in the next section we will discuss the problems that may arise for nonplanar circuits.

The procedure for constructing the dual of a given circuit *G* is as follows [\[20,22\]](#page-19-0):

(1) Draw *G* on a plane (or, equivalently, a sphere, by identifying points at infinite distance on the plane with a single point).

(2) For every face l in *G*, draw a node inside the *l* labeled *l* ∗.

(3) Every branch *e* in *G* lies on the boundary of exactly two faces, say l_1 and l_2 . If *e* is capacitive (inductive), draw an inductive (capacitive) branch labeled e^* connecting l_1^* and l_2^* .

An example of this drawing procedure is given in Fig. 4.

We remark that *B*, the orientation matrix of *G*, depends upon how *G* is drawn. Since the incidence matrix of the dual of *G* is the transpose of *B*, it follows that a single circuit can have multiple dual circuits. Since *G*'s incidence matrix is uniquely defined, all duals of *G* have the same orientation matrix, and the number of duals of *G* with distinct incidence matrices is exactly the number of drawings of *G* with different orientation matrices. For example, in Fig. 4(b), the dual of *G* has a node of degree six, while the dual of *G* in Fig. $4(a)$ has no such vertex. In this way, we can see that circuits need not have a unique dual. A detailed discussion of this circuit is given in Sec. [V A.](#page-9-0)

The manner in which incidence and orientation matrices are "exchanged" under duality can be interpreted in the following way: the combinatorial information of a graph is encoded in the topological information of its dual, and the topological information of a graph determines the

combinatorial information in its dual. In this way, it is sensible to say that for graphs (and thus circuits), topology is dual to combinatorics.

B. Nonplanar circuits

The transformation (4.1) is the most natural candidate for a duality transformation at the Lagrangian level. Unfortunately, as we now discuss, for nonplanar circuits it is not generally clear how to construct a physical circuit for which *L*[∗] is its Lagrangian. The difficulty in constructing the dual to a nonplanar circuit arises when attempting to draw the dual circuit, rather than when trying to produce the dual Lagrangian.

For planar graphs, it is possible to choose a suitable set of loops $\mathcal L$ by drawing the circuit in question on a surface (namely, the plane), and such circuits can be made to have the property that

$$
\sum_{l} B_{l e} = 0. \tag{4.5}
$$

The importance of this property is that every edge in the circuit participates in precisely two loops within \mathcal{L} . On the other hand, for all circuits, including nonplanar ones, we demand

$$
\sum_{v} A_{ev} = 0. \tag{4.6}
$$

The duality transformation [\(4.1\)](#page-7-0) sends

$$
B \to B^* = A^{\mathrm{T}},
$$

\n
$$
A \to A^* = B^{\mathrm{T}}.
$$
\n(4.7)

If

$$
\sum_{l \in \mathcal{L}} B_{le} \neq 0, \tag{4.8}
$$

then $A^* = B^T$ is *not a valid incidence matrix*. The reason for this is the 2 g "topological loops" that must be included in $\mathcal L$ in order to fully specify all of the currents in the nonplanar circuit of interest. See Fig. [5](#page-9-0) for a drawing of a circuit with topological loops chosen and emphasized with color coding. Consider some edge *e* that participates in a topological loop l_t . *e* also lies on the boundary of a pair of faces, say l_1 and l_2 .

⁹Recall that there are no loops that cannot be drawn as faces for a planar graph.

FIG. 5. A circuit on K_5 . The edges with alike labels are to be identified. The loops l_6 and l_7 are drawn in red and blue, respectively.

Then,

$$
\sum_{l} B_{l e} = B_{l_{l} e} + B_{l_{1} e} + B_{l_{2} e} = B_{l_{l} e} \neq 0. \tag{4.9}
$$

Thus, if one attempted to interpret B^T as an incidence matrix, the edge *e* would "connect" three vertices, rather than two, but then the resulting construction is not an edge. From a mathematical perspective, it is no issue to acknowledge that an edge in a graph participates in many cycles, but there is no sensible notion of an edge that connects many vertices.

Moreover, any notion of graph duality must conserve *g*, the genus of the surface of embedding. We see, however, that

$$
B \to B^* = A^{\mathrm{T}} \tag{4.10}
$$

gives rise to *B*[∗] that *does* have the property that

$$
\sum_{l} B_{le}^{*} = 0, \tag{4.11}
$$

which is a hallmark property of planar graphs in the sense that (4.11) holds for and only for planar graphs.

Hence, there exist nonplanar circuits with no physical dual. We remark that (4.1) is still perfectly well defined for nonplanar circuits, but that it may not be possible to draw a circuit that gives rise to the resulting Hamiltonian. It may be possible that one can always introduce auxiliary degrees of freedom and integrate them out, such that *L*[∗] is the reduced description of a circuit with (nonlinear) capacitive loops or inductive cuts, but we have not found an elegant and fully general construction which allows us to construct an honest circuit dual for a general nonplanar circuit. Resolving this question seems to us to be an important open problem.

While the problem of constructing nonplanar circuits is not a central subject in this paper, we would be remiss not to briefly remark on the challenges therein. Nonplanar

graphs all contain some number of copies of K_5 or $K_{3,3}$ as subgraphs or minors.¹⁰ A notable property of these graphs, which are necessary ingredients in nonplanarity, is that removing any edge from either K_5 or $K_{3,3}$ gives rise to a planar graph. Thus, for example, a circuit on K_5 could be constructed by placing all but one circuit element on a single layer, and the remaining circuit element could be placed on a second layer connected to the first. That is to say that the construction of at least some nonplanar circuits seems reasonable in principle, provided that multilayer fabrication is possible.

V. EXAMPLES

In what follows, we will solve a number of examples that are either particularly pedagogical or of particular interest.

A. A planar circuit

Consider the black circuit drawn in Fig. $4(a)$, which we will call *G*. The face in the dual of *G* (drawn in gray) corresponding to the vertex v_i in *G* will be labeled v_i^* . We will refer to the gray circuit as *G*[∗]. The capacitance (inductance) of the circuit on element e_i will be denoted as C_i (L_i). We suppose, for the sake of simplicity in the presentation, that all circuit elements are linear, but we emphasize that this is unnecessary. We will begin by analyzing *G*.

To start,

$$
A = \begin{pmatrix} v_1 & v_2 & v_3 & v_4 & v_5 & v_6 \ 0 & -1 & 1 & 0 & 0 & 0 \ 1 & 0 & 0 & -1 & 0 & 0 \ -1 & 0 & 0 & 0 & 1 & 0 \ 0 & -1 & 0 & 0 & 0 & 1 \ -1 & 1 & 0 & 0 & 0 & 0 \ 0 & 0 & -1 & 1 & 0 & 0 \ 0 & 0 & 1 & 0 & 0 & -1 \ 0 & 0 & 0 & 1 & -1 & 0 \end{pmatrix} \begin{pmatrix} v_1 & v_2 & v_3 & v_4 & v_5 \ e_2 & v_1 & v_2 & v_6 \ e_3 & v_2 & v_4 & v_6 \ e_4 & v_3 & v_4 & v_6 \ e_5 & v_4 & v_5 & v_6 \ e_6 & v_5 & v_6 & v_7 \end{pmatrix}
$$

and

$$
B = \begin{pmatrix} e_1 & e_2 & e_3 & e_4 & e_5 & e_6 & e_7 & e_8 \\ 0 & -1 & 0 & 0 & 0 & 0 & -1 \\ -1 & 0 & 1 & 0 & -1 & 0 & 1 \\ 1 & 0 & 0 & -1 & 0 & 0 & -1 & 0 \\ 0 & 1 & 0 & 1 & 1 & 1 & 0 \end{pmatrix} \begin{matrix} l_1 \\ l_2 \\ l_3 \\ l_4 \end{matrix}
$$
 (5.2)

and thus

$$
M = \begin{pmatrix} v_1 & v_2 & v_3 & v_4 & v_5 & v_6 \ 0 & 0 & 0 & -1 & 1 & 0 \ 1 & -1 & 1 & 0 & -1 & 0 \ 0 & 0 & -1 & 0 & 0 & 1 \ -1 & 1 & 0 & 1 & 0 & -1 \end{pmatrix} \begin{matrix} l_1 \\ l_2 \\ l_3 \\ l_4 \end{matrix}
$$
 (5.3)

 $10K_5$ is the fully connected graph on five vertices, and $K_{3,3}$ is the complete bipartite graph on six vertices.

Now, the Lagrangian for *G* is given by

$$
L = (q_4 - q_2)(\dot{\phi}_{v_2} - \dot{\phi}_{v_1}) + (q_2 - q_1)(\dot{\phi}_{v_4} - \dot{\phi}_{v_5})
$$

+ $(q_4 - q_3)(\dot{\phi}_{v_3} - \dot{\phi}_{v_6}) + (q_4 - q_2)(\dot{\phi}_{v_4} - \dot{\phi}_{v_3})$
- $\frac{1}{2L_1}(\phi_{v_3} - \phi_{v_2})^2 - \frac{1}{2L_2}(\phi_{v_1} - \phi_{v_4})^2 - \frac{1}{2L_3}(\phi_{v_5} - \phi_{v_1})^2$
- $\frac{1}{2L_4}(\phi_{v_6} - \phi_{v_2})^2 - \frac{1}{2C_5}(q_4 - q_2)^2 - \frac{1}{2C_6}(q_4 - q_2)^2$
- $\frac{1}{2C_7}(q_4 - q_3)^2 - \frac{1}{2C_8}(q_2 - q_1)^2.$ (5.4)

There are two right null vectors of *M*. The first corresponds to

$$
0 = \frac{\delta S}{\delta \phi_{v_2}} + \frac{\delta S}{\delta \phi_{v_3}} + \frac{\delta S}{\delta \phi_{v_6}},
$$
\n(5.5)

which contains no nontrivial constraint. The other nontrivial null vector corresponds to

$$
0 = \frac{\delta S}{\delta \phi_{v_1}} + \frac{\delta S}{\delta \phi_{v_2}}
$$

= $\frac{1}{L_1} (\phi_{v_2} - \phi_{v_3}) + \frac{1}{L_2} (\phi_{v_1} - \phi_{v_4})$
+ $\frac{1}{L_4} (\phi_{v_1} - \phi_{v_5}) + \frac{1}{L_4} (\phi_{v_2} - \phi_{v_6}).$ (5.6)

Resolving this constraint and defining

$$
Q_1 = q_4 - q_2,
$$

\n
$$
Q_2 = q_2 - q_1,
$$

\n
$$
Q_3 = q_4 - q_3,
$$

\n
$$
\Phi_1 = \phi_{\nu_2} + \phi_{\nu_4} - \phi_{\nu_1} - \phi_{\nu_3},
$$

\n
$$
\Phi_2 = \phi_{\nu_4} - \phi_{\nu_5},
$$

\n
$$
\Phi_3 = \phi_{\nu_3} - \phi_{\nu_6},
$$
\n(5.7)

we immediately find

$$
L = Q_1 \dot{\Phi}_1 + Q_2 \dot{\Phi}_2 + Q_3 \dot{\Phi}_3 - \frac{1}{2} \left(\frac{1}{C_5} + \frac{1}{C_6} \right) Q_1^2 - \frac{1}{2C_7} Q_3^2
$$

$$
- \frac{1}{2C_8} Q_2^2 - \frac{L_{\Sigma}}{2} \left[\frac{1}{L_1 L_2} \Phi_1^2 + \frac{1}{L_1 L_3} (\Phi_1 - \Phi_2)^2 + \frac{1}{L_1 L_4} \Phi_3^2 + \frac{1}{L_2 L_3} \Phi_2^2 + \frac{1}{L_2 L_4} (\Phi_1 + \Phi_3)^2 + \frac{1}{L_3 L_4} (\Phi_1 - \Phi_2 + \Phi_3)^2 \right],
$$
 (5.8)

with

$$
\frac{1}{L_{\Sigma}} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3} + \frac{1}{L_4}.
$$
 (5.9)

By taking the transformation

$$
Q_i \rightarrow Q_i^* = -\Phi_i,
$$

\n
$$
\Phi_i \rightarrow \Phi_i^* = Q_i,
$$
\n(5.10)

we can acquire the Lagrangian (and Hamiltonian) of the gray circuit drawn in Fig. [4\(a\).](#page-8-0)

We remark that the black circuit drawn in Fig. $4(b)$ is simply a different drawing of the black circuit drawn in Fig. [4\(a\),](#page-8-0)

FIG. 6. (a) The transmon. (b) The fluxonium qubit.

but the gray circuit in Fig. [4\(b\)](#page-8-0) is not even graph isomorphic to the gray circuit drawn in Fig. $4(a)$. A similarly simple analysis of the black circuit drawn in Fig. $4(b)$ would provide a canonically related Hamiltonian to the one governing *G* (of course, since the two circuits are identical). It then follows that the Hamiltonian governing the gray circuits must also be canonically related.

B. Transmon and fluxonium qubits

We now turn our attention to a pair of (formally) very similar circuits of practical interest. This pair of examples is useful in that it illustrates the "automatic" solution of a voltage constraint. We will start by considering the fluxonium qubit pictured in Fig. 6(b). The *A*, *B*, and *M* matrices may be read off of the drawing,

$$
A = \begin{pmatrix} v_1 & v_2 \\ 1 & -1 \\ 1 & -1 \end{pmatrix} \begin{matrix} e_1 \\ e_2 \\ e_3 \end{matrix}
$$

$$
B = \begin{pmatrix} e_1 & e_2 & e_3 \\ -1 & 0 & -1 \\ 1 & 1 & 0 \end{pmatrix} \begin{matrix} l_1 \\ l_2 \\ l_3 \end{matrix}
$$

$$
M = \begin{pmatrix} v_1 & v_2 \\ 1 & -1 \\ -1 & 1 \end{pmatrix} \begin{matrix} l_1 \\ l_2 \\ l_3 \end{matrix}
$$
(5.11)

Thus, the Lagrangian describing the fluxonium qubit is

$$
L_{\text{fluxonium}} = (q_{l_2} - q_{l_3})(\dot{\phi}_{v_1} - \dot{\phi}_{v_2}) - \frac{1}{2C}(q_{l_2} - q_{l_3})^2
$$

$$
-\frac{1}{2L}(\phi_{v_1} - \phi_{v_2})^2 + E_J \cos(\phi_{v_1} - \phi_{v_2}). \quad (5.12)
$$

After making the definitions

$$
\Phi = \phi_{v_1} - \phi_{v_2},
$$

\n
$$
Q = q_{l_2} - q_{l_3},
$$
\n(5.13)

we see that the (classical) Hamiltonian for the fluxonium qubit is

$$
H_{\text{fluxonium}} = \frac{1}{2C}Q^2 + \frac{1}{2L}\Phi^2 - E_J\cos(\Phi). \tag{5.14}
$$

Now, for the transmon qubit,

$$
M_{\text{transmon}} = \begin{pmatrix} v_1 & v_2 \\ 1 & -1 \\ -1 & 1 \end{pmatrix} l_1
$$
 (5.15)

Notice that *M*_{transmon} appears as a submatrix of *M* in [\(5.11\)](#page-10-0). This can be understood as a consequence of the fact that Kirchhoff's voltage rule demands that the flux across the linear inductor and Josephson junction in fluxonium must be equal (up to a constant of integration that we set to zero). It is straightforward to produce

$$
H_{\text{transmon}} = \frac{1}{2C}Q^2 - E_J \cos(\Phi). \tag{5.16}
$$

There is a subtlety regarding the process of quantizing [\(5.14\)](#page-10-0) and (5.16) after arriving at a classical Hamiltonian. Namely, $H_{\text{fluxonium}}$ is not invariant under translation of Φ by any nonzero constant. In other words, $H_{\text{fluxonium}}$ is inconsistent with a periodically identified "compact" Φ variable. To contrast this observation, it is thought that Φ as it appears in *H*transmon is a compact variable.

While it is true that the question of how the topology of phase space affects quantization is not the subject of this paper, we remark that phase space in the fluxonium case is isomorphic (equivalent) to \mathbb{R}^2 , while it may be the case that the classical phase space in the transmon case is $\mathbb{R} \times S^1$. The dual of the fluxonium qubit likewise must have classical phase space \mathbb{R}^2 , and the dual of the transmon has an equivalent phase space to that of the original transmon (albeit the periodically identified variable changes physical interpretation from flux to charge).

C. A self-dual circuit

Consider the circuit drawn in Fig. [2.](#page-3-0) The Hamiltonian that is produced is given by

$$
H(Q, \Phi) = \frac{1}{3C} (Q_1^2 - Q_1 Q_2 + Q_2^2)
$$

+
$$
\frac{1}{3L} (\Phi_1^2 - \Phi_1 \Phi_2 + \Phi_2^2).
$$
 (5.17)

It is obvious that $H(-\Phi, Q) = H(Q, \Phi)$ provided that we choose units where $C = L$, which is to say that the circuit drawn in Fig. [2](#page-3-0) is, or at least *has*, a self-dual drawing.

D. A circuit on K_5

For the purposes of this example, we will focus on the circuit drawn in Fig. [5,](#page-9-0) which will again be called *G*. The drawing at hand is slightly unconventional since it is drawn on a polygon with the boundaries identified (which is typical in mathematical descriptions of a torus, for example). For the sake of simplicity, we will suppose that all inductances take on a value *L* and all capacitances take on a value *C*.

First, we must compute the relevant *A*, *B*, and *M* matrices:

$$
A = \begin{pmatrix} v_1 & v_2 & v_3 & v_4 & v_5 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & -1 & 1 \\ 1 & 0 & 0 & 0 & -1 \\ -1 & 1 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 0 \\ 1 & 0 & -1 & 0 & 1 \\ 0 & 0 & -1 & 0 & 1 \\ 0 & 1 & 0 & 0 & -1 \\ 0 & 0 & 1 & 0 & 0 \end{pmatrix} \begin{matrix} e_1 \\ e_2 \\ e_3 \\ e_4 \\ e_5 \\ e_6 \\ e_7 \\ e_8 \\ 0 & -1 & 0 & 1 \\ 0 & 0 & -1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 \end{matrix}
$$

$$
B = \begin{pmatrix}\ne_1 & e_2 & e_3 & e_4 & e_5 & e_6 & e_7 & e_8 & e_9 & e_{10} \\
0 & 0 & 0 & 0 & 0 & -1 & -1 & -1 & -1 \\
1 & 1 & 0 & -1 & 0 & 0 & 0 & 1 & 0 & 0 \\
-1 & 0 & 0 & 0 & -1 & -1 & 0 & 0 & 1 & 0 \\
0 & 0 & 1 & 1 & 1 & 0 & 1 & 0 & 0 & 0 \\
0 & -1 & -1 & 0 & 0 & 1 & 0 & 0 & 0 & 1 \\
1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 0\n\end{pmatrix}\n\begin{matrix}\n\downarrow_1 \\
I_2 \\
I_3 \\
I_4 \\
I_5 \\
I_6 \\
I_7 \\
I_8\n\end{matrix}
$$
\n
$$
M = \begin{pmatrix}\n0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0\n\end{pmatrix}\n\begin{matrix}\nI_1 \\
I_2 \\
I_3 \\
I_4 \\
I_5 \\
I_6 \\
I_7\n\end{matrix}
$$
\n(5.18)

Thus,

$$
L = (q_{l_3} - q_{l_2})(\dot{\phi}_{v_2} - \dot{\phi}_{v_5}) + (q_{l_4} - q_{l_5})(\dot{\phi}_{v_3} - \dot{\phi}_{v_5})
$$

+ $(q_{l_5} - q_{l_3})(\dot{\phi}_{v_4} - \dot{\phi}_{v_5}) - \frac{1}{2C}[(q_{l_2} - q_{l_3} + q_{l_6})^2$
+ $(q_{l_2} - q_{l_5} + q_{l_6})^2 + (q_{l_4} - q_{l_5} + q_{l_6})^2]$
- $\frac{1}{2C}[(q_{l_4} - q_{l_2} + q_{l_7})^2 + (q_{l_4} - q_{l_3} + q_{l_7})^2$
+ $(q_{l_5} - q_{l_3} + q_{l_7})^2] - \frac{1}{2L}[(\phi_{v_5} - \phi_{v_3})^2 + (\phi_{v_2} - \phi_{v_5})^2$
+ $(\phi_{v_4} - \phi_{v_2})^2 + (\phi_{v_4} - \phi_{v_3})^2].$ (5.19)

Choosing the variables

$$
Q_1 = q_{l_3} - q_{l_2},
$$

\n
$$
Q_2 = q_{l_4} - q_{l_5},
$$

\n
$$
Q_3 = q_{l_5} - q_{l_3},
$$

\n
$$
\Phi_1 = \phi_{v_2} - \phi_{v_5},
$$

\n
$$
\Phi_2 = \phi_{v_3} - \phi_{v_5},
$$

\n
$$
\Phi_3 = \phi_{v_4} - \phi_{v_5},
$$
\n(5.20)

we can rewrite

$$
L = \sum_{i=1}^{3} Q_i \dot{\Phi}_i - \frac{1}{2C} [(q_{l_6} - Q_1)^2 + (q_{l_6} - Q_1 - Q_3)^2
$$

+ $(Q_2 + q_{l_6})^2$] $-\frac{1}{2C} [(q_{l_7} + Q_1 + Q_2 + Q_3)^2$
+ $(q_{l_7} + Q_2 + Q_3)^2 + (q_{l_7} + Q_3)^2]$
- $\frac{1}{2L} [\Phi_2^2 + \Phi_1^2 + (\Phi_3 - \Phi_1)^2 + (\Phi_2 - \Phi_3)^2]$. (5.21)

From (5.21), it is clear to see that q_{l_6} and q_{l_7} are constrained in terms of *Q* variables as a result of

$$
0 = \frac{\delta S}{\delta q_{l_6}} = \frac{\delta S}{\delta q_{l_7}}.\tag{5.22}
$$

After using (5.22), we find

$$
q_{l_6} = \frac{1}{3}(2Q_1 - Q_2 + Q_3),
$$

\n
$$
q_{l_7} = \frac{1}{3}(-Q_1 - 2Q_2 - 3Q_3).
$$
\n(5.23)

Then, the Hamiltonian describing *G* is given by $H(Q_1, Q_2, Q_3, \Phi_1, \Phi_2, \Phi_3) = \sum_{i=1}^3 Q_i \dot{\Phi}_i - L$. The Poisson brackets of the system at hand are

$$
\{\Phi_i, Q_j\} = \delta_{ij}.\tag{5.24}
$$

One may find it peculiar that the "topological loops" q_{l_6} and q_l are nondynamical in the sense that they are not independent of loops on the surface of the torus. This is no accident. Indeed, for circuits on the fully connected graph on*V* vertices, K_V , there are $\binom{V}{2}$ edges and there must be at least 2*g* loops made of only capacitors or only inductors. To see how this is true, observe that the number of independent loops in a circuit *G* with *E* edges and *V* vertices is at least

No. loops
$$
\ge n(E, V) = \max(E - V + 1, 0).
$$
 (5.25)

We emphasize that this bound on $n(E, V)$ holds even for graphs that are not connected. Now, suppose the number of capacitors in a circuit is N_C , while the number of inductors is N_I . There exists a pair of graphs G_C and G_I that consist of all vertices from *G* and only the capacitive edges or inductive edges, respectively. The number of inductive (capacitive) loops in G_I [G_C] is then at least $n(N_I, V)$ [$n(N_C, V)$]. Since *GC* and *GI* are subgraphs of *G*, it follows that the number of homogenous loops in *G* is at least $n(N_I, V) + n(N_C, V)$. Moreover, it must be the case that $N_I + N_C = E$. Thus, we have that the number of homogenous loops in *G* is bounded below by

$$
N_l = n(N_l, V) + n(N_C, V) = n(E - N_C, V) + n(N_C, V).
$$
\n(5.26)

Now, for fully connected graphs K_V , $E = \binom{V}{2}$, so a circuit on K_V with N_C capacitors has

$$
N_l = n \left[\binom{V}{2} - N_C, V \right] + n(N_C, V) \geqslant 2g \tag{5.27}
$$

since

$$
\min_{x} \left\{ \max \left[\binom{V}{2} - x - V + 1, 0 \right] + \max \left(x - V + 1, 0 \right) \right\}
$$

\n
$$
\geq 2g. \tag{5.28}
$$

In a few words, a fully connected graph on *V* vertices can always be drawn on a *g*-holed torus in such a way that all 2*g* topological loops are null vectors of *M*. It is, in principle, always possible to synthesize some planar circuit with the same dynamics as a given circuit on *K*5.

While it is generally impossible to construct a dual circuit for a nonplanar circuit, it is nonetheless sometimes possible to do something similar. In particular, it is sometimes possible to reduce a nonplanar circuit to an effectively planar circuit by using constraints that follow from Kirchoff's rules (e.g., by adding inductors or capacitors in series or parallel or by using the delta-wye transform $[31]$). One way to accomplish this goal is to arrange circuit elements such that the edges lying on a given topological loop contain either all capacitors or all inductors (so that the relevant loop degree of freedom is nondynamical). Then, one can produce a simplified equivalent circuit with fewer edges (by using Kirchoff's rules) than the original. If the simplified circuit is planar then it has a well defined dual. In some sense, the resulting dual serves as what would be the dual of the nonplanar circuit. Whether or not this planarization may be carried out apparently depends on whether or not there exist at least 2*g* homogenous loops in a circuit. We mention in passing that no similar result holds for circuits on, say, $K_{3,3}$. From this, we suspect that the most interesting nonplanar circuits are likely to be those that are most sparsely connected.

VI. CONCLUSIONS

In this paper, we have derived a Lagrangian description of circuits that treats fluxes and charges on an equal footing, extending our previous work [\[16\]](#page-19-0) towards a more general theory of circuit quantization. Existing methods can be shown to be equivalent to our formalism. A key feature of this "flux-charge symmetric" formulation of circuit mechanics is that circuit duality becomes a simple relabeling transformation, for planar circuits.

For nonplanar circuits, it is not always obvious if a dual circuit is physical. An interesting future research direction is to understand whether it is possible to add *additional* circuit elements such that the dual of a general nonplanar circuit is well defined.

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APPENDIX A: GRAPH THEORY

Where possible, the demonstrations in this Appendix will follow [\[16\]](#page-19-0) as closely as possible.

Definition A1 (Graph). Take a set V and let $\mathcal E$ be the set of ordered pairs of elements of V. We say that $G = (V, \mathcal{E})$ is a (directed) *graph*.

In all of what follows, we will assume that graphs and structures built upon graphs are connected. This assumption will not henceforth be stated, but we remark that it is not required by every result that we prove.

Definition A2 (Embedding). Let $G = (\mathcal{V}, \mathcal{E})$ be a graph. Choose a two-dimensional orientable surface *S* and associate one (distinct) point in *S* for every element of V : crudely, we can think of $V \subset S$. Every edge $e = (u, v) \in \mathcal{E}$ corresponds to a smooth map $e : [0, 1] \rightarrow S$ such that $e(0) = u$ and $e(1) = v$. Assuming that for $x, x' \in (0, 1)$, $e(x) \neq e(x')$ (i.e., no two lines ever cross), *S* is partitioned into a set of surfaces. If such a drawing exists, we call it an *embedding* of *G* on *S*, or simply an embedding of *G*.

A single graph can have many embeddings. The combinatorial information in *G* is independent of the manner in which it is embedded. If a graph *G* can be embedded upon a surface *S* at all, it is always possible to draw some embedding of *G* on *S* such that the surface *S* is partitioned into regions that are isomorphic to the unit disk, though we remark that Definition A2 does not require this property. Nonetheless, these "nice" embeddings will be the subject of our discussion.

Definition A3 (Face). In an embedding of *G* on *S*, each "patch" topologically equivalent to the unit disk is a *face*. For two faces f_1 and f_2 and edge e of G embedded on S , we write $f_1 \leftrightarrow ef_2$ to mean that *e* is an edge on the common boundary of the disk corresponding to f_1 and the disk corresponding to *f*2.

A graph *G* is a purely combinatorial object. We emphasize that while there is a universal notion of topology in the one-dimensional setting, the topology of the embedding is nonuniversal. Perhaps surprisingly, at first glance, even the subsets of edges in E which correspond to the boundaries of faces in an embedding are not unique and can depend on the choice of embedding. As we will see in later discussion, these ambiguities certainly will have no physical consequences in circuit quantization, although they can surprisingly lead to different looking Lagrangians or Hamiltonians at first glance.

Definition A4 (Loop). Let $G = (V, E)$ be a graph. For the purposes of this definition, we regard $e = (u, v)$ and $e' =$ (*v*, *u*) as equivalent. A *loop* γ is a subset $\gamma \subset \mathcal{E}$, so that (properly orienting each edge)

$$
\gamma = \{ (v_0, v_1), (v_1, v_2), \dots, (v_{n-1}, v_n), (v_n, v_0) \}. \qquad (A1)
$$

We say that γ is of length *n* if $|\gamma| = n$.

Every face's boundary is a loop, so there is a natural injection from the set of faces to the set of loops.

Definition A5 (Linearly independent loops). Let $G =$ (V, \mathcal{E}) be a graph. Let $\Gamma = {\gamma_1, \gamma_2, ..., \gamma_n}$ be a set of *n* loops in *G*. We say that the set Γ is linearly dependent if there exists $m \in \{1, \ldots, n\}$ and set $\iota = \{i_1, i_2, \ldots, i_p\} \subset$ $\{1, 2, 3, ..., n\} \setminus \{m\}$, such that

$$
\gamma_m = \gamma_{i_1} \Delta \gamma_{i_2} \Delta \dots \Delta \gamma_{i_p}, \qquad (A2)
$$

where

$$
A \Delta B = (A \cup B) \setminus (A \cap B). \tag{A3}
$$

Otherwise, we say that the loops in Γ are *linearly independent*. We say that the rank of a set of loops Γ is the number of linearly independent loops in Γ.

Definition A6 (Cut). Let $G = (V, \mathcal{E})$ be a graph. Partition V into *m* sets V_i with $i = 1, 2, 3, \ldots, m$, so that

$$
\mathcal{V} = \bigcup_{i=1}^{m} \mathcal{V}_i
$$
 (A4)

and

$$
\emptyset = \mathcal{V}_i \cap \mathcal{V}_j,\tag{A5}
$$

for $i \neq j$. Such a partition $(\mathcal{V}_1, \mathcal{V}_2, \mathcal{V}_3, \dots, \mathcal{V}_m)$ of V is called a *cut* of *G*.

Definition A7 (Edge cut). Let $G = (\mathcal{V}, \mathcal{E})$ be a graph. Let (V_1, V_2, \ldots, V_m) be a cut of *G*. Define the set $K \subset \mathcal{E}$ such that

 $K = \{(u, v) \in \mathcal{E} \text{ such that } \exists i \text{ such that } \{u, v\} \subset V_i\}.$ (A6) The set $\mathcal{E} \setminus \mathcal{K}$ is called the *edge cut* of *G* induced by $(\mathcal{V}_1, \mathcal{V}_2, \ldots, \mathcal{V}_m)$.

The notions of a cut and an edge cut are formally equivalent and every result of this manuscript may be stated and proven favoring one notion over the other. Nonetheless, it is useful to possess an understanding of both conventions since some ideas are easier to understand in terms of cuts and others are easier to understand in terms of edge cuts.

Definition A8 (Genus). Let $G = (V, E)$ be a graph. We say that *G* has genus *g* if there exists no embedding of *G* on any surface *S* of topological genus $g' < g$. This is not the same definition as the usual graph genus from graph theory.

Definition A9 (Embedded graph). Let *G* be a graph and *S* an orientable surface. Suppose that there exists some embedding of *G* on *S*, i.e., on a sphere with *g* holes. Under this embedding, denote the set of faces of *G* embedded in *S* as F. We write $G_S = (\mathcal{V}, \mathcal{E}, \mathcal{F})$ to be the *embedded graph* G on S.

In much of what follows, we will suppress some of the above-defined terminology when either the embedding of *G* on *S* is of no consequence or when the embedding of *G* on *S* is clear from context. In such cases, we will write $G = (\mathcal{V}, \mathcal{E}, \mathcal{F})$ and we will refer to *G* simply as a graph.

Theorem A1. Let $G = (V, \mathcal{E}, \mathcal{F})$ be an embedded graph. Denote the loop on the boundary of the face f_i as γ_i . If *G* is connected, the set

$$
\Gamma = \{ \gamma_1, \gamma_2, \dots, \gamma_{|\mathcal{F}|} \}
$$
 (A7)

is linearly dependent and the set $\Gamma \setminus {\gamma_1}$ is linearly independent.

Proof. Every edge in *G* appears on the boundary of precisely two faces, so $\gamma_1 = \gamma_2 \Delta \gamma_3 \Delta \ldots \Delta \gamma_{|\mathcal{F}|}$. For any γ_j obeying $\gamma_1 \cap \gamma_j \neq \emptyset$, γ_j is linearly independent of the rest since every edge appears in no other face. Removing such γ_i , we can inductively deduce the linear independence of the remaining γ 's since the graph is connected.

The following two important, and classic, results, are stated without proof:

Theorem A2 (Euler's formula). Let $G = (\mathcal{V}, \mathcal{E})$ and suppose that *G* has genus *g*. Let *S* be a compact, orientable discretization of a Riemann surface of genus *g*. For any embedding of *G* on *S*, we have

$$
|\mathcal{V}| - |\mathcal{E}| + |\mathcal{F}| = 2 - 2g.
$$
 (A8)

Corollary A1. Let $G = (V, \mathcal{E})$ be a graph and let Γ be a linearly independent set of loops in *G*. Then,

$$
|\Gamma| \le g_G = |\mathcal{E}| - |\mathcal{V}| + 1. \tag{A9}
$$

In effect, Corollary $A1$ serves to indicate that for nonplanar graphs, it is possible to construct a linearly independent set of loops that is greater in size than the set of faces of a graph. As we will see, this fact is crucial to our discussion of circuit dualities for nonplanar graphs.

Theorem A3. Let $G = (V, \mathcal{E}, \mathcal{F})$ be an embedded, nonplanar graph with genus $g > 0$. There exist 2*g* loops that are independent of all of the loops bounding faces f in \mathcal{F} .

Proof. By Theorem [A2,](#page-13-0)

$$
|\mathcal{F}| + 2g = g_G + 1. \tag{A10}
$$

As we have seen in Theorem $A1$, the set of loops bounding faces in F is $|\mathcal{F}| - 1$, and Corollary A1 tells us that it is possible to construct a set of loops of rank *gG*. -

Definition A10 (Loop set). Let $G = (V, \mathcal{E}, \mathcal{F})$ be an embedded graph of genus *g*. Choose 2*g* loops independent of all loops at the boundary of some face in \mathcal{F} , say, l_1, \ldots, l_{2g} . Denote the loop at the boundary of f_i in $\mathcal F$ as l_{2g+i} . The set

$$
\mathcal{L} = \{l_1, l_2, \dots, l_{2g+|\mathcal{F}|}\}\tag{A11}
$$

is called the *loop set* of *G*.

Definition A11 (Extended embedded graph). Let $G =$ $(V, \mathcal{E}, \mathcal{F})$ be an embedded graph and let \mathcal{L} be the loop set of *G*. The object $G' = (\mathcal{V}, \mathcal{E}, \mathcal{L})$ is called an *extended embedded graph*.

Definition A12 (Planar graph). A graph *G* is *planar* if it has genus $g = 0$.

We remark that for planar graphs, $\mathcal{F} = \mathcal{L}$.

Planar graph theory is well studied. In the circuit literature, many formal results are limited to planar graphs in consideration because such circuits are both simpler to draw and analyze, let alone build in experiment. Note that according to Definition $A2$, a plane is not a suitable surface on which to embed a graph because the "external face" cannot be isomorphic to a unit disk. This problem is resolved by considering the embedding of a planar graph on a sphere or, equivalently, by identifying the points at infinity to be equivalent. Of course, in practice, we will draw planar graphs in the plane since the plane is equivalent to the sphere if we identify all points at spatial infinity with the same point. So, henceforth, we will consider planar graphs to be embedded on the unit sphere.

Nonplanar graphs have genus $g > 0$, by definition. They do have much in common with planar graphs, once we find the right perspective. To talk about graph duality, it is necessary to specify surfaces on which we consider embedding the graph. Generally, for a graph of genus *g*, we elect to embed upon a "sphere with *g* handles" or, equivalently, a "torus with *g* holes."

Definition A13 (Chains). Let *X* be a finite set. For every $x \in X$, define a real vector $|x\rangle$ and define

$$
\mathcal{D}(X) = \text{span}(\{|x| : x \in X\}).\tag{A12}
$$

We say that $D(X)$ is the *set of chains* over X, and we say that $|x\rangle$ is a chain.

Definition A14 (Incidence matrix). Let $G = (\mathcal{V}, \mathcal{E})$ be a directed graph. Define the linear map $A: \mathcal{D}(\mathcal{V}) \to \mathcal{D}(\mathcal{E})$ so that

$$
\langle e|A|v\rangle = \begin{cases} 1, & e \text{ is incident upon } v \\ -1, & e \text{ leaves } v \\ 0, & \text{otherwise.} \end{cases}
$$
 (A13)

We say that *A* is the *incidence matrix* of *G* and we often write $\langle e|A|v\rangle = A_{ev}.$

Definition A15 (Orientation matrix). Let $G = (V, \mathcal{E}, \mathcal{L})$ be an extended embedded graph. Orient all faces of *G* alike.¹¹ Choose some orientation for the 2 g loops in $\mathcal L$ that does not bound a face of *G*. Define the linear map $B : \mathcal{D}(\mathcal{E}) \to \mathcal{D}(\mathcal{L})$ so that

$$
\langle l|B|e\rangle = \begin{cases} 1, & e \text{ borders } l \text{ and } e \text{ is oriented with } l \\ -1, & e \text{ borders } l \text{ and } e \text{ is oriented against } l \\ 0, & \text{otherwise.} \end{cases}
$$
\n(A14)

We say that *B* is the *orientation matrix* of *G*.

An abstract graph *G* has a unique incidence matrix *A*, but not necessarily a unique orientation matrix *B*. On the other hand, an extended embedded graph on a surface S , G_S , has both a unique *A* and a unique *B*.

Theorem A4. Let *G* be an extended embedded graph with incidence matrix *A* and orientation matrix *B*. The rank of *A* is $|\mathcal{V}| - 1$ and the rank of *B* is $|\mathcal{L}| - 1$.

Proof. Suppose

$$
\sum_{v} A_{ev} c_v = 0, \tag{A15}
$$

with c_v in $\mathbb{R}^{|\mathcal{V}|} \setminus \{0\}$. Then, there exists at least v such that c_v is nonzero, and if A_{ev} is nonzero, then there exists *u* so that $e = (u, v)$ or $e = (v, u)$. In either case, $A_{ev} = -A_{eu}$ and thus $c_u = c_v$. Continue in this way to discover that $c_v = 1$ for all $v \in V$. The proof that the only left null vector of *B* is given by $c_f = 1$ for all $f \in \mathcal{F}$ is exactly analogous. We remark that $\mathcal{F} \neq \mathcal{L}$ in general; hence the left null vector of *B* corresponds to a sum over loops bounding faces only (see Theorem $A1$).

Theorem A5. If *G* is an extended embedded graph with incidence matrix *A* and orientation matrix *B*,

$$
\sum_{e \in \mathcal{E}} B_{le} A_{ev} = 0. \tag{A16}
$$

Proof. This fact is an elementary result in the theory of CW complexes.¹² Nonetheless, we provide an explicit demonstration. Choose a loop l and a vertex v . If v is not connected to any edges in *l*, the result is trivial, so suppose that there exist edges *e* and e' in¹³ *l* and vertices u_1 and u_2 so that one of the following possibilities holds:

(i)
$$
e = (u_1, v)
$$
 and $e' = (v, u_2)$,

(ii) $e = (v, u_1)$ and $e' = (v, u_2)$,

¹¹Our convention is that loops bounding faces ought to be oriented such that the right-hand rule points out of the surface.

 12 Explicitly, this is a discrete version of the statement that exterior derivatives are nilpotent.

¹³Each vertex along a loop must be hit an even number of times or the loop would not be closed. If a vertex is hit 2*m* times, then there will always exist *m* pairs of *e* and *e'* for which this argument holds.

(iii) $e = (u_1, v)$ and $e' = (u_2, v)$,

 (iv) $e = (v, u_1)$ and $e' = (u_2, v)$.

Now, in cases (i) and (iv), $B_{le} = B_{le'}$ and $A_{ev} = -A_{e'v}$. In cases (ii) and (iii), the opposite is true. In any case,

$$
B_{le}A_{ev} + B_{le'}A_{e'v} = 0.
$$
 (A17)

This concludes the proof. -

Theorem A6. Let *G* be an extended embedded graph with incidence matrix *A* and orientation matrix *B*. Then,

$$
Ker(B) = Im(A). \tag{A18}
$$

Proof. From Theorem [A5,](#page-14-0) it is clear that

$$
Im(A) \subseteq Ker(B). \tag{A19}
$$

For the other direction, note that

$$
Rank(A) = |\mathcal{V}| - 1, \tag{A20a}
$$

$$
Rank(B) = |\mathcal{L}| - 1. \tag{A20b}
$$

Since extended embedded graphs satisfy

$$
|\mathcal{V}| - |\mathcal{E}| + |\mathcal{L}| = 2, \tag{A21}
$$

we see that

dim[Ker(B)] =
$$
|\mathcal{E}|
$$
 - Rank(B) = $|\mathcal{E}|$ - $|\mathcal{L}|$ + 1 = $|\mathcal{V}|$ - 1
= Rank(A) = dim[Im(A)]. (A22)

It follows from $(A18)$ and $(A22)$ that $Ker(B)$ is spanned by elements of $Im(A)$.

Another way to state Theorem A6 is that for any vector γ in $\mathbb{R}^{|\mathcal{E}|}$ satisfying

$$
\sum_{e} B_{le} \gamma_e = 0, \tag{A23}
$$

there exists some other vector δ in $\mathbb{R}^{|\mathcal{V}|}$ such that

$$
\gamma_e = \sum_v A_{ev} \delta_v. \tag{A24}
$$

Likewise, any left null vector γ of *A* is of the form $\gamma = \delta^T B$.

Informally, *A* maps vertices (or integer linear combinations of vertices) to edge cuts of a graph *G*, and such edge cuts are precisely the null vectors of *B*. More precisely, if (V_1, V_2) is a cut of *G*, then $\langle e|A \sum_{v \in V_1} |v\rangle$ is nonzero if and only if *e* is in the edge cut induced by $(\mathcal{V}_1, \mathcal{V}_2)$. The sign may be either positive or negative and is determined by the relative orientation of the edges leaving or entering V_1 . Likewise, the matrix *B* maps cycles of *G* to linear combinations of faces of *G*. As a remark, we note that by cutting every edge in a graph, V is partitioned into singlet sets, and since the graphs of interest are also circuits, there is some sense in which the cycle consisting of all edges *is* indeed a loop. However, the vector $\sum_{e \in \mathcal{E}} |e\rangle$ is not in the range of *A*.

APPENDIX B: FORMAL APPROACH TO SYMMETRIC QUANTIZATION

In this Appendix, we more formally discuss the flux-charge symmetric theory of circuit quantization.

1. Properties of circuits and the connection matrix

In this section, we describe the full formalism for symmetric quantization on arbitrary graphs. In what follows, we consider a circuit on a planar graph with a fixed but arbitrary embedding. In analogy to graphs as combinatorial objects, we regard circuits as graphs with "colored" edges. That is to say that we demand that edges contain precisely a single circuit element and that circuit elements are either inductive or capacitive.

Definition B1 (Circuit). Let $G = (\mathcal{V}, \mathcal{E}, \mathcal{L})$ be an extended embedded graph with incidence matrix *A* and orientation matrix *B*. Partition the set $\mathcal E$ into the sets $\mathcal C$ and $\mathcal I$ such that edges housing inductors (capacitors) go into the set $\mathcal{I}(\mathcal{C})$. The tuple (V, C, I, L, A, B) is called a *circuit*.
Definition B2 (Connection

(Connection matrix). Let $G =$ (V, C, I, L, A, B) be a circuit. Define the matrix $M: \mathcal{D}(\mathcal{V}) \to \mathcal{D}(\mathcal{L})$ so that

$$
M_{lv} := \langle l | M | v \rangle = \frac{1}{2} \sum_{e \in C} B_{le} A_{ev} - \frac{1}{2} \sum_{e \in \mathcal{I}} B_{le} A_{ev}. \tag{B1}
$$

We say that *M* is the *connection matrix* of *G*.

Unlike *A* and *B*, *M* has no intuitive interpretation which can be easily read off of a circuit (at least that we have found). Still, in practice, it is straightforward to simply calculate it. Since $C \cup T = \mathcal{E}$, it follows that

$$
M = \sum_{e \in C} B_{le} A_{ev} = -\sum_{e \in \mathcal{I}} B_{le} A_{ev}.
$$
 (B2)

It will often be useful to rewrite *M* using (B2). Furthermore, for planar circuits,

$$
\sum_{l \in \mathcal{L}} M_{lv} = \sum_{v \in \mathcal{V}} M_{lv} = 0, \tag{B3}
$$

since $\sum_{v} A_{ev} = 0$ and $\sum_{l} B_{l} = 0$. For nonplanar circuits, the set of faces $\mathcal{F} \subset \mathcal{L}$ has the property that

$$
\sum_{l \in \mathcal{F}} B_{le} = 0. \tag{B4}
$$

Our first goal is to prove the following result:

Corollary B1. Let $G = (V, C, \mathcal{I}, \mathcal{L}, A, B)$ be a circuit. We say that a loop is homogenous if the edges are all capacitors or all inductors. Similarly, a cut is called homogenous if its induced edge cut consists only of inductors or only of capacitors. The following conditions hold:

(i) $M|\varphi\rangle = 0$ if and only if $(\mathcal{V}_1, \mathcal{V}_2)$ is a homogeneous cut of *G* and $|\varphi\rangle = \sum_{v \in \mathcal{V}_1} |v\rangle$.

(ii) $\langle \psi | M = 0$ if and only if γ is a homogeneous loop and $\langle \psi | = \sum_{e \in \gamma} \langle e |$.

This result is the corollary of the following more abstract mathematical result:

Theorem B1. Let V_1 , V_2 , and V_3 be vector spaces and let $A: V_1 \rightarrow V_2$ and $B: V_2 \rightarrow V_3$ be linear maps satisfying¹⁴

$$
ker(B) = im(A). \tag{B5}
$$

The matrix $M = BPA : V_1 \rightarrow V_3$ has the following properties:

¹⁴In other words, $B|\varphi\rangle = 0$ for $|\varphi\rangle \in V_2$ if and only if, for some $|\varphi'\rangle \in V_1, |\varphi\rangle = A|\varphi'\rangle.$

(1) $M|\varphi\rangle = 0$ if and only if there exist vectors $|+\rangle$ and $|-\rangle$ such that $|\varphi\rangle = |+\rangle + |-\rangle$ and $PA|\pm\rangle = \pm A|\pm\rangle$; moreover, $|\pm\rangle$ are separately also right null vectors of *M*.

(2) $\langle \psi | M = 0$ if and only if there exist vectors $|+\rangle$ and $|-\rangle$ such that $|\psi\rangle = |+\rangle + |-\rangle$ and $\langle \pm |BP = \pm \langle \pm |B\rangle$; moreover, ±| are separately also left null vectors of *M*.

Proof. We prove point (1) of the list, as point (2) is proven analogously. Suppose

$$
M|\varphi\rangle = BPA|\varphi\rangle = 0.
$$
 (B6)

Define the projectors

$$
K_{\pm} = \frac{1}{2}(\mathbb{I} \pm P),\tag{B7}
$$

which have the property that $PK_{\pm} = \pm K_{\pm}$, $K_{\pm}^2 = K_{\pm}$, and $K_{+} + K_{-} = \mathbb{I}$. It follows that

$$
0 = BPA|\varphi\rangle = BP(K_+ + K_-)A|\varphi\rangle = B(K_+ - K_-)A|\varphi\rangle.
$$
\n(B8)

Of course, we also know that

$$
0 = BA|\varphi\rangle = B(K_+ + K_-)A|\varphi\rangle, \tag{B9}
$$

meaning that

$$
BK_{+}A|\varphi\rangle = BK_{-}A|\varphi\rangle = 0. \tag{B10}
$$

By [\(B5\)](#page-15-0), we conclude that there exist $|\pm\rangle$ for which

$$
A|\pm\rangle = K_{\pm}A|\varphi\rangle. \tag{B11}
$$

Evidently,

$$
A(|+\rangle + |-\rangle) = (K_+ + K_-)A|\varphi\rangle = A|\varphi\rangle. \tag{B12}
$$

Since any right null vector of A , $|n\rangle$, satisfies

$$
PA|n\rangle = \pm A|n\rangle = 0,\tag{B13}
$$

we see that $|+\rangle$ and $|-\rangle$ are only determined up to the addition of right null vectors of *A*, should any exist. Therefore, $A(|+\rangle + |-\rangle) = (K_+ + K_-)A|\varphi\rangle = A|\varphi\rangle$, which implies that $|\varphi\rangle = |+\rangle + |-\rangle$ (for appropriate definitions of $|+\rangle$ and $|-\rangle$) corresponding to the freedom to add right null vectors of *A* to either). Left multiply (B11) by *P* to conclude that $PA|\pm\rangle =$ $\pm A|\pm\rangle$. Since *PA* $|\pm\rangle$ is proportional to $A|\pm\rangle$ and $BA = 0$, it follows that $M|\pm\rangle = 0$, which proves the desired statements.

-A straightforward, but useful, consequence of this result is the following:

Corollary B2. Adopt the definitions made in the proof of Theorem [B1.](#page-15-0) Consider the matrix

$$
W = BK_+.\tag{B14}
$$

If $|\varphi\rangle$ satisfies

$$
W|\varphi\rangle = 0,\t\t(B15)
$$

then there exist vectors $|\theta\rangle$ and $|\psi\rangle$ such that

$$
|\varphi\rangle = A|\theta\rangle + K_-|\psi\rangle, \tag{B16}
$$

with $K_+A|\theta\rangle = A|\theta\rangle$.

As a passing remark, the hypothesis of Theorem $B1$ is satisfied by the vector spaces and boundary maps in any short exact sequence of vector spaces together with some partition of the intermediate vector space. For our purposes, Theorem [B1](#page-15-0) serves to enumerate all of the null vectors of *M*. To see how Theorem [B1](#page-15-0) applies to *M*, define $P : \mathcal{D}(\mathcal{E}) \to \mathcal{D}(\mathcal{E})$ such that

$$
P_{ee'} = (-2\mathbb{I}[e \in \mathcal{I}] + 1)\delta_{ee'}, \tag{B17}
$$

where $\mathbb I$ is an indicator function that vanishes if its argument is untrue and is otherwise equal to one. Then,

$$
M = \frac{1}{2} BPA. \tag{B18}
$$

To make more clear our enumeration of null vectors of *M*, we make the following definitions:

Definition B3 (Homogeneous cut). Let $G = (V, \mathcal{C}, \mathcal{I}, \mathcal{I})$ \mathcal{L}, A, B) be a circuit. Let $C = (\mathcal{V}_1, \mathcal{V}_2)$ be a cut of *G*. *C* is a homogeneous cut if the set

$$
\mathfrak{C} = \{ e \subset \mathcal{E} : \exists v_1 \in \mathcal{V}_1 \text{ and } v_2 \in \mathcal{V}_2 \text{ such that } e
$$

$$
\times \in \{ (v_1, v_2), (v_2, v_1) \} \} \tag{B19}
$$

has the property that

$$
\mathfrak{C} \subset \mathcal{C} \tag{B20}
$$

or

$$
\mathfrak{C} \subset \mathcal{I}.\tag{B21}
$$

In the former case, we say that $\mathfrak C$ is capacitive, and in the latter case, we say that $\mathfrak C$ is inductive.

Definition B4 (Homogeneous loop). Let γ be a loop in the sense of Definition [A4.](#page-13-0) If $\gamma \subset \mathcal{C}$ or $\gamma \subset \mathcal{I}$, we say that γ is a *homogeneous loop*.

Corollary B3. Let $G = (V, C, \mathcal{I}, \mathcal{L}, A, B)$ be a circuit. Let Δ_I (Δ_C) be the set of homogeneous inductive (capacitive) loops of G, and let Γ _I (Γ _C) be the set of homogenous inductive (capacitive) loops in *G*. Then,

$$
|\mathcal{F}| - |\Delta_I| - |\Delta_C| = |\mathcal{V}| - |\Gamma_I| - |\Gamma_C|.
$$
 (B22)

Proof. This is an immediate consequence of Theorem [B1,](#page-15-0) together with the rank-nullity theorem.

Corollary $\overline{B3}$ was a result nearly achieved in [\[16\]](#page-19-0), but the relevant discussion relied upon the enumeration of null vectors *and* a number of Noether currents. One of the merits of this approach is that Noether currents in the formalism of [\[16\]](#page-19-0) are promoted to null vectors.

Thus, the number of degrees of freedom in a circuit is equal to the number of loops in a circuit which are neither purely inductive nor purely capacitive.

2. Formal circuit Lagrangian

Here, we restrict our attention to planar graphs. These results can be made to hold for nonplanar graphs with some minor modifications, which will be made explicit in Appendix [C.](#page-17-0)

Definition B5 (Symmetric circuit Lagrangian). Let $G =$ (V, C, I, L, A, B) be a circuit. Let *M* be the connection matrix of *M* and define $|C \cup I|$ functions labeled E_e which describe the energy of the circuit element on branch *e*. The function

$$
L = \sum_{l \in \mathcal{L}, v \in \mathcal{V}} q_l M_{fv} \dot{\phi}_v - \sum_{e \in \mathcal{C}} E_e \left(\sum_l q_l B_{le} \right)
$$

$$
- \sum_{e \in \mathcal{I}} E_e \left(\sum_v A_{ev} \phi_v \right) \tag{B23}
$$

is called the *symmetric circuit Lagrangian* for *G* or "the Lagrangian for *G*" for short.

We see that from (B23), $S = \int dt L$ is symmetric in C and $V.$ As we will discuss later, this choice of variables leads to a very straightforward circuit duality transformation.

For the following result, we will need to rely upon the re-sults of Sec. [III A](#page-6-0) as well as a number of definitions originally made in $[16]$.

Theorem B2. Let $G = (V, C, \mathcal{I}, \mathcal{L}, A, B)$ be a circuit. Let L be the symmetric circuit Lagrangian of *G*. Define $\Gamma_C(\Gamma_I)$ to be the set of capacitive (inductive) cuts of *G*, and let Δ_C (Δ_I) be the set of capacitive (inductive) cycles of *G*. It is always possible to define $|V| - |\Gamma_I| - |\Gamma_C| - 1$ variables $Q_i = \sum_l D_{il} q_l$ and $\Phi_i = \sum_v S_{iv} \phi_v$ so that

$$
\sum_{l,v} q_l M_{lv} \dot{\phi}_v = \sum_{i=1}^{|\mathcal{V}| - |\Gamma_l| - |\Gamma_c| - 1} Q_i \dot{\Phi}_i.
$$
 (B24)

All possible choices of *S* and *D* are related by canonical transformations.

Proof. Define $q_e = \sum_l q_l B_{l}$ for $e \in C$, define $\Omega_{ev} = A_{ev}$ for $e \in C$, and then apply Theorems 10 and 13 from [\[16\]](#page-19-0) directly. directly.

APPENDIX C: CIRCUIT DUALITY

The contents of this Appendix depend broadly on the results of Appendix \bf{B} \bf{B} \bf{B} and serve to formalize the claims in Sec. [IV.](#page-7-0) Duality as a map can be sensibly defined on Lagrangians, graphs, and structures from the theory of topological algebra. While we take a minimal perspective here, the results of this section are very simply expressed as a property of chain-complex isomorphisms.

Definition C1 (Hamiltonian duality transformation). Suppose *H* is a Hamiltonian function of variables Φ_i and Q_i for $i = 1, 2, \ldots, N$, equipped with Poisson brackets

$$
\{\Phi_i, Q_j\} = \delta_{ij}.\tag{C1}
$$

The transformation

$$
Q_i \to Q'_i = -\Phi_i,
$$

\n
$$
\Phi_i \to \Phi'_i = Q_i
$$
 (C2)

is called a *Hamiltonian duality transformation*. We will write $H(Q', \Phi') = H^*$.

Clearly, Hamiltonian duality transformations are canonical since $\{Q_i^j, \Phi_j^j\} = \{Q_i, \Phi_j\}$. Certainly, at the level of Hamiltonian mechanics, it is straightforward to take the dual of any Hamiltonian arising from a circuit Lagrangian in the spirit of the formalism of this work. However, the challenge of constructing the circuit (or circuits) that produces H^* is the subject of this Appendix. Moreover, it is not always possible to produce a (physically sensible) circuit that accomplishes

this task—at least using any known algorithm for constructing a dual circuit.

Definition C2 (Dual circuit). Let $G = (V, C, \mathcal{I}, \mathcal{L}, A, B)$ be a circuit. Define

$$
\mathcal{V}^* = \mathcal{L},
$$

\n
$$
\mathcal{I}^* = \mathcal{C},
$$

\n
$$
\mathcal{C}^* = \mathcal{I},
$$

\n
$$
\mathcal{L}^* = \mathcal{V},
$$

\n
$$
A^* = B^T,
$$

\n
$$
B^* = A^T,
$$
 (C3)

and, finally,

$$
G^* = (\mathcal{V}^*, \mathcal{C}^*, \mathcal{I}^*, \mathcal{L}^*, A^*, B^*). \tag{C4}
$$

We say that *G*[∗] is the *dual circuit* of *G*. For an element *v* of ^V, we write the corresponding element of ^L[∗] as *^v*[∗]. For an element *l* of \mathcal{L} , we write the corresponding element of \mathcal{V}^* as *l* ∗.

Our reason for using this terminology will become clear shortly. Both a combinatorial object and a topological object are encoded in *G*[∗]. That is to say that the combinatorial properties of *G*[∗] are encoded in the structure of *A*[∗]. While it is straightforward to recover the combinatorial structure of *G*[∗] by looking at the matrix *A*[∗], it is less obvious how one might recover a particular embedding of *G*[∗] by using *B*[∗]. Though we will not belabor this point presently, we remark that a particular embedding of G^* is recoverable by a gluing procedure where every element of $\mathcal F$ is represented by a patch isomorphic to the unit disk, and then patches are glued together by identifying segments on the boundary of different patches, in a way that is consistent with the content of *A*[∗]. This is always possible. For planar graphs, this procedure is always accomplished by the following procedure:

Definition C3 (Embedding of dual circuit). Let $G =$ $(V, C, I, \mathcal{L}, A, B)$ be a circuit. Further suppose *G* is embedded upon a sphere. We construct the *embedded dual circuit* of *G*, *G*[∗], as follows:

(1) For every loop *l* in \mathcal{L} , draw a vertex labeled l^* (inside of the face whose boundary is *l*).

(2) For every pair of loops l_0 and l_1 in \mathcal{L} , draw an inductive (capacitive) edge between l_0^* and l_1^* for every capacitive (inductive) edge in both l_0 and l_1 . For such an edge e of G , label the corresponding edge in *G*[∗] as *e*[∗].

(3) For every edge *e*[∗] in *G*[∗], give *e*[∗] an orientation so that when the surface is drawn (locally) on the plane, the cross product between *e* and *e*[∗] is always positive.

Definitions C2 and C3 are equivalent for planar graphs. We emphasize that the construction of a dual graph is intrinsically dependent upon the embedding of the chosen *G*. We will make this point explicit with the next observation.

Observation C1. Let *G* be a planar graph. Choose two embeddings of *G* on *S*, G_S and G_S' . G_S^* and $(G_{S'})^*$ need not be graph isomorphic.

Proof. We provide a proof by example in Figs. [4\(a\)](#page-8-0) and [4\(b\).](#page-8-0) In order to view a circuit as a graph, one only needs to ignore all of the circuit elements in the circuit so that every branch becomes simply a graph theoretic edge. -

Observation C2. Let $G = (V, C, \mathcal{I}, \mathcal{L}, A, B)$ be a circuit. Let $G^* = (\mathcal{V}^*, \mathcal{C}^*, \mathcal{I}^*, \mathcal{L}^*, A^*, B^*)$ be the dual circuit of *G*. Define the matrix $M^* : \mathcal{V}^* \to \mathcal{L}^*$ with matrix elements

$$
M_{v^*,l^*}^* = \frac{1}{2} \sum_{e^* \in C^*} B_{v^*e^*}^* A_{e^*l^*}^* - \frac{1}{2} \sum_{e^* \in \mathcal{I}^*} B_{v^*e^*}^* A_{e^*l^*}^*.
$$
 (C5)

Then, $M^* = -M^T$.

Proof. By relabeling,

$$
\langle v^* | M^* | l^* \rangle = \frac{1}{2} \sum_{e^* \in C^*} B_{v^* e^*}^* A_{e^* l^*}^* - \frac{1}{2} B_{v^* e^*}^* A_{e^* l^*}^*
$$

$$
= \frac{1}{2} \sum_{e \in \mathcal{I}} A_{ve} B_{el} - \frac{1}{2} \sum_{e \in C} A_{ve} B_{el} = -\langle v | M^{\mathrm{T}} | l \rangle.
$$
 (C6)

Since $\langle v^* | M^* | l^* \rangle = \langle v | M^T | l \rangle$, we say simply $-M^T = M^*$. *Theorem C1.* Let $G = (V, C, \mathcal{I}, \mathcal{L}, A, B)$ be a circuit. Let

 G^* be the dual circuit of *G*. For each edge *e* in $\mathcal{I} \cup \mathcal{C}$, suppose that the energy associated with edge *e* is a function $E_e : \mathbb{R} \to \mathbb{R}$. For each edge e^* in $\mathcal{I}^* \cup \mathcal{C}^*$, fix $E_{e^*} : \mathbb{R} \to \mathbb{R}$ so that

$$
E_{e^*}(x) = E_e(x). \tag{C7}
$$

The Lagrangian for *G* and the Lagrangian for *G*[∗] are related by a relabeling transformation.

Proof. The Lagrangian for *G* is given by

$$
L = \sum_{l \in \mathcal{L}} \sum_{v \in \mathcal{V}} Q_l M_{lv} \dot{\phi}_v - \sum_{e \in \mathcal{I}} E_e \left(\sum_v A_{ev} \phi_v \right)
$$

$$
- \sum_{e \in \mathcal{C}} E_e \left(\sum_l q_l B_{l e} \right). \tag{C8}
$$

On the other hand, the Lagrangian for *G*[∗] is given by

$$
L^* = \sum_{v^* \in L^*} \sum_{l^* \in \mathcal{V}^*} q_{v^*} M_{v^*l^*}^* \dot{\phi}_{l^*} - \sum_{e^* \in \mathcal{I}^*} E_e \left(\sum_{l^* \in \mathcal{V}^*} A_{e^*l^*}^* \phi_{l^*} \right) - \sum_{e^* \in \mathcal{V}^*} E_e \left(\sum_{v^* \in \mathcal{L}^*} K_{v^*} B_{v^*e^*}^* \right).
$$
 (C9)

The transformation

$$
q_{v^*} \to \phi_v,
$$

\n
$$
\phi_{l^*} \to q_l,
$$

\n
$$
M_{v^*l^*}^* \to -M_{lv},
$$

\n
$$
C^* \to \mathcal{I},
$$

\n
$$
\mathcal{I}^* \to C
$$
 (C10)

can easily be seen to relate L^* to L after integrating the first term by parts.

Corollary C1. Let *G* be an embedded circuit with Lagrangian *L* and *G*[∗] be the dual circuit of *G*. By Theorems C1 and [B2,](#page-17-0) it is always possible to find $N = |\mathcal{V}| - |\Gamma_I| - |\Gamma_C|$ – 1 variables so that the Lagrangian for *G* may be written

$$
L = \sum_{i=1}^{N} Q_i \dot{\Phi}_i - H(Q, \Phi).
$$
 (C11)

FIG. 7. A heuristic drawing on an identified polygon representation of a torus. If a charge or flux about some "topological" loop is to be dynamical, then its dual must also be topological. A "topological current" is drawn and labeled in red. The naive dual to the current \dot{q} would be a voltage drop across the corresponding cut. In the figure above, the nonlocal "topological" voltage resulting from the naive duality map would participate in all three dual edges with the label ϕ_{dual} .

It is always possible to write the Lagrangian for *G*[∗] as

$$
L^* = -\sum_{i=1}^{N} \Phi_i \dot{Q}_i - H(-\Phi, Q). \tag{C12}
$$

Proof. Since

$$
\sum_{i=1}^{N} Q_i \dot{\Phi}_i = \sum_{v,l} q_l M_{lv} \dot{\phi}_i,
$$
 (C13)

it follows that under the transformation $(C10)$,

$$
Q_i \dot{\Phi}_i \to -\Phi_i \dot{Q}_i. \tag{C14}
$$

-

We remark that for nonplanar graphs, the Lagrangian transformations given in Corollary C1 is perfectly well defined. It is also true that the transformation (C10) is *also* perfectly well behaved. The issue is simply that for nonplanar graphs, there is no systematic analog of Definition C_3 that applies to nonplanar graphs in any meaningful sense. The reason for this is that edges in so-called topological loops would, in the dual of a nonplanar graph, have an odd number of endpoints (See Fig. 7), which contradicts our definition of what an edge is. Nonetheless, it is sometimes possible to "planarize" a nonplanar circuit and then take the dual after planarization, as we saw for K_5 in the main text.

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