Imaging localized variable capacitance during switching processes in silicon diodes by time-resolved electron holography

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Interference gating or iGate is a unique method for ultrafast time-resolved electron holography in a transmission electron microscope enabling a spatiotemporal resolution in the nm and ns regime with a minimal technological effort. Here, iGate is used for the first image-based investigation of the local dynamics of the projected electric potential in the area of the space-charge region of two different general purpose silicon diodes during switching between unbiased and reverse-biased condition with a temporal resolution of 25 ns at a repetition rate of 3 MHz. The obtained results for a focus-ion-beam-prepared ultrafast UG1A rectifier diode, which shows a decreasing capacitance with increasing reverse bias are in good agreement with an electric characterization of the macroscopic device as well as with theoretical expectations. For a severely modified 1N4007 device, however, time-resolved electron holography revealed a MOSCAP-like behavior with a rising capacitance in the area of the space-charge region during the switching into reverse-biased condition. Remarkably, a different behavior, dominated by the effective capacitance of the electrical setup, can be observed in the vacuum region outside both devices within the same measurements, clearly showing the benefits of localized dynamic potentiometry.

I. INTRODUCTION

The semiconductor industry with its continuous developments plays a central role in our modern technology-driven society. Here, the theoretical understanding of underlying physical processes (e.g., from analytical models or numerical simulations) and experience-based knowledge in processing (e.g., from experimental observations) go hand in hand. This is particularly noticeable in the course of the continuous miniaturization of semiconductor structures (e.g., semiconductor nanostructures) in order to increase their efficiency while reducing their switching times [1].

Probably the most established transmission electron microscopic (TEM) and thus imaging technique for the investigation of electrical potential distributions in semiconductor structures in the nm range is off-axis electron holography (EH) [2,3]. By overlapping a reference wave with an object wave, an interference pattern can be acquired, which, via a numerical reconstruction process, grants access to the phase modulation $\varphi_{el}(x)$ of the reconstructed electron wave, which is directly proportional (by an interaction constant σ) to the projected potential distribution $V(x, y, z)$ inside and outside

investigated samples [4]:

$$\varphi_{el}(x, y) = \sigma \int V(x, y, z)\mathrm{d}z. \tag{1}$$

In static experiments, EH has been able to demonstrate, among other things, the increasing influence of surface effects (e.g., crosstalk due to stray fields [5] or the broadening of space charge regions (SCR) [4,6]) with a continuous reduction of the structure dimensions, thus serving as input for new theoretical models [7,8]. For a long time, however, EH has, within the exposure times of common detectors (in the subsecond range), been limited to static investigations [9], so that observations of ultrafast dynamic effects (e.g., charge-carrier transients or the effects of a dynamic variation of the capacitance, both of which contribute to changed switching times of the devices) have not been possible so far.

A novel method for realizing robust time-resolved experiments in the TEM, called interference gating (iGate) [10,11], seems promising to address this shortcoming. By a deliberate destruction of the interference pattern by controlled external disturbances, synchronized to a periodic process with periodicity T under investigation, a large part of the interferometric information is suppressed. Only for a fixed fraction τ (gate) of the period T, an undisturbed interference pattern can build up. The "partially disturbed" interference pattern acquired
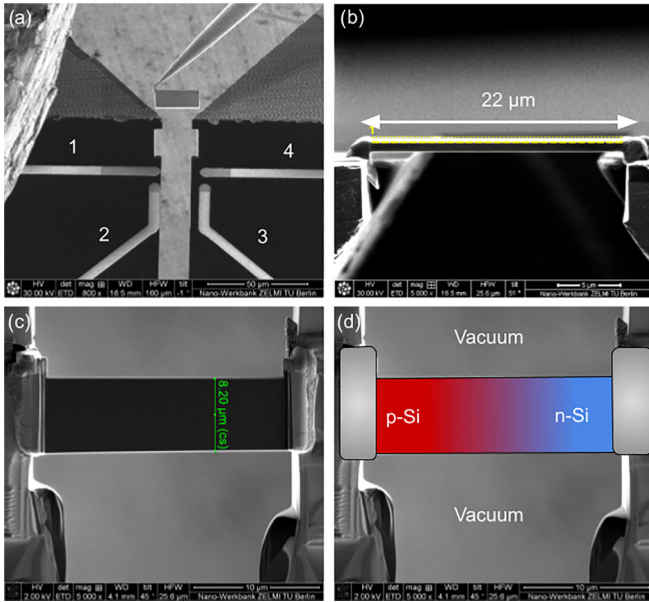
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FIG. 1. Contacting and post processing of the TEM lamella on a FIB-optimized E-chip: (a) conventional lamella transfer with the micromanipulator, where the numbers 1 to 4 denote the contact pads, (b) thinning and polishing of the surfaces (view in cross-section), (c) SEM image of the final contacted lamella with (d) overlaid markings of the contacts, the p and n regions and the reference- and object-wave areas for the electron holographic acquisition.

over an arbitrary number of periods represents a time-resolved electron hologram, with the numerical reconstruction process acting as a temporal filter that only retains the information from the gate. With this scheme, in principle, time resolutions into the picosecond (ps) range can be realized [12], making iGate a powerful tool for dynamic investigations of electronic nanostructures.

As a first real-world application of iGate, localized capacitive effects in periodically switched general-purpose Silicon (Si) diodes are investigated with nm spatial and ns temporal resolution, addressing the question of to what extent electrical properties of samples can be characterized using dynamic imaging.

II. SAMPLE

As objects of interest, two general-purpose Silicon diodes, a fast switching UG1A diode and a common 1N4007 rectifier diode, are investigated. Since both are manufactured by a thermal diffusion process, a strongly extended space-charge region (SCR) in the μm range is expected. The diodes are ground out of their housing (via a T-tool grinding device [13]) and the area of the p-n junction (located by voltage contrast microscopy [14,15]) is lifted out, transferred, contacted, thinned, and cleaned (Fig. 1) via focused ion beam (FIB) preparation (FEI Helios NanoLab 600, 30 kV Ga-ion beams of 2.8 nA, 280 pA, and 93 pA) into a TEM lamella with dimensions of approx. 22 μm × 8 μm × 400 nm Figs. 1(b), 1(c)]. For the flat fixation and proper contacting of the TEM lamella on the E-chip, the thick transfer needle must lower the lamella without any physical interaction between the needle

and the E-chip. Therefore, a tall spacer lug between lamella and needle [Fig. 1(a)] is prepared with ion beam (30 kV, 10 pA) induced platinum deposition prior to the mentioned lift-out process. The spacer lug is thereby slightly tilted with respect to the lamella to have enough mechanical freedom of movement. The lamellae are contacted at pads 1 and 4 in such a way that their interface of the p-n junction sits parallel between the free-standing electrodes [false colored in Fig. 1(d)] of the carrier chip [Protochips FIB optimized E-chip, Fig. 1(a)]. By this, parasitic currents (e.g., due to platinum halo on the surface of the carrier chip) are avoided and the diode current is guided directly through the lamella (and its surface).

The preparation process was monitored by *I-V* measurements (before and after FIB preparation), shown for both diodes in the Supplemental Material, Fig. 1 [16]. After subtracting a shunt resistance (due to surface conduction), the FIB-prepared diodes exhibit a strongly nonlinear behavior, which is similar to the expected diode behavior for the UG1A diode. The prepared 1N4007 diode, however, shows a different *I-V* characteristic, featuring a saturation behavior for negative and positive biases. Nevertheless, both prepared diodes represent switchable devices (detailed description in the Supplemental Material [16]). Furthermore, the switching times of both macroscopic devices (before preparation) were investigated (Supplemental Material, Fig. 2 [16]) in small signal operation (±1 V). For the switching into reverse bias condition, the macroscopic UG1A diode shows a switching time of approximately $t_{rr} = 25$ ns (according to the data sheet, the expected switching time in full load operation is $t_{rr} = 15$ ns [17]). Under the same conditions, the macroscopic 1N4007 diode shows a switching time of approx. $t_{rr} = 33$ ns (no information available in the data sheet [18]).

III. STATIC ELECTRON HOLOGRAPHY

The FIB-prepared diodes were investigated with static electrical biasing EH. For this purpose, the FEI Titan 80-300 Berlin Special Holography TEM was used in a special Lorentz mode for wide fields of view [12] at an acceleration voltage of $U_a = 200$ kV. The electron holograms were acquired with an acquisition time of $t_{exp} = 4$ s using a Gatan US1000 CCD. The vacuum region in front of the lamella [according to Fig. 1(d)] was utilized as reference-wave area. Exemplary reconstructed holograms are shown in Fig. 2. For the static investigations, the electrical bias U is applied by a Keithley 2460 source meter, connected to a modified Protochips Aduro electrical biasing holder [19].

As expected, the reconstructed amplitude [Fig. 2(a)] shows no modulation due to the potential distribution even with an applied reverse bias of $U = -4$ V, but the reconstructed phase clearly exhibits a modulation [Fig. 2(b)]. The phase modulation includes not only the projected potential of the reverse biased sample itself, but also parasitic influences (stray field of the surface of the sample, stray field of the contacts, influences of the electron-optical beam path, and unwanted modulation of the reference wave). The latter in particular lead to the unexpected bending of the equiphase lines within the sample [Fig. 2(b)], which can be corrected by normalization. For the normalization, the reconstructed
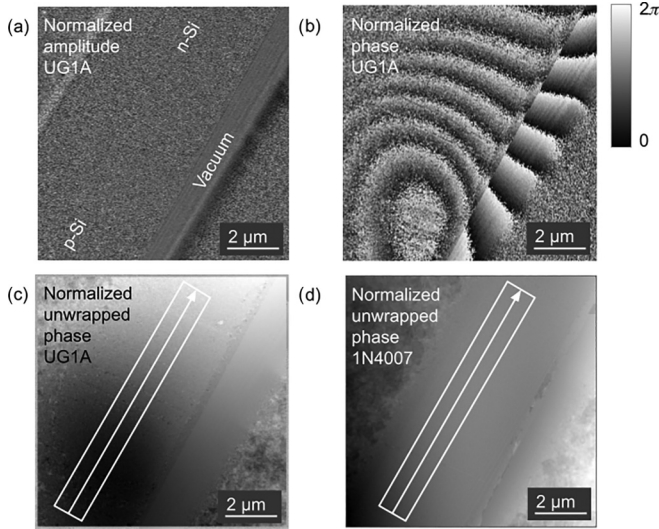
FIG. 2. Reconstructed electron holograms of both diodes with a reverse bias of $U = -4\,\mathrm{V}$: (a) normalized amplitude of the UG1A diode with markings for the p and n region as well as the vacuum region in front of the lamella, (b), (c) normalized wrapped (b) and unwrapped (c) phase of the UG1A diode, (d) normalized unwrapped phase of the 1N4007 diode. Areas for the phase profiles (Figs. 3 and 4) are indicated in the unwrapped phases.

electron waves from measurements with applied bias are divided by reconstructed electron waves from measurements without applied bias. This compensates for all artifacts of the measurement setup (e.g., due to distortions or charges in the beam path), the sample (e.g., due to dynamic diffraction and charging) but also for the built-in potential. The normalized reconstruction thus only contains information resulting from a change of the applied bias.

The profile plot of the normalized unwrapped phases $\varphi_{el}(x)$ of the UG1A diode (Fig. 3) shows an unmodulated phase course for the unbiased condition and a nonlinear phase course
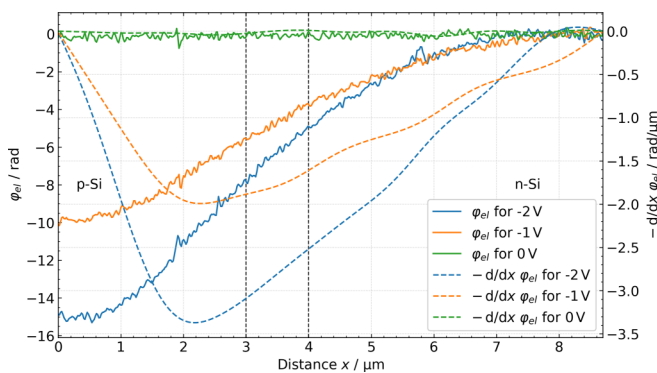

FIG. 3. Plot of the normalized unwrapped phase profiles $\varphi_{el}(x)$ (phase offset to zero on the n-doped side) as well as their first-order derivatives (phase slopes) $-\mathrm{d}/\mathrm{d}x\,\varphi_{el}(x)$ (dashed lines) of the FIB-prepared UG1A diode in x direction for different applied reverse biases U [taken from the area according to Fig. 2(c)] with the doped regions of the diode indicated near the edges of the plot. The vertical dashed lines mark the area for the evaluation of the dynamic phase slopes (Figs. 8 and 9).
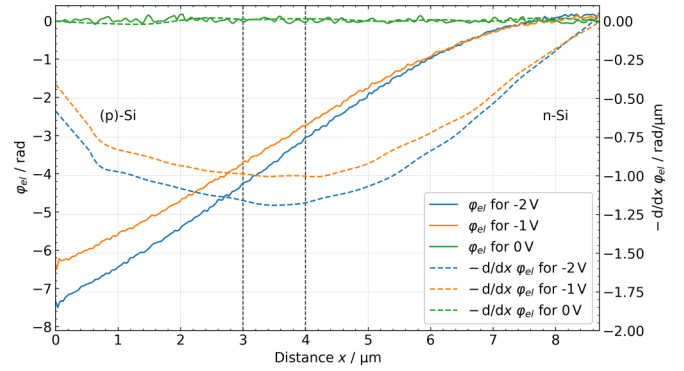

FIG. 4. Plot of the normalized unwrapped phase profiles $\varphi_{el}(x)$ (phase offset to zero on the n-doped side) as well as their first-order derivatives (phase slopes) $-\mathrm{d}/\mathrm{d}x\,\varphi_{el}(x)$ (dashed lines) of the FIB-prepared 1N4007 diode in x direction for different applied reverse biases U [taken from the area according to Fig. 2(d)] with the doped regions of the diode indicated near the edges of the plot. The vertical dashed lines mark the area for the evaluation of the dynamic phase slopes (Figs. 8 and 9).

for applied reverse biases, whereas the phase jump (phase difference for the beginning and end of the phase profile) increases with applied reverse bias. Additionally, the phase slopes [first-order derivative $-\mathrm{d}/\mathrm{d}x\,\varphi_{el}(x)$, which is proportional to the projected electric field] show a minimum around $x = 2\,\mu\mathrm{m}$, which also increases with applied reverse bias. The derivatives were calculated by *a priori* smoothing of the phase profiles with a one-dimensional (1D) Gaussian Filter with $\sigma_G = 100\,\mathrm{nm}$.

Taking into account Eq. (1), the reconstructed phases (Fig. 2) and their correlated profiles (Figs. 3 and 4) are directly proportional to the projected electric potential distribution of the samples. For the UG1A diode, the phase profiles for the reverse-biased condition (Fig. 3) qualitatively agree with a projection of the typical potential profile of a p-n junction diode (e.g., quadratic approximation) with an asymmetric doping concentration. However, it must be taken into account that the electric stray field of the sample not only modulates the reference wave, but also leads to non-negligible phase modulations above and below the sample. These can, for example, result in an expansion of the width of the measured potential jump and thus hinder quantitative investigations. Nevertheless, the whole SCR appears to be inside the prepared TEM lamella for the UG1A diode, suggesting a successful FIB preparation of an intact diode.

The plot for the 1N4007 diode (Fig. 4) paints a different picture. While the phases $\varphi_{el}(x)$ show a similar course towards the end of the profile (n doped side), they seem to be truncated towards the p doped side (at the beginning of the profile) resulting in a TEM lamella which only features a partial SCR. This was caused during the cut-out procedure due to the fact that the junction width of the 1N4007 diode seemingly exceeds the overall length of the lamella, which is limited by the width of the slit in the E-chip. Consequently, neither a phase jump can be detected nor does the phase slope $-\mathrm{d}/\mathrm{d}x\,\varphi_{el}(x)$ show a pronounced minimum (dashed lines). Although, in contrast to the UG1A diode, both profiles show only limited
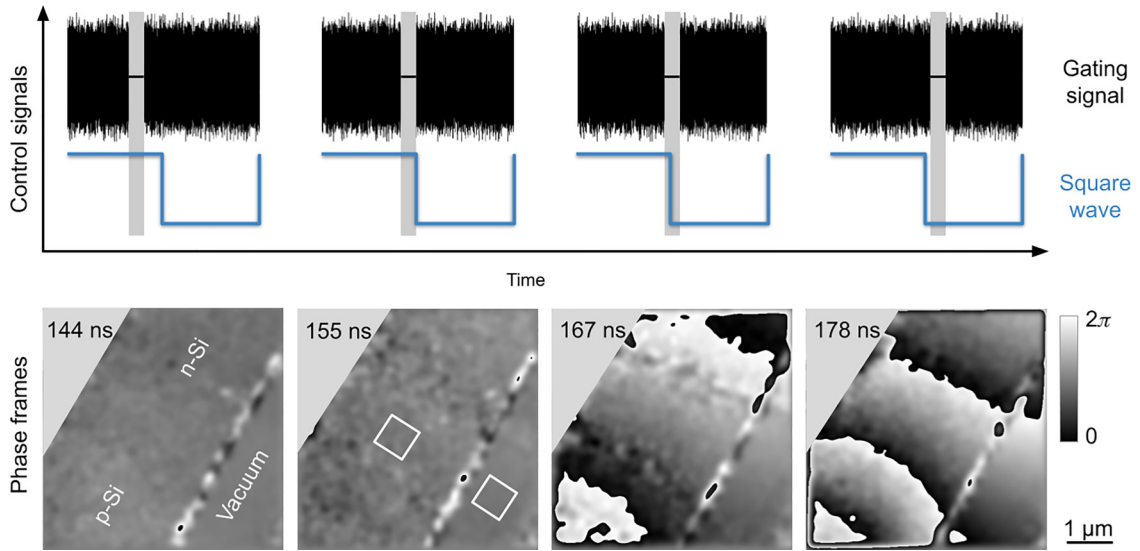
FIG. 5. Schematic representation of the applied control signals during sampling and the corresponding reconstructed time-resolved wrapped phases (frames) with a temporal resolution of $\tau = 25$ ns for the switching of the UG1A diode into reverse-biased condition for different gate positions between 144 ns and 178 ns with a sampling resolution of $t_0 = 11.1$ ns.

changes with increasing reverse bias for the 1N4007 diode, a difference to the unbiased condition is still clearly visible (due to the normalization).

According to the course of the phase, this sample is more likely to represent a capacitor with a poorly chosen dielectric (lightly p-doped Si on the left electrode and gradually increasing n-doped Si on the right electrode), which is supported by the limited change of the phase jump (Fig. 4) for different reverse biases. On this basis, and considering the *I-V* characteristics (Supplemental Material, Fig. 1 [16]), a severely modified device with a different electric switching behavior than that of a conventional diode is expected.

IV. TIME-RESOLVED ELECTRON HOLOGRAPHY

For the investigation of the switching dynamics of both diodes, interference gating [10] is used in order to produce time-resolved electron holograms. For this, a GW Instek MFG-2260MRA multichannel arbitrary signal generator producing synchronized control signals (a gating signal and a signal for the switching the diodes) was connected to a biprism in the condenser aperture plane (used as a gating device) and the electrical biasing holder (detailed description of the setup in Ref. [12]). Both signals, provided by a custom Python script, were monitored by an oscilloscope (GW Instek GDS-1102B connected in parallel). For the switching of the diodes, a square wave with a peak-to-peak amplitude of $U = 1.0$ V$_{pp}$ (from $U = 0$ V to $U = -1$ V) at a repetition rate of $f = 3$ MHz was applied. By this, the diodes are unbiased and reverse biased for half of the period $T = 333.3$ ns respectively. For the gating, a noise signal with a peak-to-peak amplitude of $U = 2.7$ V$_{pp}$ featuring a $U = 0.0$ V$_{pp}$ gate with a gate length of $\tau = 25$ ns was used to sample the switching process with a sampling resolution of $t_0 = 11.1$ ns, resulting in 33 phase frames (schematically shown in Fig. 5). The time-resolved electron holograms were acquired in a setup similar to the static ones with a slightly higher magnification (in order

to increase the fringe contrast) in a central region of the diodes (around $x = 4$ μm in Figs. 3 and 4). Since a major advantage of interference gating is that the time resolution is independent of the used detector, the time-resolved holograms, with an acquisition time of $t_{\mathrm{exp}} = 8$ s each, were likewise recorded with a Gatan US1000 CCD. The interference gating thus reduces the fringe contrast of the time-resolved holograms by the ratio between gate length τ and period T (the so-called gate fraction) compared to a static hologram, leading to an increased phase noise [10,12]. In order to increase the signal-to-noise ratio and compensate for the increased phase noise (to a certain degree), five time-resolved holograms for each gate position (frame) were averaged during the reconstruction [20].

Exemplary phase frames (wrapped) for the switching into reverse-biased condition of the UG1A diode are shown in Fig. 5.

The development of the phase modulation [comparable to the static case in Fig. 2(b)] can be seen step by step in the exemplary phase frames (e.g., by the equiphase lines moving closer together). In addition, slight double-exposure electron holography (DEEH) artifacts [10,21] are visible in the frames at $t = 155$ ns and $t = 167$ ns (surrounding the white square in the central region of the UG1A diode). However, their influence on the phase modulation is limited, therefore the time-resolved phase information can be regarded as an extension to Eq. (1) by means of a dynamic projected potential distribution.

Considering the high frequency of $f = 3$ MHz of the applied square-wave signal, capacitive effects of the overall system (cabling, electrical biasing holder, carrier chip, and the diodes) play a non-negligible role. In order to take these into account, a capacitive system (representative of the overall system), driven by a 3 MHz square wave signal ($U_{\mathrm{in}} = 1$ V$_{pp}$), was modeled by numerical simulation using LTspice [22] (lower left box in Fig. 6).

In the simulation, the capacitance of the system was varied from $C = 0$ pF to $C = 200$ pF for an effective transmission
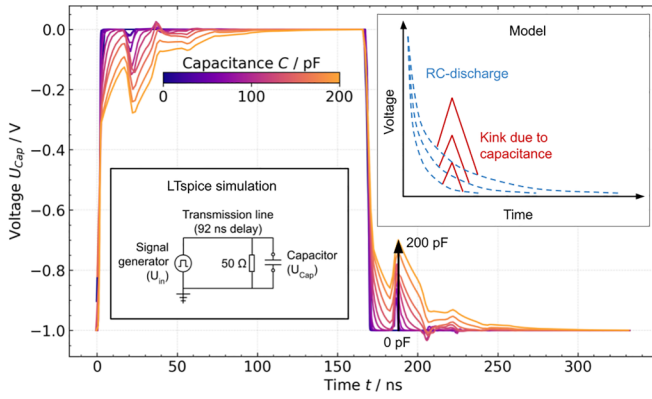
FIG. 6. Plot of simulated dynamic voltages $U_{cap}(t)$ at a capacitor, driven by a 3 MHz square wave ($U_{in} = 1 V_{pp}$) for different capacitances from $C = 0$ pF to $C = 200$ pF (circuit for the LTspice simulation embedded in the lower left box). Basic model for the illustration of the effect with varying capacitance (resulting kink due to reflections) embedded in the upper right box.

line delay of 92 ns (determined by time-domain reflectometry), yielding dynamic voltages U_{cap} plotted in Fig. 6. Without a capacitance ($C = 0$ pF), U_{cap} matches the applied square wave U_{in}, with increasing C, however, a kink starts building near the transition between the two voltages. The kink is primarily caused by signal reflections on the capacitor traveling back the transmission line [23]. The behavior of U_{cap} can be described, to a first approximation, by a basic *R-C* charge/discharge superimposed with a kink of variable height (upper right box in Fig. 6). The height of the kink in this basic model is proportional to the capacitance C.

In the experiment, the applied control signal for the time-resolved electron holographic investigations, monitored by an oscilloscope (blue line in Fig. 7) and measured in the vacuum region in front of the TEM lamella, features a kink (similar to the simulated signals) as well. Interestingly, the course of the monitored signal (e.g., the height of the kink) does not change for the different diodes (or even an empty carrier chip without
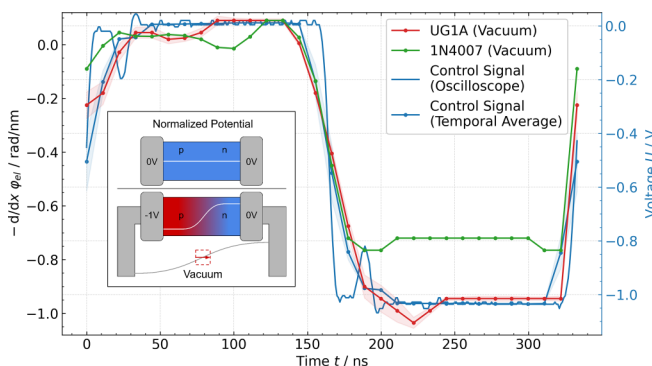

FIG. 7. Plot of the applied control signal, measured by the oscilloscope (blue line), its temporal average (blue dots), calculated phase slopes of the phase frames, taken in the vacuum region in front of the lamella, for the UG1A diode (red dots) and the 1N4007 diode (green dots). The standard deviation (light colored) is given for all averaged signals. A schematic representation of the measurement is depicted in the lower left box.

any TEM lamella). This behavior is predominantly caused by the electrical biasing system itself (mainly the carrier chip). A TEM lamella, given by its relatively small dimensions (in contrast to the carrier chip), does not have a notable effect on the monitored signal at all (at least in this experimental setup of the TEM lamella, which can be regarded as a parallel setup of capacitors). In regard to the simulated signal (comparison of the height of the capacitive kinks), the overall capacitance of the biasing system can be determined to approx. $C = 150$ pF.

Since in the time-resolved measurements, the dynamic phase modulation is averaged over the gate length of $\tau = 25$ ns with a sampling resolution of $t_0 = 11.1$ ns, the monitored signal is also temporally averaged in the same manner (25 ns every 11.1 ns; blue dots in Fig. 7) in order to be comparable. By this, the transient between the two switching states broadens due to the averaging (comparable to a convolution with a rectangular pulse).

According to Eq. (1), the phase frames themselves are proportional to the dynamic projected electric potential distribution $\varphi_{el}(x)$, therefore the phase slopes $-d/dx\,\varphi_{el}(x)$ are proportional to the projected electric field strength distribution and thus correlated to an electric voltage distribution. Consequently, the phase slopes in the vacuum region in front of the lamellae (indicated by the white square in Fig. 5, plotted as red dots for UG1A diode and green dots for 1N4007 diode in Fig. 7), which are mainly modulated by the electric potential of the free-standing electrodes of the carrier chip, can be compared to the temporal averaged control signal shown as blue line in Fig. 7.

The course of the dynamic phase slopes $-d/dx\,\varphi_{el}(x)$ in the vacuum region in front of the UG1A diode (red dots in Fig. 7) is in excellent agreement with the control signal. This is also true for the course of the dynamic phase slopes in the vacuum region of the 1N4007 diode (green dots in Fig. 7), whose scaling, however, deviates from that of the control signal. This is mainly caused by a larger distance between the free-standing electrodes of the carrier chip (manufacturing-related) for this lamella, which leads to a reduced field strength (for the same applied voltage U).

In contrast to the measurements in the vacuum region, the dynamic phase slopes in a central region of the UG1A diode (indicated by a white square in Fig. 5, plotted as red dots in Fig. 8; notably within the same data set, only at a different spatial location) show a different course, primarily as a narrowing of the transient during switching into reverse bias condition.

This becomes particularly clear in comparison to the temporal average (blue dots) of the modeled control signal (blue line) in Fig. 8. Here, a switching time of $t_{rr} = 25$ ns (taken from the electrical investigation shown in the Supplemental Material, Fig. 2 [16]) and capacitance of $C = 7.5$ pF was used for the basic model. For these values, the signals are in excellent agreement, yielding a capacitive kink that is significantly smaller compared to the measurements in the vacuum region (Fig. 7). This indicates a reduction of the capacitance of the diode during the transition into reverse-biased condition. When switching back to the unbiased condition, the dynamic phase slopes in the diode region (Fig. 8) behave almost
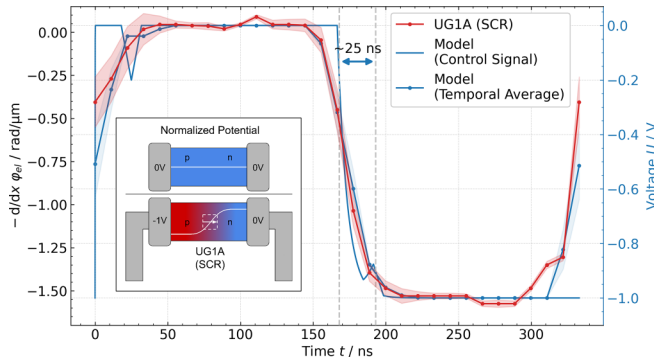
FIG. 8. Plot of the best fitting modeled control signal, according to the basic model in the upper right box in Fig. 6 (blue line), its temporal average (blue dots), calculated phase slopes of the phase frames, taken in the center region of the lamella, for the UG1A diode (red dots). The standard deviation (light colored) is given for all averaged signals. A schematic representation of the measurement is depicted in the lower left box.
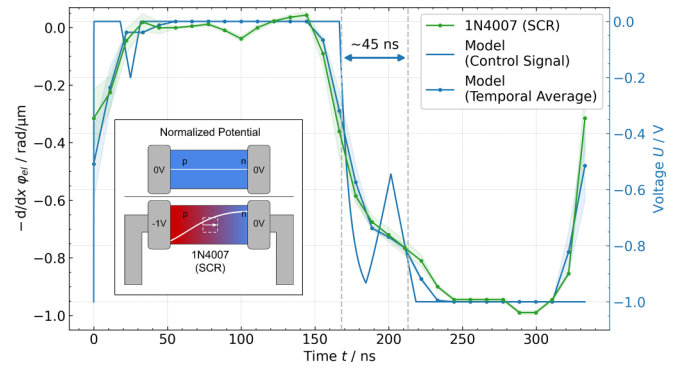

FIG. 9. Plot of the best-fitting modeled control signal, according to the basic model in the upper right box in Fig. 6 (blue line), its temporal average (blue dots), calculated phase slopes of the phase frames, taken in the center region of the lamella, for the 1N4007 diode (green dots). The standard deviation (light colored) is given for all averaged signals. A schematic representation of the measurement is depicted in the lower left box.

identically to those in the vacuum region (Fig. 7), indicating an increase back to the initial capacitance. This behavior, called depletion capacitance [24], is quite typical for diodes (fundamental principle of varicap diodes) and is primarily caused by a change in the width of the SCR due to an applied bias. Given by the small influence of the reduced capacitive kink, the transient time into reverse biased condition (according to the basic model) was determined to take approx. 25 ns, which is also in excellent agreement with the electrical characterization (Supplemental Material, Fig. 2 [16]).

Even stronger deviations from the vacuum region are observed for the dynamic phase slopes in a center region of the 1N4007 diode (green dots in Fig. 9). For a nearly excellent agreement with the temporal average (blue dots) of the modeled control signal (blue line), a switching time of $t_{rr} = 33$ ns (taken from the electrical investigation shown in the Supplemental Material, Fig. 2 [16]) and a capacitance of $C = 430$ pF was used in the basic model. By this, the height of the capacitive kink is drastically increased compared to the vacuum region, resulting in an overall extended transition time of approximately 45 ns. Under the (aforementioned) assumption of a capacitor with lightly doped Si as dielectric, such a behavior could be related to a reduction of the free-charge carriers in the doped silicon by the applied "reverse" bias. Such behavior is typical for metal-oxide-semiconductor capacitors (MOSCAP), where reverse bias leads to an accumulation of charge carriers at the interfaces and thus to a depletion zone inside the oxide, resulting in an increasing capacitance [24]. Similar to the UG1A diode, the transition back into the unbiased condition seems to be unchanged (compared to the measurement in the vacuum region in Fig. 7).

V. CONCLUSION AND OUTLOOK

It was shown that iGate is well suited for the investigation of dynamic electrical potential distributions and their

effects in semiconductor devices. Here, it was used to image the effects of localized dynamic capacitance in switching general-purpose silicon diodes with a temporal resolution of $\tau = 25$ ns. For a successfully prepared fast switching UG1A diode, a decreasing capacitance (down to approx. $C = 7.5$ pF) during switching into reverse-biased condition was observed inside the sample, whereas within the same measurement, the capacitance outside the sample remained unchanged at approximately $C = 150$ pF. For a severely modified 1N4007 diode, featuring only a partial SCR inside the TEM lamella, an increasing capacitance (up to approx. $C = 430$ pF) was observed, revealing a MOSCAP-like behavior, which fits well with the saturation behavior of the measured I-V characteristic (Fig. 2 [16]). Both results clearly demonstrate the advantages of a dynamic imaging method with high spatiotemporal resolution, through which static physical properties of samples (e.g., capacitance), remaining hidden in static experiments, can be uncovered. This clearly affirms the initial question and shows that the potential-sensitive EH, in particular, can be improved into local dynamic potentiometry by means of iGate.

While for the used extended Lorentz mode (only used due to the large dimension of the investigated diodes) the spatial resolution is limited to approximately 30 nm and the temporal resolution to approx. 25 ns (due to the bandwidth limitations of the used signal generator), a transition to higher magnifications (e.g., common medium- or even high-resolution TEM modes) is inherently given by the TEM, opening the door to the investigation of smaller nanostructures (e.g., dynamic of semiconductor/magnetic nanostructures). Meanwhile, the step to higher temporal resolutions (in the sub-ns regime) have already been demonstrated using self-developed control devices [19]. In addition, iGate can in principle be applied to further interferometric techniques (e.g., inline electron holography, ptychography, or diffraction), hence, creating a completely new pathway for the acquisition of movies of *in operando* nanostructures.

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