Blocking transition of interface traps in MoS_2/SiO_2 field-effect transistors

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The interface traps and associated charge disorder in two-dimensional-material field-effect transitors (FETs), and many other devices, limits their performance but offers interesting physics and potential for applications. The electrical conductivity with gate-sweep in a few-layer MoS_2-on-SiO_2 FET is found to show an abrupt reduction in hysteresis when cooled. The hysteresis and time-dependent conductivity of the MoS_2 channel are modeled using the dynamics of interface traps' occupancy. The reduction in hysteresis is found to be steepest at a blocking temperature near 225 K. This is attributed to the interplay between thermal and barrier energies and fitted using a distribution of the latter. Further, the charge stored in the blocked traps at low temperature, and thus the threshold gate voltage, is reversibly programed over a wide range by cooling under suitable gate voltage. This illustrates the application of this blocking of traps for heat-assisted nonvolatile memory.

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I. INTRODUCTION

Single- and few-layer transition metal dichalcogenides [1,2] offer much potential for device applications including transistors [3,4] with high frequency capability [5], logic gates [6,7] for integrated circuits [8], and optoelectronic [9–12] devices. The MoS_2 single-layer devices with direct band gap [1,3] in optical range have been of particular interest. The field-effect transistors (FETs) based on MoS_2 show a very promising behavior with scalability, nonideal behavior, and degradation with time as the main hurdles. The defects [13–15] and traps [16–18] at the interfaces and within MoS_2 are mostly detrimental and lead to nonideal behavior. Such traps lead to reductions in mobility, gate sensitivity of conductance, and response frequency as well as increased noise and hysteresis. Some of the recent works demonstrate much improved MoS_2 FETs [19] and even observation of the Shubnikov–de Haas oscillations [20] in a similar two-dimensional (2D) material WSe_2. Nevertheless, traps offer interesting physics and application potential in memory devices and thus a more comprehensive understanding of the traps is desirable.

The threshold gate voltage at which an FET shows a steep rise in conductance is determined by both the traps' charge and the displacement charge across the gate dielectric. A positive hysteresis in the transfer characteristics of MoS_2 FETs has been studied as a function of various parameters [16–18,21,22] and attributed mainly to charge traps. This arises from the slow traps that have a timescale comparable to the gate-voltage sweep-time. This also amounts to a slow relaxation in channel's conductance. The fast traps do not lead to hysteresis, but they do shield the gate electric field. This widens the threshold region and together with the slow traps it forbids the access to ambipolar behavior in MoS_2 FETs even for gate voltages far exceeding the energy gap. Further, the electrostatic potential of the trap ions leads to reduced mobility while the change in the charge-state of traps gives rise to carrier density and mobility fluctuations.

The blocking transition results from an interplay between the strongly temperature-dependent thermally activated switching rate $\tau_s(T)^{-1}$ and the inverse of the measurement time τ_m. This crossover transition occurs at a temperature T_B at which $\tau_s(T_B) \approx \tau_m$. In the case of a narrow distribution of $\tau_s(T)^{-1}$ this can lead to a peak in the frequency dependence of the response. Thus the peak may be accessible experimentally in rare devices such as MoS_2-on-SiO_2 FETs with hBN at the interface as reported by Illarionov *et al.* [18]. In the temperature dependence, one would expect to find a hysteretic behavior below T_B and no hysteresis above it. This is the case in ferromagnetic nanoparticles, exhibiting superparamagnetism [23], and high electron mobility transistors [24]. In contrast, the blocking of traps in MoS_2 FETs leads to hysteresis reduction with cooling and negligible hysteresis at low temperatures. A similar behavior is also observed in graphene FETs [25]; though, the much sharper transfer characteristics in MoS_2 devices with a threshold gate voltage help carry out a more quantitative analysis.

In this paper, the transfer characteristics and its' time dependence in few-layer MoS_2-on-SiO_2 FETs as a function of temperature is presented. The hysteresis, its temperature dependence, and the blocking transition is modeled using some simplifications and analogy with superparamagnets. Finally, the traps' blocking is used to reversibly control the threshold voltage at 80-K temperature illustrating its application to nonvolatile memory devices.

II. EXPERIMENTAL DETAILS

Few-layer MoS_2 was transferred on SiO_2 by a dry method [26] from a natural MoS_2 single crystal (from SPI, USA) using commercial polydimethylsiloxane (PDMS) film-based viscoelastic stamp. The stamp is first fixed on a glass slide and an MoS_2 flake is transferred on it using scotch tape. The mechanism of this transfer process uses the viscoelastic

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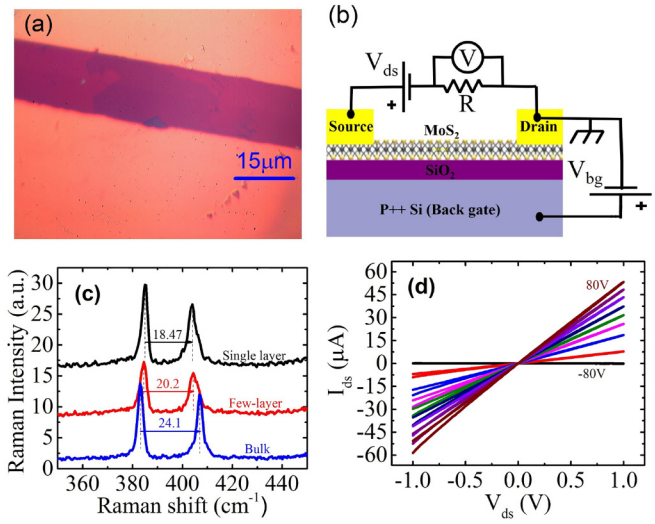

FIG. 1. (a) Optical image of few-layer Mos_2 with gold contacts. (b) The electrical schematic drawing of MoS_2 FET. (c) Raman spectra measured on exfoliated single layer, few-layer, and bulk MoS_2. (d) I_{ds} versus V_{ds} for a few-layer device at different gate voltage values.

response of the PDMS film, which behaves as an elastic solid for short timescales. So pulling the PDMS film from the scotch tape is done at high speed leading to strong adhesion of MoS_2 on PDMS as the viscoelastic solid makes a strong conformal contact with the flake [27]. The PDMS with MoS_2 flake is aligned with a SiO_2/Si substrate fixed by carbon tape on a XYZ micromanipulator and under an optical microscope. The stamp is removed with sufficiently low speed so that the adhesion of the flake to the stamp is weak and the flake gets transferred to the SiO_2 surface easily. Raman spectra, see Fig. 1(c), were used to confirm the few-layer nature of MoS_2.

The number of MoS_2 layers is determined by optical microscope contrast and verified by Raman spectroscopy with 532-nm wavelength laser excitation. As seen in Fig. 1(c) the separation between the E^1_{2g} and A_{1g} Raman peaks is 18.47, 20.20, and 24.1 cm^{-1}, which correspond to the single-layer, few-layer, and bulk MoS_2, respectively [28,29].

The source-drain contacts of 50-nm-thick gold film are made using mechanical masking with a 15-μm-diameter tungsten wire. The use of Au without a Cr/Ti adhesion layer promotes Ohmic contacts due to a very small difference in the contact potentials of Au and MoS_2 [30,31]. Mechanical masking avoids the use of organic lithography resist which can leave residue on MoS_2. The wire is carefully aligned under an optical microscope with few-layer MoS_2 on the SiO_2 substrate. Figure 1(a) shows an optical micrograph of a MoS_2 device with source-drain contacts. Two-probe conductance down to 80 K temperature was measured, with the configuration shown in Fig. 1(b) in a homemade vacuum cryostat with a heater for temperature control. A 10 kΩ series resistance was connected with the gate-voltage supply, which was controlled by a data acquisition card using a LABVIEW program. The Ohmic contacts were confirmed by two-probe current-voltage characteristics as shown in Fig. 1(d). The contact resistance in this device is estimated to be of 5 kΩ order from another four-probe device [32]. The cryostat was pumped by a turbomolecular pump to less than 10^{-4} mbar pressure. When the cryostat is dipped into liquid nitrogen for cooling, the vacuum is expected to be much better than this. The device was annealed at 400 K in a vacuum to minimize adsorbates on the MoS_2 surface.

III. MODELING OF CHANNEL TRANSPORT AND BLOCKING TRANSITION WITH TIME-DEPENDENT INTERFACE TRAPS

In the absence of traps the gate-voltage (V_g) dependence of the channel's carrier density in a 2D FET is dictated by the gate capacitance and the channel's quantum capacitance [35]. The traps change this dependence significantly. A given trap has two important attributes, namely, the electron energy level, when it is bound to the trap, relative to the channel bands, and the energy barrier height, from this energy level, for the trap electron to transition to the channel. The barrier dictates the rate of transition between the trap and the channel. This, together with the dynamics of trap occupancy and its influence on the channel conduction, have been elaborated on in the Supplementary Material [32]. Depending on the trap transit time, as compared to the gate-sweep time, the traps can be broadly divided into three categories: fast, slow, and extremely slow. A slow trap changes its state over a timescale comparable to the gate-sweep time and contributes to hysteresis. The fast traps change their state almost instantaneously while the extremely slow ones do not change their state at all over the gate-sweep time. Further, depending on the chemical nature, a trap can be of two types: an acceptor or donor. An occupied donor trap will be charge-neutral while an occupied acceptor will have $-e$ charge. Both these types can be incorporated in the same model [32] by using an appropriate offset charge density. The fast traps reduce the channel's response to gate voltage and thus lead to an increase in subthreshold swing (SS) given by [32]

$$\mathrm{SS} = \left(\frac{d\log(G)}{dV_g}\right)^{-1} = \frac{k_B T \ln 10}{e}(1+\gamma_{\mathrm{ftr}}). \qquad (1)$$

Here, $\gamma_{\mathrm{ftr}} = e^2 g_{\mathrm{ftr}}/C_{\mathrm{ox}}$ with g_{ftr} as the density of states (DOS) of fast traps and C_{ox} as the unit area gate-oxide capacitance. This helps us find g_{ftr} from the measured transfer characteristics.

A trap's charge state determines the channel's chemical potential μ_{ch}, which, in turn, dictates the traps' occupancy. This makes it a complex nonlinear system with coupling between the traps' occupancy and μ_{ch}. Thus, even the traps at a single energy and with the same barrier lead to nonexponential relaxation after a step change in the gate voltage is made. In fact, this leads to a slow tail in the relaxation [32] resembling a stretched exponential which can also arise from a distribution in the traps' energy barriers.

The channel carrier density, dictating μ_{ch} and conductance, is given by the sum of the gate-dielectric displacement charge-density and the slow traps' charge density. Note that, for a fixed μ_{ch}, the fast trap filling as well as channel quantum capacitance remain unchanged. A given sum of displacement and the slow-trap's charge can be realized in many ways depending on the gate-voltage history. Thus, at the two

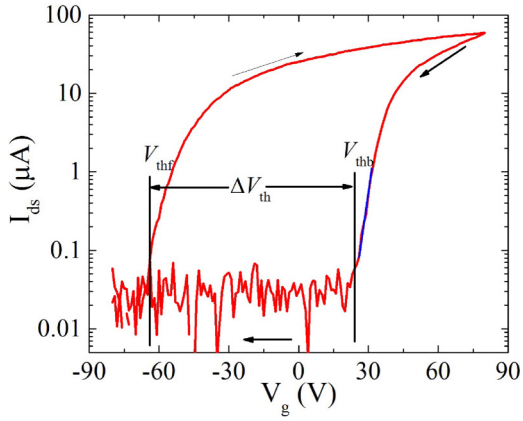

FIG. 2. The measured gate-dependent drain current for a few-layer MoS_2 at $V_{ds} = 1$ V as a function of V_g and over a V_g cycle from 0 to −80 V, then to +80 and back to zero.

conduction thresholds of the channel, occurring at different $V_g = V_{thf}$ or V_{thb} values during a closed-loop V_g sweep, see Fig. 2, the difference in the displacement charge and the slow traps' charge compensate for each other. Hence, $C_{ox}(V_{thf} - V_{thb}) = C_{ox}\Delta V_{th}$ directly reflects the change in the charge of slow traps. Eventually, for slow-traps having a distribution $n_{str}(\Delta_2)$ in the barrier heights Δ_2, the temperature (T) dependence of ΔV_{th} can be written as [32]

$$\Delta V_{th} \propto \int n_{str}(\Delta_2)\left[1 - \exp\left(-\frac{\tau_m/\tau_a}{\exp(\Delta_2/k_BT)}\right)\right] \times \exp\left(-\frac{\tau_m/\tau_a}{\exp(\Delta_2/k_BT)}\right) d\Delta_2. \quad (2)$$

Here τ_m/τ_a is the ratio of the gate-sweep time and the traps' attempt rate. In the case of the same barrier value Δ_2 for all the traps we expect a peak in ΔV_{th} at a blocking temperature $T_B = \Delta_2/[k_B \ln(\tau_m/\tau_a)]$. A distribution around a mean Δ_2 will increase the width of this peak. The nature of Δ_2 distribution may lead to nonobservability of some parts of this peak in the measurable temperature range.

IV. EXPERIMENTS ON HYSTERESIS, BLOCKING, AND GATE-COOLING

In this section we discuss experimental measurements focusing on the slow traps in an FET device with a few-layer MoS_2 on SiO_2. This helps us understand the energy and barrier distribution associated with these traps. The observed temperature dependence of hysteresis, quantified by ΔV_{th}, is presented next, together with the blocking model discussed earlier. Finally, the reversible handle on V_{th} through blocking of the traps in the desired charge state by cooling under different gate voltages is discussed.

A. Hysteresis and time dependence at room temperature

The transfer characteristics, shown in Fig. 2, of a few-layer MoS_2 FET at room temperature exhibits a large hysteresis. The on-state high conductance at $V_g = +80$ V due to n-doping can be attributed to the electron-rich sulfur vacancies and other n-type impurities present in natural MoS_2 crystals [15].

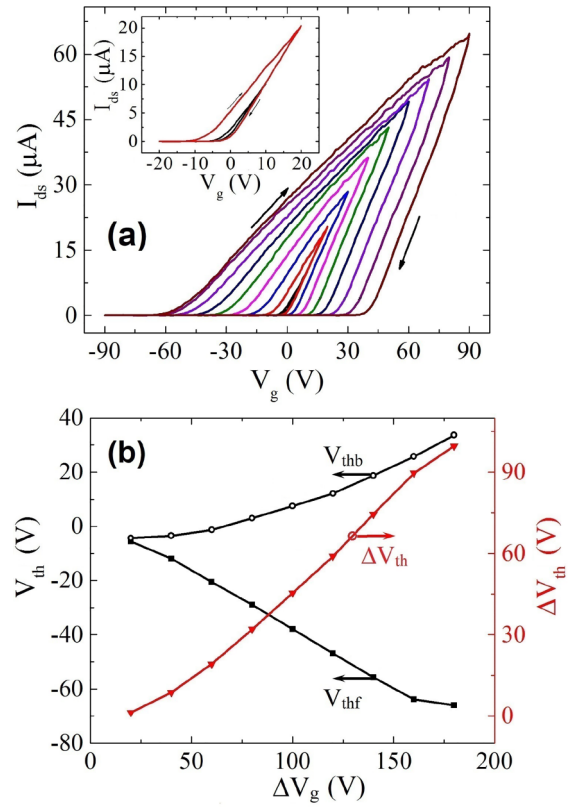

FIG. 3. (a) I_{ds} versus V_g at $V_{ds} = 1$ V for different sweep ranges of V_g from ±10 to ±90 V. All these curves are acquired at the same V_g sweep rate. The inset shows the zoomed-in portion for ±10 and ±20 V range V_g sweeps. (b) Variation of V_{thf}, V_{thb}, and ΔV_{th} with sweep range ΔV_g as extracted from (a).

This also leads to the pinning of E_c of MoS_2 close to the Fermi energy of the contact metal (gold) and thus negligible electron Schottky barrier at the MoS_2-metal contacts [36,37]. The blue line in Fig. 2 marks the subthreshold region for backward V_g sweep. The subthreshold swing (SS) from this line works out as 3 V/dec as opposed to 0.06 V/dec, i.e., the value expected for no traps, see Eq. (1). This measured SS gives $\gamma_{ftr} \approx 50$ and $g_{ftr} = 3.7 \times 10^{12}$ eV^{-1}cm^{-2}.

Figure 3(a) shows the measured $I_{ds} - V_g$ curves for different V_g sweep ranges varying from ±10 ($\Delta V_g = 20$) V, to ±90 V ($\Delta V_g = 180$ V). There is negligible hysteresis for ±10 V sweep range as V_{th} values for both the sweep directions are well within this sweep range and nearly equal. With increasing sweep range, V_{thf} reduces and V_{thb} increases leading to a monotonic rise in ΔV_{th}, see Fig. 3(b). Thus the slow traps, responsible for hysteresis, are nearly uniformly distributed over the μ_{ch} range accessible up to the largest V_g sweep range. From ΔV_{th} we can find the areal density of the slow traps responsible for hysteresis for a given ΔV_g by using $C_{ox}\Delta V_{th}/e$ with $C_{ox}/e = 7.6 \times 10^{10}$ cm^{-2}V^{-1}. Typical resulting values of areal density of slow traps $\sim 10^{12}$ cm^{-2} are smaller than the usual three-dimensional (3D) semiconductors and similar to other 2D materials like graphene [38,39].

A closer look at Fig. 3(b) shows an asymmetry between V_{thf} and V_{thb} with the first changing more with ΔV_g than the second. This is expected, for an n-doped channel, even for

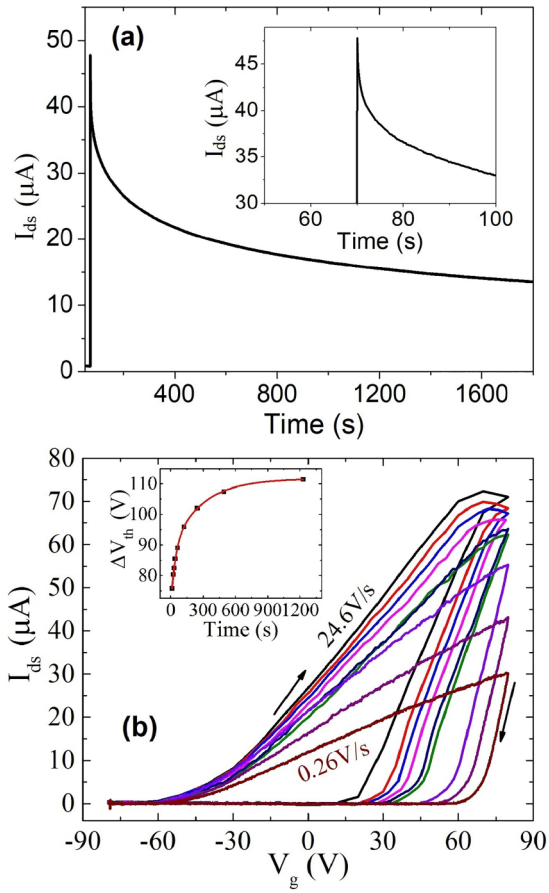

FIG. 4. (a) The measured time dependence of I_{ds} when V_g is changed abruptly from −80 to +80 V at $t = 70$ s. The inset shows the zoomed-in initial part of the relaxation. (b) I_{ds} versus Gate voltage curves for different sweep rates of back gate voltage at a fixed $V_{ds} = 1$ V. The solid squares in the inset show ΔV_{th} as a function of overall sweep time with the red line showing a fit to a sum of two exponential relaxations.

uniform distribution of traps as the magnitude of change in μ_{ch} for positive V_g is less than that for negative V_g. This is due to the rapid increase in the channel's quantum capacitance when μ_{ch} approaches E_c. This will amount to the activation of traps in a narrower energy range for the same magnitude positive V_g change than negative. A continuous rise in the rate at which V_{thb} changes with ΔV_g and up to the highest ΔV_g implies an increase in the slow traps' DOS near E_c. Also towards large ΔV_g values V_{thf} seems to saturate, indicating a reduction in slow trap's density of states when μ_{ch} moves away from E_c and into the gap. From the monotonic rise in ΔV_{th} with ΔV_g we conclude that the slow traps are somewhat uniformly distributed. Although from the details of the V_{thf} and V_{thb} variation the traps seem to be concentrated over a limited energy range close to E_c.

Figure 4(a) shows a measured time-dependent I_{ds} as a function of time when V_g is abruptly changed from −80 to +80 V. There is a fast initial relaxation followed by a slow stretched exponential tail indicating multiple timescales. This relaxation would be rather complex to fit to a microscopic model [32] in the absence of the knowledge about the distribution of trap energies and activation barriers. A fitting with the multiexponential or stretched exponential does work and it has indeed been used [21] to conclude a distribution in barrier energies. However, due to the coupling between the dynamics of different trap's occupancy and μ_{ch}, even traps at single energy and with the same barrier can lead to nonexponential relaxation, with a long tail that can resemble a stretched-exponential [32].

As a consequence of this slow relaxation of traps, the hysteresis has a significant dependence on the V_g sweep rate for a fixed sweep range. Figure 4(b) shows the conductance hysteresis loops acquired at different sweep rates from 0.26 to 24.6 V/s. A high sweep rate also gives higher peak conductance as a lesser number of traps acquire negative charge leading to more electrons in the channel. In fact, for some of the very fast sweep rates, a saturation or a downturn in channel conductivity is seen with V_g due to a delayed response of the traps which depletes electrons from the channel. As discussed earlier, the rate of filling of an empty trap state at a given energy will increase with V_g as μ_{ch} rises with V_g. The inser of Fig. 4(b) shows the variation of ΔV_{th} as a function of the V_g sweep time. It fits well to a double exponential function, $\Delta V_{th} = \alpha - \beta e^{-r_1 \Delta t} - \gamma e^{-r_2 \Delta t}$ with $r_1^{-1} = 35$ s, $r_2^{-1} = 292.5$ s, and α, β, and γ as other fitting parameters.

B. Blocking transition of interface traps

Figure 5(a) shows $I_{ds} - V_g$ curves at several temperatures between 300 and 80 K over a ±80 V V_g sweep range and a 2.6 V/s sweep rate. For these measurements, the device was first kept at room temperature at $V_g = 0$ for 2 to 3 hours to equilibrate the traps and then cooled and stabilized at each different temperature keeping $V_g = 0$. The hysteresis can be seen to reduce with cooling though the rate of reduction is not monotonic as seen in Fig. 5(b). ΔV_{th} reduces slowly near room temperature and the rate of reduction, i.e., $d\Delta V_{th}/dT$, peaks near 225 K and then the rate as well as ΔV_{th} diminish as a 80-K temperature is approached.

When compared to superparamagnets (SPM) with parameters relevant to traps, one expects to see a peak in ΔV_{th} [32]. In SPM, the M-H curves show hysteresis below the blocking temperature T_B and the hysteresis vanishes as temperature rises above T_B. There are four major differences between the slow traps in MoS_2 and a SPM, as elaborated in the Supplementary Material [32]. (i) The attempt rate for traps is of 10^{12} s^{-1} order or higher while for SPM the attempt rate is of 10^9 s^{-1} order. (ii) The barrier height for slow traps can be of 1 eV order while that for SPM is only tens of meV. (iii) In SPM, the barrier can be made to vanish by applying less than 1 Tesla magnetic field. However, in the case of slow traps, the change in μ_{ch} for experimentally possible V_g values is much smaller than the barrier height. This is due to the large overall trap density in MoS_2 on SiO_2. Thus, at low temperatures, the slow traps do not change their state, even at extreme V_g values, and one does not see hysteresis. (iv) There is a much wider distribution in barrier heights in the case of MoS_2-on-SiO_2 traps as compared to that in SPM. Thus the hysteresis of traps does not vanish at room temperature or slightly above it as the larger barrier height traps contribute to hysteresis at higher temperatures. In contrast, the hysteresis in high-electron-mobility transistors (HEMTs) is seen only at very low temperatures [24]. This is similar to SPM and

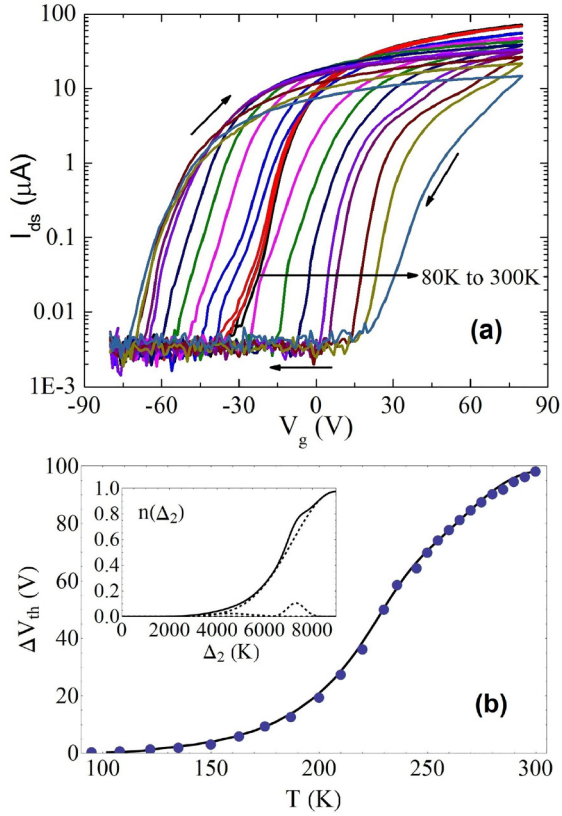

FIG. 5. (a) Temperature dependence of I_{ds} versus V_g curves at $V_{ds} = 1$ V between 80 and 300 K. (b) The solid circles show ΔV_{th} as a function of temperature. The solid line shows the calculated variation of ΔV_{th} using Eq. (2) with the barrier distribution function $n(\Delta_2)$ depicted by the solid line in the inset. This $n(\Delta_2)$ is the sum of three Gaussian distributions shown by discontinuous lines in the inset. The traps with Δ_2 beyond 8000 K do not contribute to ΔV_{th} variation over the studied temperature range.

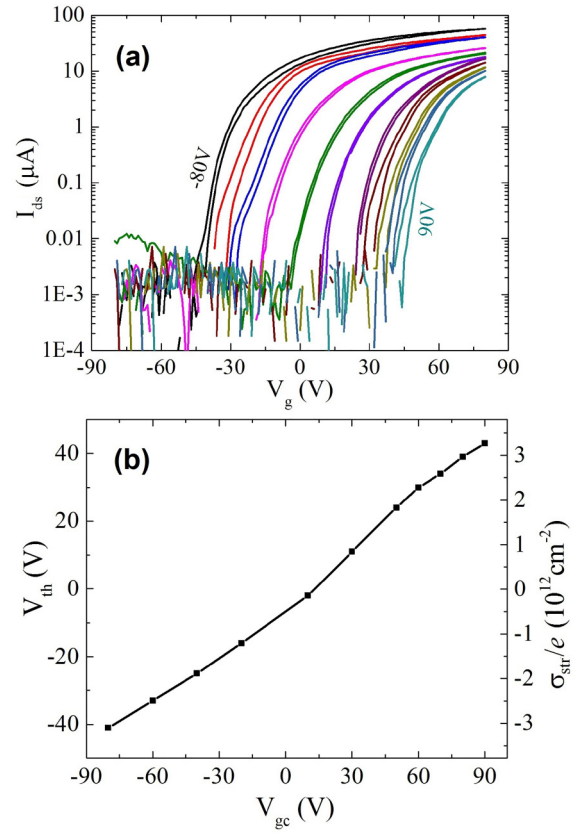

FIG. 6. (a) Effect of cooling the device from 350 K to 80 K under different applied gate voltages V_{gc} from −80 V to 90 V. All the curves measured at 80 K and for $V_{ds} = 1$ V show negligible hysteresis. (b) Variation of V_{th} with V_{gc}. The axis labels on the right in (b) show the corresponding blocked slow trap density.

presumably due to the small barrier height and much less the traps' density, which can make the shift in μ_{ch}, in response to V_g, larger to make the barrier vanish.

The continuous line in Fig. 5(b) shows the temperature dependence of ΔV_{th} found using Eq. (2) and a Δ_2 distribution depicted in the inset. Here we use a fixed $\tau_m/\tau_0 = 10^{13}$ though a change in this value by up to even two orders of magnitude only slightly affects the required $n(\Delta_2)$ for fitting the measured $\Delta V_{th}(T)$. Traps with Δ_2 higher than 8000 K do not contribute to the hysteresis at temperatures 300 K or below. One may see a decline in ΔV_{th} at further higher temperatures, however, we find that the $I_{ds} - V_g$ curves do not exhibit so sharp transitions at V_{thf} and V_{thb}. This could be from the activation of a larger number of traps and some of the slow traps may turn into fast ones at higher temperatures. Other extrinsic effects, such as the traps' diffusion, may also come into play. Eventually, the very high V_g needed to access V_{thf} and V_{thb}, and particularly at high temperatures, also leads to the breakdown of the dielectric oxide and permanent device damage.

C. Gate cooling and reversible control of V_{th}

Figure 6(a) shows I_{ds} versus V_g measured at 80-K temperature after cooling the device from 350-K temperature to 80 K in the presence of different gate voltages, labeled as V_{gc}, between −80 and 90 V. The device was first warmed to 350 K in a vacuum and kept at the desired V_{gc} for an hour before cooling it down to 80 K. As expected there is negligible hysteresis at 80 K, but more striking is the reversible change in V_{th} over a wide range from −40 to +40 V. At negative V_{gc} the traps get blocked in a positively charged state. This trap charge electron dopes the channel and thus a negative V_g is needed to deplete it. Similarly a positive V_{gc} leads to traps blocked with negative charge that depletes the electrons from the channel and thus a positive V_g is needed to make it conduct. In this way the traps act as a controllable virtual gate. In fact, this also demonstrates heat-assisted nonvolatile memory with a high achievable ON-OFF ratio.

Figure 6(b) shows the variation of V_{th} with V_{gc}. The V_{th} value at 80 V can be converted into an appropriate charge density σ_{str} associated with the blocked slow traps. The axis on the right shows this $\sigma_{str}/e = C_{ox}V_{th}$. Another fact from this figure is the nearly linear relation between V_{th} and V_{gc} with a slope close to 1/2. This indicates that about half of the charge induced by V_{gc} gets stored in the blocked slow traps while the remaining half is taken up by the fast traps and channel carriers. This is striking as the change in μ_{ch} with V_g near the conduction threshold is quite nonlinear, see Fig. 4 of the Supplementary Material [32].

V. DISCUSSION AND CONCLUSION

On the possible origin of these slow interface traps in MoS_2-on-SiO_2, the thermally grown SiO_2 surface either houses these traps directly or it is more susceptible to the adsorption of ambient species. The siloxane-terminated sites can easily hydrogen-bond with ambient water [40,41] that can contribute to slow traps. The slow traps can be efficiently disabled by polymethyl methaacrylate (PMMA) or hexamethyldisilane (HMDS) passivation [32] but the fast traps do not seem to be much affected by this, indicating that the fast traps may be intrinsic to MoS_2 and could be related to S vacancies.

In conclusion, a temperature-dependent study of few-layer MoS_2 FET transfer characteristics shows hysteresis with a large difference ΔV_{th} between the backward- and forward-sweep threshold gate voltages. This is modeled using the complex coupled dynamics of channel carrier density and slow traps' occupancy. The observed temperature dependence of ΔV_{th} is attributed to the blocking of traps and fitted to a distribution of energy barriers for charge exchange between the traps and the channel. Finally, the blocking helps to get nearly nonhysteretic behavior at 80-K temperature with a voltage threshold programmable by gate-cooling voltage illustrating a nonvolatile memory device. Further, recent work on a neuromorphic device [42] clearly demonstrates the potential of the interface traps in MoS_2-on-SiO_2. The understanding and the model proposed in this work can help optimize these traps for such applications.

ACKNOWLEDGMENTS

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